Sink or Swim at 28 Gbps™

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Abstract: How do you know that your signal integrity software is qualified for the analysis of interconnects with signals running at 28-32 Gbps? The software vendor told you so? How does the vendor know? Most of the time, it is the "sink or swim" situation for the SI software user. One way to figure it out is to use a validation platform such as Wild River Technology's CMP-28/32 Channel Modeling Platform providing interconnect structures specifically designed to benchmark the signal integrity software at these data rates. Just run the post-layout analysis of interconnects on the validation platform and compare with the pre-qualified measurements taken by an expert up to 50 GHz. The validation process may be that simple in general, but has some peculiarities discussed in this article.

Introduction

Design of PCB and packaging interconnects for data links running at 28-32 Gbps bitrates and beyond is a challenging problem to say the least. It requires accurate electromagnetic analysis over extremely broad frequency bandwidth from DC to 40-50 GHz. What complicates it further is the absence of the broadband frequency-continuous dielectric and conductor roughness models. In addition, the final board is usually manufactured not as designed due to un-controlled variations and manipulations by the board manufacturers to "dial in the impedance". It is also extremely difficult to make high-quality measurements up to 50 GHz. So, is it possible to design and manufacture interconnects and have acceptable analysis to measurement correlation up to 40-50 GHz systematically? To answer, four necessary elements for design success were formulated in [1]. One of the elements is systematic benchmarking of manufacturing, measurement, and the software. Systematic in this context means analysis-to-measurement correlation observed not just for one or two structures (test coupons for instance), but rather for broad range of typical interconnects – single-ended and differential, strip and micro-strip, simple planar and with the vertical transitions or vias, etc. Such comparison should be done consistently both in frequency (magnitude and phase of S-parameters) and time (TDR and eye diagram) domains. In other words, the systematic validation or benchmarking is needed to make sure that the board is manufactured as designed, measurements are taken properly and, finally, that the interconnect analysis software provides acceptable accuracy. It is a whale of a project, if you do it yourself from scratch. Though, the process can be facilitated if you start with a readily available validation platform such as CMP-28/32 from Wild River Technology [2]. The platform was designed to illustrate and facilitate systematic analysis to measurement validation process at 28-32 Gbps and to demonstrate that interconnects for 28-32 Gbps can be predictably designed. Use of such a platform saves time and lowers the risks by benchmarking against known and already measured and simulated structures. The CMP-28 platform [2] and Simbeor electromagnetic signal integrity software [3] are used here to illustrate signal integrity software validation process for 28 Gbps interconnects. The validation process can be divided into three steps:

1. Measure S-parameters with VNA up to 50 GHz and qualify them with formal quality metrics and, optionally, compare with S-parameters measured by an expert;

2. Identify or confirm broadband dielectric and conductor roughness models;

3. Simulate all test structures with the identified material models and verified board design adjustments and compare with the measured data in frequency and time domains;

Validation platform

A validation platform is a very important tool for signal integrity software benchmarking or formal pre-qualification. Accuracy and limitations of the software can be easily identified with the analysis to measurement comparisons on a typical set of interconnect structures. A validation platform can be either developed in-house or purchased from a vendor. One of the industry-first validation platforms was the physical layer reference design board (PLRD-1) from Teraspeed Consulting Group [4]. Use of the PLRD-1 revealed the need and enabled development of the industry-first broadband dielectric and conductor roughness models in Simbeor software. Another example of validation platform is the CMP-28/32 channel modeling platform from Wild River Technology [2]. Both CMP-28 and 32 versions contain 27 microstrip and strip-line interconnect structures. All structures are equipped with either 2.92 mm (CMP-28) or 2.4 mm (CMP-32) connectors to facilitate accurate measurements with a VNA. The CMP-28/32 platform is shown in Fig. 1 and will be used here to demonstrate the systematic approach to the analysis to measurement correlation.

The CMP-28/32 platform contains multiple single-ended and differential line segments, suitable for identification or confirmation of material models, and also serve as the simplest validation structures. It also contains practical strip and micro-strips link paths with vias and cross-talk. In addition, it has a set of resonant structures to validate analysis of t-lines with different widths and do validation for highly reflective interconnects. Complete platform description is available at [2] and [5].
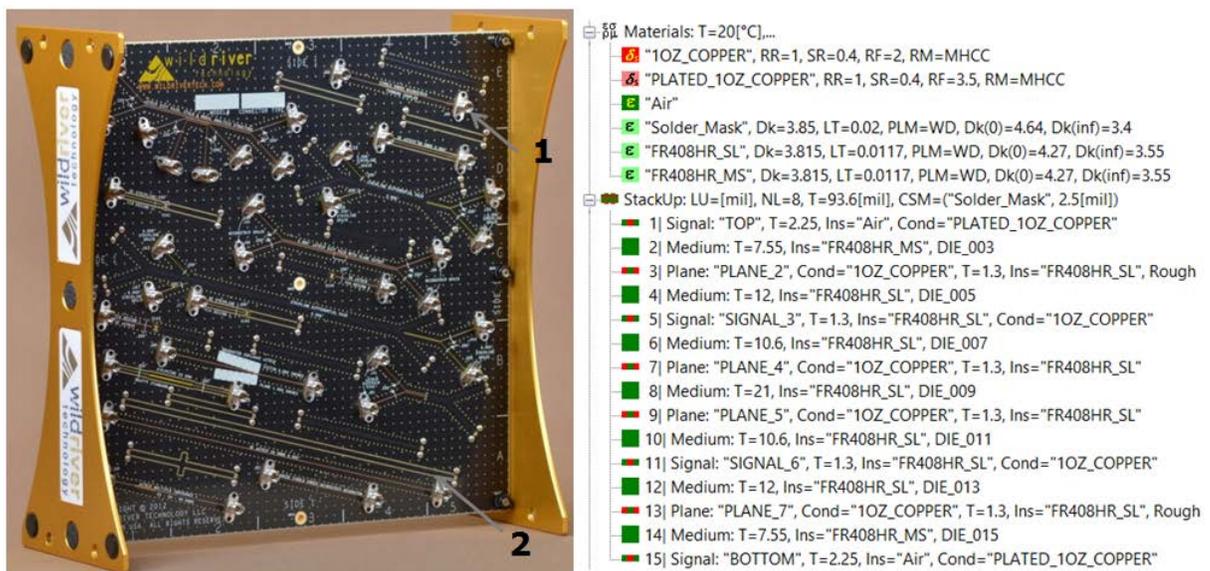
Fig. 1. CMP-28/32 channel modeling platform with 27 structures to benchmark software with stackup and broadband dielectric and conductor roughness models identified in Simbeor software (see details in [5]).

Step 1: S-parameters measurement and pre-qualification

The first step in the systematic validation process is to make S-parameter measurements with VNA up to 50 GHz for 28-32 Gbps data rates and pre-qualify them for further analysis. For the reference, the CMP-28/32 kit includes S-parameter in Touchstone format measured for all structures by an expert with SOLT calibration up to the SMA connector. We will start with the example of formal pre-qualification of these measured data. The process is described in details in [1], [6]. We start with preliminary estimation of the passivity, reciprocity and causality metrics computed for discrete and bandwidth limited datasets. All metrics conveniently range from 0 (bad) to 100 (excellent) and further subdivided into bad, questionable, acceptable and good intervals as described in [6]. If all metrics fall into acceptable (blue) or good (green) intervals, we proceed and estimate the final quality metrics with the rational approximation or rational compact model. Models measured with high quality allow rational approximation with high accuracy – the root mean square error of such approximation can be used to construct the final quality metric [1], [6]. The end result of the measured S-parameters quality evaluation in Simbeor software is shown in Fig. 2. All models measured by the expert pass the final quality test (Quality column).

Touchstone Analyzer

File name	Quality	Passivity	Reciprocity	Causality
C:\Repository\Simbeor\CMP-28_Simbeor_Kit_Rev4\CMP-28_Rev4\Touchstone_Files\1stc...				
cmp28_gnd_voids_p1J74_p2J75.s2p	99.5	100	99.4	-
cmp28_graduated_coplanar_p1J70_p2J69.s2p	99.7	100	99.5	-
cmp28_mstrp_2in_p1J1_p2J2.s2p	99.5	100	99.7	-
cmp28_mstrp_8inch_p1J4_p2J3.s2p	99.7	100	99.8	-
cmp28_mstrp_Beatty_25ohm_p1J25_p2J26.s2p	99.6	100	99.4	-
cmp28_mstrp_multiZ_p1J31_p2J32.s2p	99.6	100	99.3	-
cmp28_mstrp_p1J30_p2J29.s2p	99.6	100	99.8	-
cmp28_mstrp_resonator_p1J22_p2J22.s2p	99.7	100	99.7	-
cmp28_mstrp_whiskers_p1J68_p2J67.s2p	99.5	100	99.8	-
cmp28_strpl_2in_50ohm_p1J6_p2J5.s2p	99.6	100	99.1	-
cmp28_strpl_2in_Capacitive_p1J10_p2J09.s2p	99.5	100	99.5	-
cmp28_strpl_2in_Inductive_p1J12_p2J11.s2p	99.5	100	99.4	-
cmp28_strpl_8inch_p1J7_p2J8.s2p	99.6	100	99.7	-
cmp28_strpl_Beatty_25ohm_p1J28_p2J27.s2p	99.7	100	99.4	-
cmp28_strpl_resonator_p1J23_p2J24.s2p	99.6	100	99.4	-
cmp28_via_pathology_p1J65_p2J66.s2p	99.6	100	99.8	-

Fig. 2. Example of formal quality evaluation in Simbeor software for a subset of S-parameters measured for CMP-28 platform.

Note that the frequency-continuous approximation of the discrete Touchstone models with the rational compact models is 100% causal by definition, because of the passivity is ensured by the software from DC to infinite frequency in this process. Such models are usable not only for the original Touchstone model quality evaluation, but also for further validation in time domain - fast and accurate computations of TDR/TDT and eye diagrams.

Step 2: Broadband material model identification

After S-parameters are measured and pre-qualified, the next step is to identify broadband dielectric and conductor roughness models. The model identification with Generalized Modal S-parameters (or GMS-parameters) is the simplest and most accurate way to do it [7]-[9]. It requires S-parameters measured for two line segments with different length. Line of any type with any impedance can be used. It also does not require modelling of the connectors and launches. The CMP-28/32 platform contains 2 and 8 inch segments of single ended stripline and microstrip traces and 2 and 6 inch segments of differential stripline and microstrip traces that can be used to extract or confirm dielectric and conductor roughness models.

We start with the single-ended strip line and first extract reflection-less GMS-parameters for 6 inch segment from the measured data shown in Fig. 3 (red and blue lines with stars). The useful range of the GMS-parameters is about 30 GHz for the insertion loss and 40 GHz for phase delay (restricted by the manufacturing variations). Next we build a model of 6-inch strip line segment with quasi-static field solver and first define dielectric model as the wideband Debye (aka Djordjevic-Sarkar) [7] with dielectric constant Dk=3.66 and loss tangent LT=0.0117 as specified for Isola FR408HR material at 1 GHz. To match the measured and modeled phase delay as shown in Fig. 3, the Dk in the model needed adjustment from 3.66 to 3.815. This adjustment can be explained by the anisotropy of the composite dielectric. To match measured and modeled generalized modal insertion loss, we have two choices – increase the loss tangent or model conductor roughness. We choose to simulate conductor roughness with the simplest Modified Hammerstad model [7], defined by two surface roughness (SR) and roughness factor (RF) parameters. It is applied to the conductor surface impedance in the model. SR=0.4 um and RF=2 produced perfect good for the generalized modal (GM) insertion loss as shown in Fig. 3.
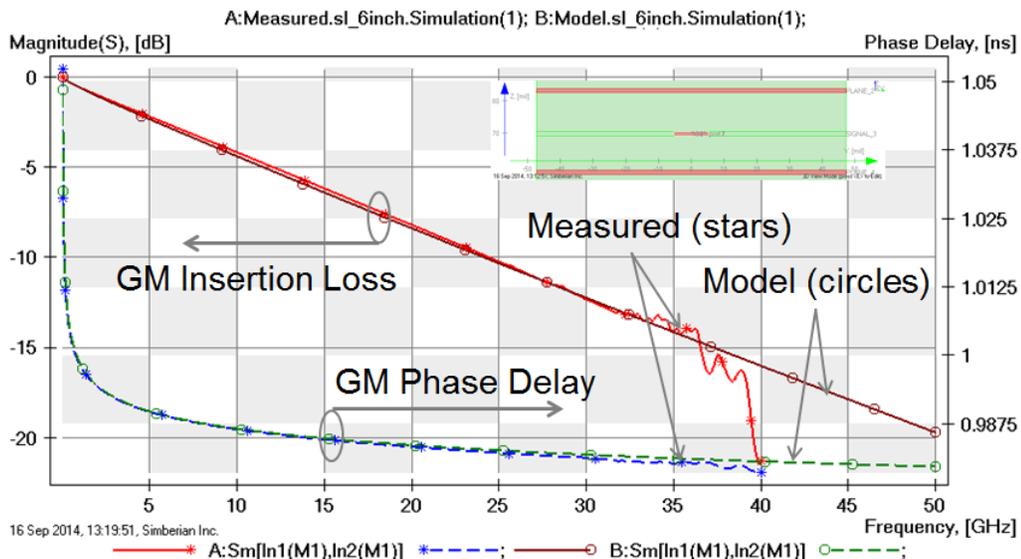
Fig. 3. GMS parameters computed from S-parameters measured for 2 and 8 inch strip line segments (red and blue lines) and modeled for 6 inch strip line segment (brown and green lines) with wideband Debye dielectric model with Dk=3.815, LT=0.0117 @ 1 GHz, and Modified Hammerstad conductor roughness model with SR=0.4 um, RF=2.
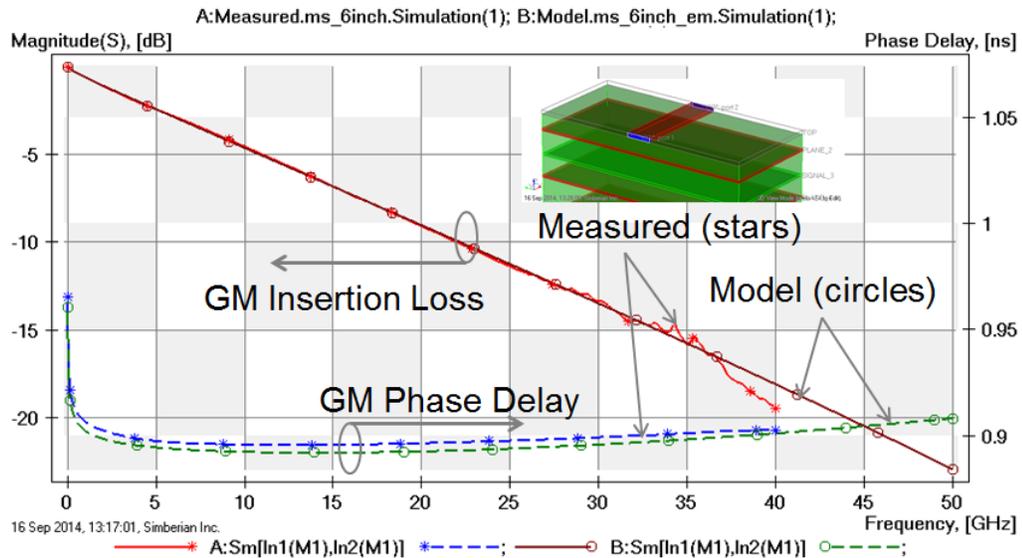
Fig. 4. GMS parameters computed from S-parameters measured for 2 and 8 inch micro-strip line segments (red and blue lines) and modeled for 6 inch micro-strip line segment (brown and green lines) with the same FR408HR model as for the strip line and wideband Debye model for solder mask with Dk=3.85, LT=0.02 @ 1 GHz and Modified Hammerstad conductor surface roughness model with SR=0.4 um, RF=3.5.

FR408HR model identified with the strip line should also work for the microstrip line. It can be validated with the GMS-parameters computed from the measured S-parameters of 2 and 8 inch microstrip line segments and shown in Fig. 4. The 6 inch segment model is constructed with the electromagnetic solver to capture the high-frequency dispersion seen as the upward trend in the phase delay in Fig. 4. In addition we define solder mask model as the wideband Debye with the values taken from the manufacturer specification: Dk=3.85 and LT=0.02 at 1 GHz. Good match of the phase delay can be observed in Fig. 4. To match measured and modeled GM insertion loss, the conductor roughness parameters for the microstrip line needed adjustment of the roughness factor from 2 to 3.5. That concludes the material model identification. The process is automated in Simbeor software and typically takes 5-10 minutes.

As an optional, but recommended step, GMS-parameters extracted from S-parameters measured for 2 and 6 inch differential links can be further used to confirm (or further adjust) the models extracted with the single-ended lines as demonstrated in [5].

Note that the identified dielectric and conductor roughness models are simple frequency-continuous expressions [7]. The models are not just tables of Dk and LT frequency points and do not end where the measured data end. The extracted models are expected to be sufficiently accurate from DC up to 40 GHz and well above that frequency – the validation step will confirm it.

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Step 3: Analysis to measurement validation

After the S-parameters are measured and pre-qualified and broadband material models are identified, the final step is to run the post-layout analysis on all 27 structures on the validation platform and compare magnitude and phase of S-parameters, TDR and eye diagrams for 28 Gbps signals. Note, that before proceeding with the post-layout analysis and even before the material model identification step, all stackup and trace width adjustments made by the PCB manufacturer must be discovered. If no information is available, the board has to be cross-sectioned to proceed further. PCBs are rarely manufactured as they appear in your favorite layout tool, but a post-layout analysis tool usually takes geometry directly from the board design files. Changes in stackup, trace width and shape, and via back-drilling have to be verified and applied to the interconnect geometry consistently before running any analysis. Believe it or not, even the most accurate electromagnetic solver will produce garbage results without proper geometry description. Note that these manufacturing variations introduce additional uncertainties, and they usually cause discrepancies at frequencies above 20-30 GHz and so far cannot be properly accounted for.

The validation can be done in two ways – for just the PCB interconnect part with de-embedded connectors, or for complete link paths with the connectors and optionally adapters (exactly as measured in step 1). De-embedding is the additional step that can be problematic and error-prone. From the earlier validation experience [4] we have learned that the de-embedding of PCB structures with TRL procedure produces acceptable results only for highly reflective structures such as resonators or highly reflective vias. The highly reflective structures can be used to validate the software, but they are not typical for the actual interconnects with the minimized reflection. TRL de-embedding produces large errors in the reflection for the typical low-reflective structures. It makes it difficult or even practically impossible to use TDR for the validation. This is due to large manufacturing and dielectric properties variations in the test fixtures typical for PCB realm. Thus, we proceed with the second option – validation for the complete link path. All measurements for the step 1 were done with the 2.92 mm SMA connectors and 2.92 to 2.4 coaxial adapters – no models were available for both. To overcome this obstacle, the model of the connector with the adapter was simply synthesized from S-parameters measured for two connectors and two adapters connected symmetrically back-to-back. We used cascaded connection of 4 coaxial sections to model adapter and connector and then matched both magnitude and phase of the reflection and transmission of the measured S-parameters and the circuit model of the back-to-back structure [5]. In addition, models for all launches (PCB part) were built with the 3D electromagnetic solver as a part of the post-layout electromagnetic de-compositional analysis in Simbeor. That eliminated the error-prone de-embedding step.

Technically, comparison of the magnitudes and phases of S-parameters is sufficient to either make a decision on the accuracy or spot a problem. However, comparison in time domain is usually also needed and may reveal additional problems. Comparison with TDR/TDT response that is measured directly with TDR scope requires modeling with the step function with the shape and spectrum matching to one used in the experiment. Similar situation is with the eye diagrams. Use of the ideal ramp step functions or PRBS with ideal trapezoidal shaped pulses may obfuscate and distort the results. Alternatively, measured and modeled S-parameters should be used to do all time domain computations with exactly the same stimuli matching the bandwidth of the model. It can be done in two ways – either with convolution with the impulse response computed directly from discrete S-parameters with IFFT, or with the rational approximation and fast recursive convolution as it is done here. The rational approximation is frequency-continuous and naturally extends S-parameters to DC and to infinite frequencies. It is also causal by

definition if passivity is ensured. The accuracy of the time domain analysis in this case is defined only by the accuracy of the rational approximation. In other words, the accuracy is always under control, unlike in case of analysis with IFFT where interpolation and extrapolation introduce uncontrolled errors. In addition, the recursive convolution is exact for piecewise linear signals and much faster than the direct convolution. Thus, we will naturally use rational approximation for all time-domain computations here.

After all modeling decisions on what to compare and how to compare are made, we run the post-layout analysis for all 27 structures on the CMP-28 platform and compare the magnitudes of S-parameters, phase and group delays (and optionally phases), TDR computed with Gaussian step with 20 ps 10-90% rise time and eye diagrams computed with PRBS signal with 25 ps rise and fall time generated with LFSR with order 32. Two examples of the validation are shown in Fig. 5 and Fig 6.
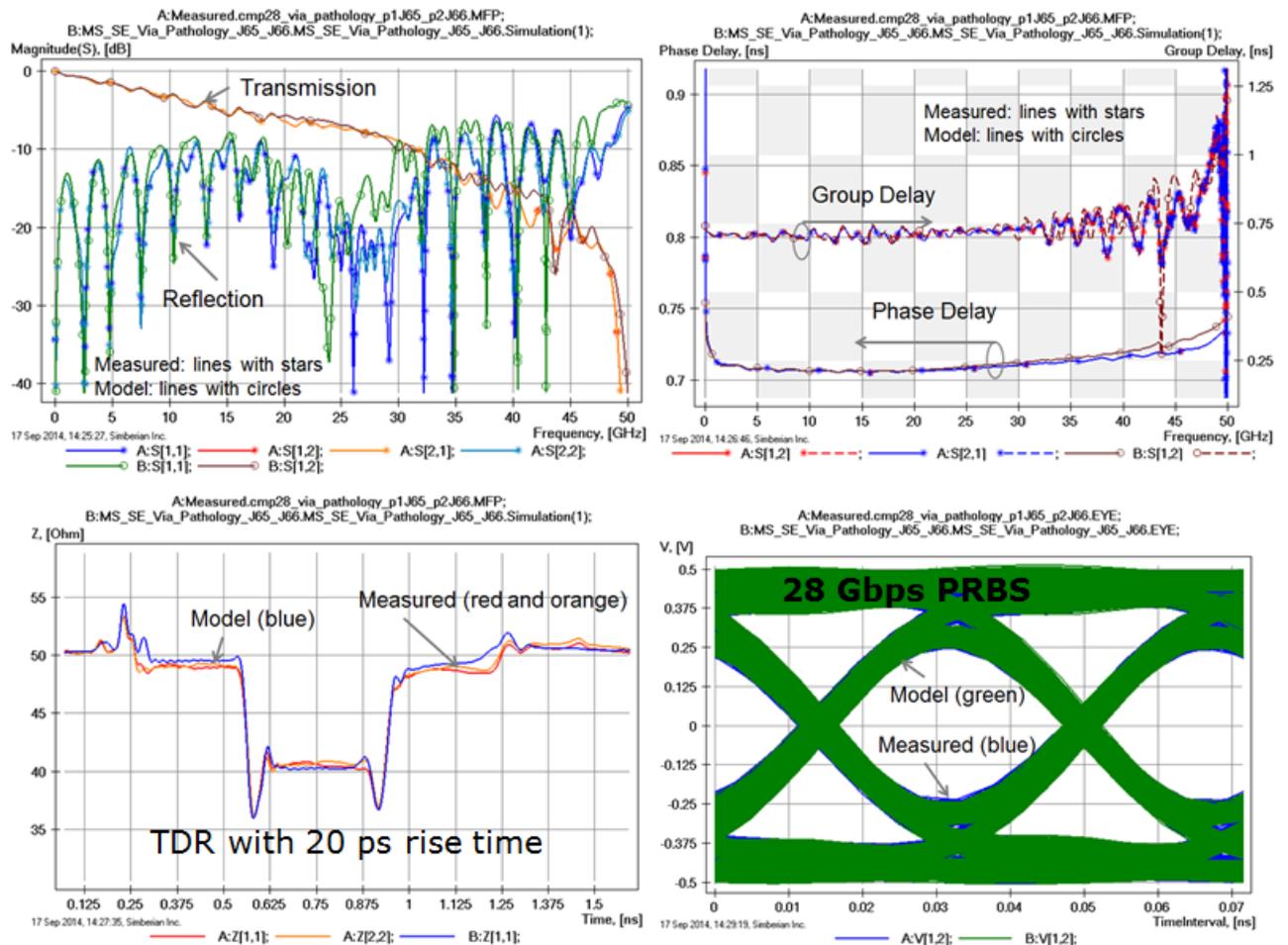
Fig. 5. Model to measurement validation results for microstrip link with two capacitive vias (structure 1 in Fig. 1): Magnitudes of the transmission and reflection parameters (top left); Group and phase delays of the transmission (top right), TDRs computed with 20 ps rise time Gaussian step (bottom left); Eye diagrams for 28 Gbps PRBS signal (bottom right - on top of each other literally).
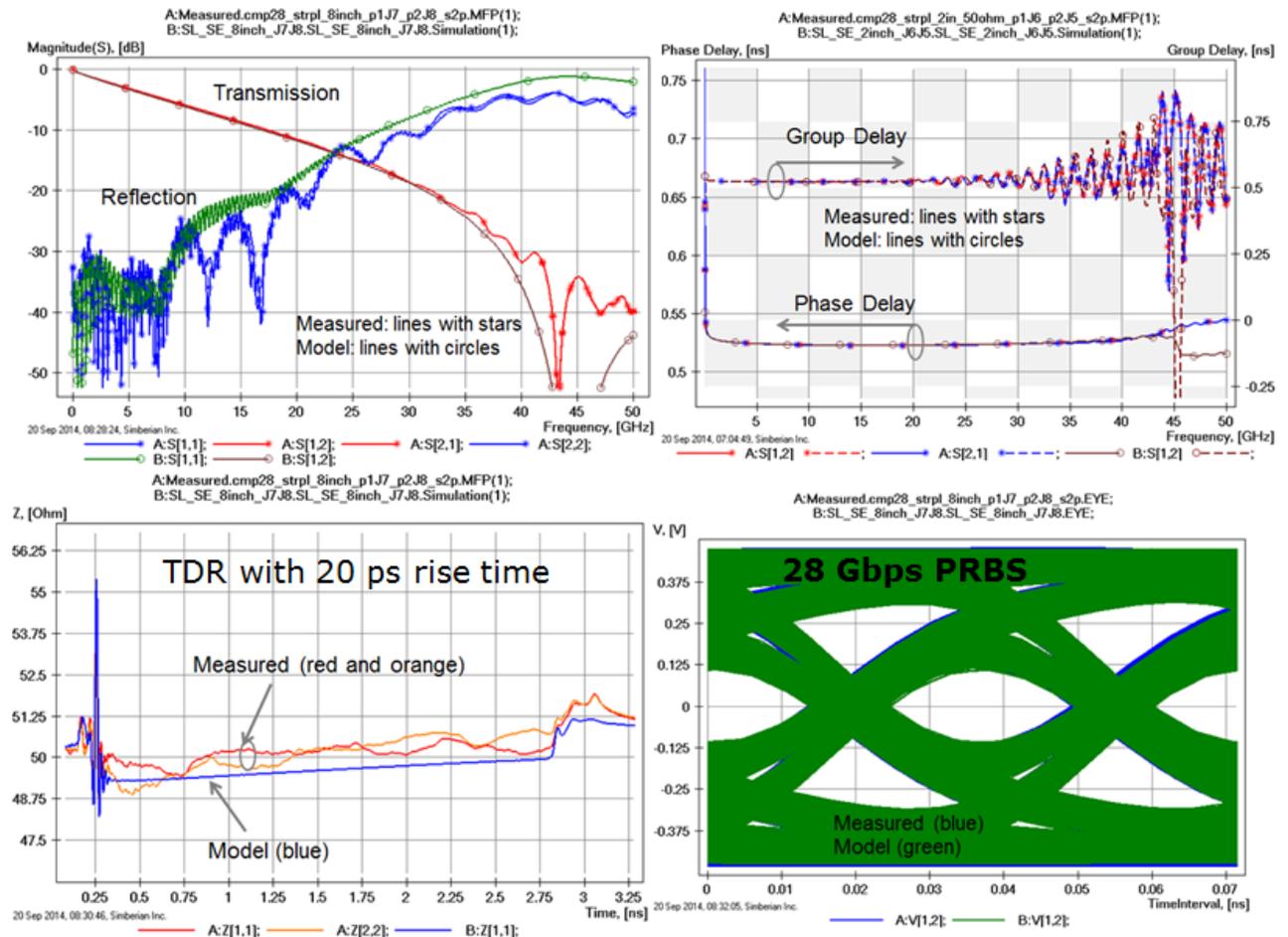
Fig. 6. Model to measurement validation results for 8-inch strip line link (structure 2 in Fig. 1): Magnitudes of the transmission and reflection parameters (top left); Group and phase delays of the transmission (top right), TDRs computed with 20 ps rise time Gaussian step (bottom left); Eye diagrams for 28 Gbps PRBS signal (bottom right - on top of each other literally).

      Results for microstrip line link with two capacitive vias (structure 1 in Fig. 1) are shown in Fig. 5. It contains connectors with adapters on both ends, microstrip launches with through-hole vias, two segments of microstrip line with about 50 Ohm impedance, two vias and one segment of wide microstrip line in the middle. The link is not optimal by design and represents highly reflective structure. We can conclude that the correlation is very good in this case and all discrepancies may be explained by the manufacturing and material properties variations.

      Results of validation for a relatively low-reflective structure are shown in Fig. 6. It is a simple 8-inch segment of single-ended strip line with launches, connectors and adapters on both ends (structure 2 in Fig. 1). The launches in this case are back-drilled with the goal to have less than 10-mil via stubs. Though, the manufacturer specified that the stubs may have +- 5 mil variation. 10 mil stubs were used in the model. Considering this and other types of variations, the correlation is acceptable. See all details of the analysis and analysis to measurement correlation for all 27 structures on CMP-28 platform in [5].

Conclusion

A systematic process of the analysis to measurement validation up to 50 GHz is introduced here. The process is illustrated in this article with the CMP-28/32 validation platform and Simbeor software. Note that the validation problems can fall into three categories: manufacturing, measurement, and analysis, and only measurement quality and the interconnect analysis parts are covered here. Following the procedure, you can easily qualify or reveal problems in your signal integrity software of choice. Just try to do the analysis of all 27 test structures on CMP-28/32 validation platform and swim at 28 Gbps and beyond… Do not forget to compare the productivity and cost of the tools. Finally, is your software qualified for the analysis of PCB interconnects running at 50 Gbps? – The question is rhetorical so far ☺

References

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