How Interconnects Work: Minimal-reflection 90-degree bends in strip lines

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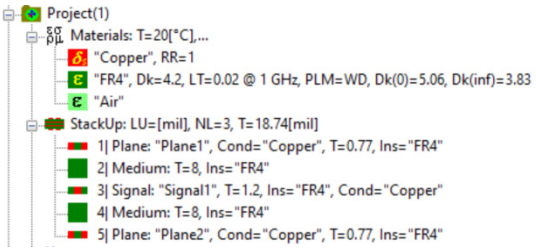
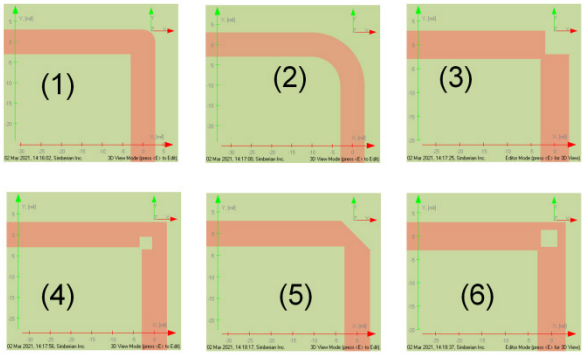
Bends in strip and microstrip lines are often discussed as a source of reflection in PCB interconnects (see SI list reflector http://www.freelists.org/archives/si-list/ - search for “bends” and you will get over 400 matches). It is practically impossible to detect the effect with TDR due to smallness of effect and not sufficient bandwidth and dynamic range of such measurements. Precise frequency-domain measurements are required to detect the effect. The effect of bend may be hidden by the mismatch at the connectors or probes, de-embedding errors, frequency-dependent transmission line impedance and so on. Precise de-embedding is required to reveal the effect. That is hard to do on PCBs due to variations in dielectric properties and variations of trace geometry. **Alternatively electromagnetic analysis with precise de-embedding can be used to reveal the effect and to minimize the reflections.** This short article demonstrates how to do quick “what-if” numerical experiments with Simbeor electromagnetic signal integrity software and provide design rules for PCB/packaging layout. Simbeor THz 2021 has been used for all computations.

Simple 90-degree turns in a strip line usually have small excessive capacitance. As was shown in [1], anything that reduces this capacitance while not increasing the inductance should work. The following PCB stackup and materials are used for this investigation

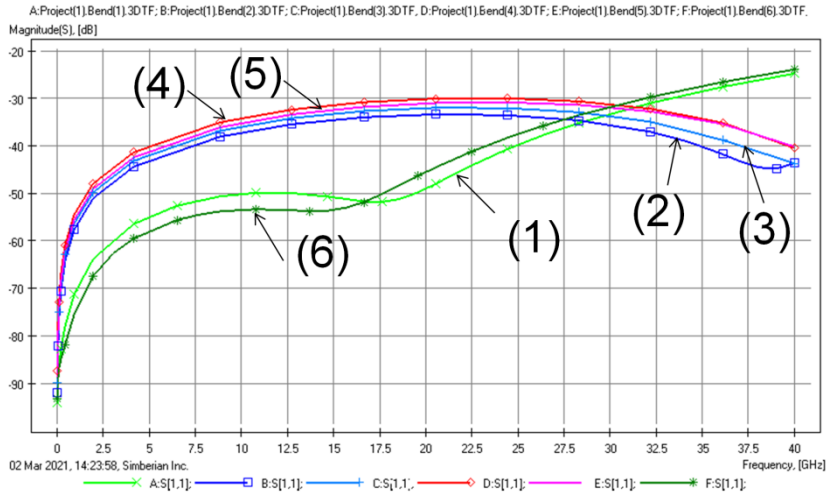


Traces are 8-mil wide – that is about 50 Ohm at 1 GHz. They are intentionally wider than usual – bends in wider traces are usually more reflective. There are multiple ways for cutting the excessive bend capacitance. Here are 6 possible ways to do it

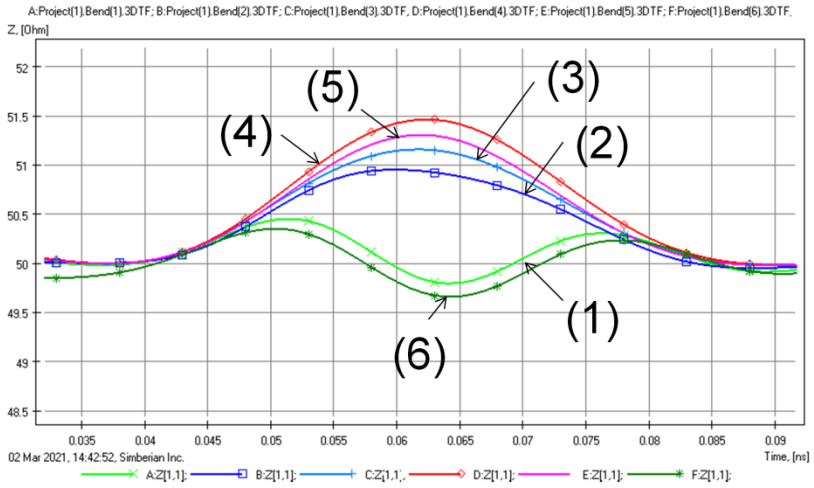


Case (1) is simply rounded bend – no optimization. Case (2) is arched turn – no optimization either. Cases (3),(4) and (6) are optimized rectangular cuts and case (5) is chamfered optimized bend.

Reflection parameters for all configurations are shown below

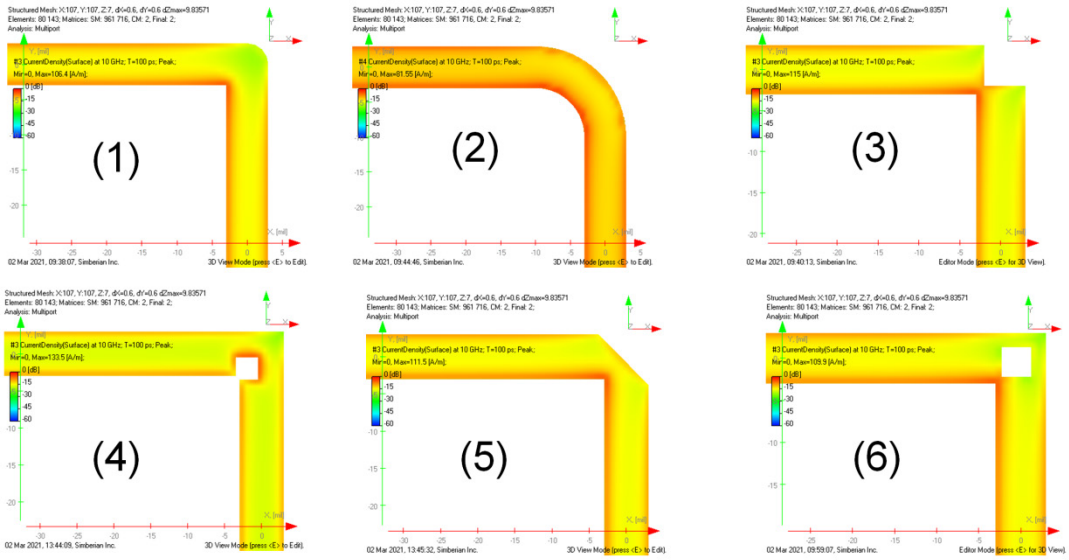


It is rather difficult to say which one is better – four configurations have reflection below -30 dB and two below -25 dB. Both numbers are difficult to measure accurately on PCBs and de-embedding does not work at this level of reflection due to variations in test fixtures. Comparison of TDR with 16 ps 10-90 rise time is shown next



We can see that configurations (1) and (6) are slightly capacitive and the other configurations are inductive. Case (4) with the internal corner cut shows the largest impedance increase. However, it may work up to higher frequencies.

Finally, it is always interesting to look at the currents at the bends. Below are plots for surface current density at 10 GHz in dB (normalized to maximal value) computed with Simbeor 3DTF solver



Ports are terminated with 50 Ohm resistors and excitation is 1 V source in series with 50 Ohm resistor from the left side.

This article shows how to use electromagnetic simulation for investigation of possible design decisions. Some “crazy” ideas can be quickly investigated. Single bend is usually not a problem for PCB traces. However, if bends are placed at a half wavelength distance, it creates resonances as shown in [1] and the resonances should be avoided by any means.

1. Minimal-reflection bends in micro-strip lines, Simberian App. Note #2008_05 available at https://www.simberian.com/AppNotes.php