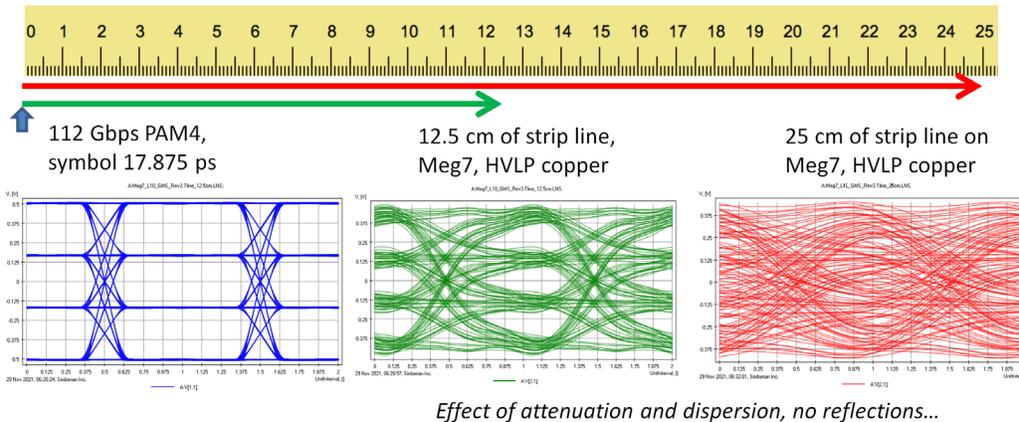


How Interconnects Work: Absorption, Dissipation and Dispersion

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Impact of Dielectrics and Conductors



Simberian booth at the last “normal” DesignCon 2020 was next to a booth with very loud demonstration equipment for 112 Gbps transfer over a distance about 1 meter through a bunch of cables. I do not know how many terabytes of data they transferred (wasted, ha-ha) during the DesignCon, but the demonstration equipment was very noisy due to the industrial cooling equipment. One can literally feel the heat coming out of it and, apparently, the devices were just transferring the data and doing nothing else. So, I start wondering how much energy is required to transmit the data and why so much power is dissipated into heat.

First, let’s start from simple evaluation of energy absorbed (or dissipated) by copper interconnects. Power delivered to 100 Ohm differential transmission line with 1V signal amplitude is 10 mW. It doubles to 20 mW if the transmitter back termination resistor is taken into account. Let’s assume that the link is ideally designed - no reflections and coupling (such links can be designed indeed). The remaining signal degradation factor is the absorption or dissipation – losses in conductors and dielectrics and dispersion related to it. So, if the link insertion loss due to absorption at the Nyquist frequency (half of bit rate for NRZ signal) is -20dB, we have got only 0.1 mW at the receiver end (0.1 V, 100 Ohm). Note that receivers on some expensive components allow -30 dB (0.032V, 10 uW) and even -40 dB (0.01V, 1uW) loss at the Nyquist frequency. Actually, it does not matter for our evaluation, because of signal at the receiver end is also converted into the heat at the termination resistor. **It basically means that all signal energy is converted to the heat!** For 50 Gbps NRZ signal with 20 ps bit time, the energy converted into the heat in differential link with termination resistors is about 0.4 pJ/bit (product of power and bit time). **This is practically immutable bottom level – we cannot reduce the energy per bit in the copper interconnects under the assumptions provided above (1 V, 100 Ohm).** 20 mW of power or 0.4 pJ/bit for 50 Gbps NRZ signal – is it small or not? It would take almost 929 hours to boil one cup of water (heat 200g of water from 20 to 100 deg. C). Looks like not much. Though, this is just one link and internet routers or switches may have over a thousand of such links – that is enough to have a cup of tea about 1 hour. It is still not impressive (if my math is correct – I am not an accountant after all, ha-ha). But, this is not the end of the story. **The actual cost of a bit transfer on PCB for 50 Gbps is at least order of magnitude larger – it is about 5 pJ/bit (or 250 mW) for 50 Gbps NRZ [Stauffer,2014].** With a thousand

of links this is enough to prepare a cup of tea in 5 min! And about 90% of this energy is dissipated by the IOs on chip. Does it explain the industrial cooling equipment for 112 Gbps links? I have not seen the power consumption data for 112 Gbps or the upcoming 224 Gbps links (ping me if you do have it). But, following the recent trends (doubling data rate increases required power by 30%) it should be about 6.5 pJ/bit (325 mW) for 112 Gbps and 8.45 pJ/bit (422 mW) for 224 Gbps. The number of IOs does not increase at the same time – that may be the clue. Also, the prototype equipment may be much less efficient. On the bright or cool side, some recent developments in this area promise to reduce the numbers to about 2 pJ/bit or 100 mW [Razavi, 2021]. **Why do we need so much power? – To mitigate the signal degradation in interconnects between the driver and receiver.** Transmitters and receivers are not 2-transistor devices in serial interconnects – they contain hundreds (may be even thousands) of transistors and most of the energy is spent to generate and restore the signal. **Can we reduce the power by design of interconnects? The answer is absolutely yes, by reducing the signal degradation in interconnects!** In general, more power and more expensive components is required for interconnects with larger losses or overall signal distortion and lower power is needed for interconnects with smaller losses and distortions.

At the recent tutorial at DesignCon 2020 [1] we have discussed the major signal degradation factors and how to reduce them or design “transparent” or “clean” interconnects. The degradation factors can be broken into three categories: (1) absorption or dissipation by conductors and dielectrics and dispersion related to that, (2) reflections, and (3) coupling. We called the first category “thermal losses”, because of the signal energy is literally heating the interconnect materials. Though, may be absorption or dissipation losses are better terms and this article is about it. When doing interconnect modeling, the following questions should be answered: What effects are important at a particular data rate? Are they accounted for by signal integrity software? If all effects are included, will model correlate with measurements?

Dielectrics

- Electric polarization dominates
- Small number of free charges $\sim 10^{10}$ to $\sim 10^{16}$ 1/m³
- Small bulk conductivity $\sim 10^{-9}$ to $\sim 10^{-17}$ 1/Ohm*m (large resistivity)
- Conductivity increases with the temperature

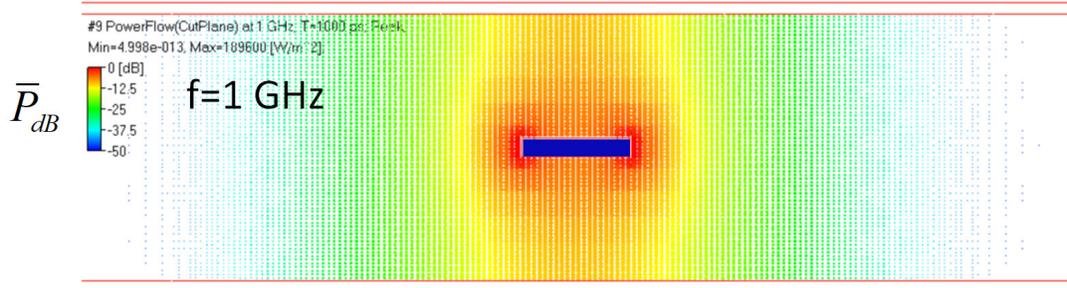
C.A. Balanis, *Advanced engineering electromagnetics*, 2012
I. S Rez, Y.M. Paplavko, *Dielectrics (in Russian)*, 1989

Semi-metals Semiconductors

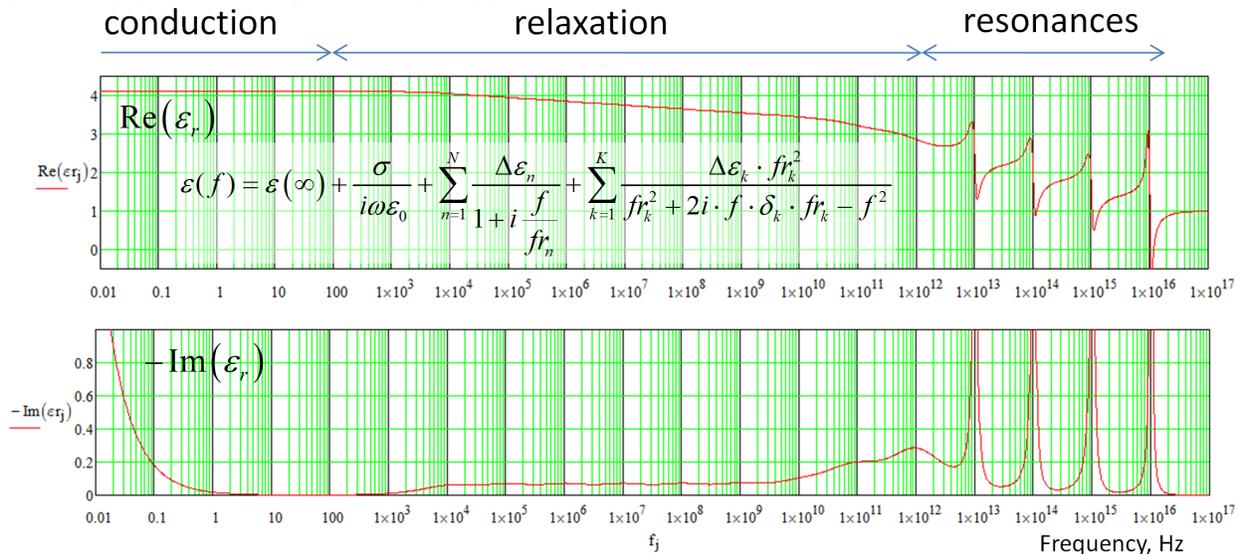
Conductors

- Almost no electric polarization up to $\sim 10^{16}$ Hz (shielding)
- Large number of free charges $\sim 10^{27}$ to $\sim 10^{29}$ 1/m³
- Large bulk conductivity $\sim 10^6$ to $\sim 10^8$ 1/Ohm*m (small resistivity)
- Conductivity decreases with the temperature

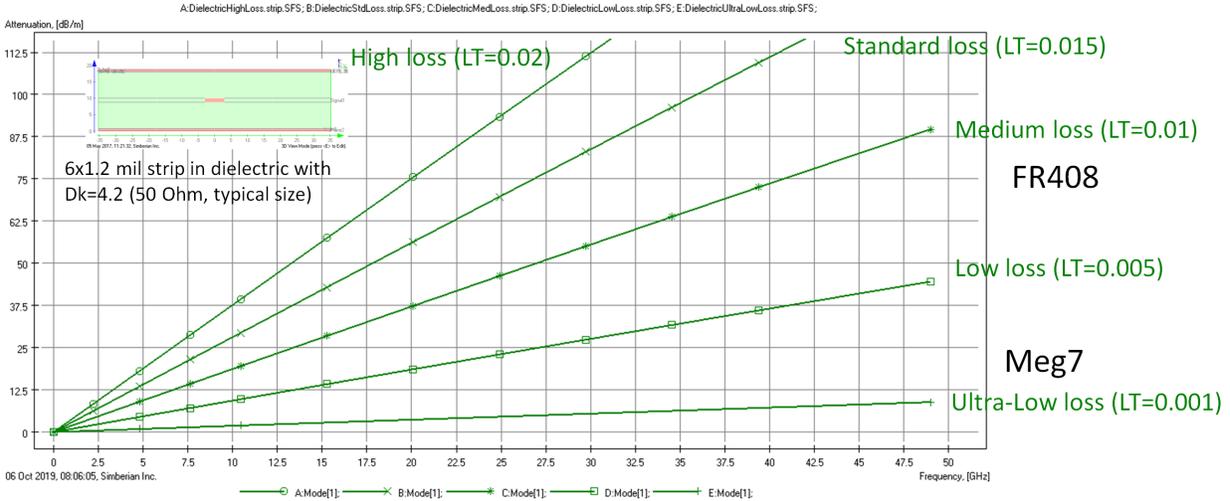
Let’s start with the energy absorbed (or dissipated) by dielectrics and dispersion related to it. Why dielectric matter anyway? **Because of the signal energy propagates along the PCB and packaging interconnects mostly in dielectrics around the signal conductors.** The signal energy location can be illustrated with the peak power flow density (vector product of electric and magnetic field) for a typical PCB stripline interconnect shown below (strip 1.2 mil thick, 7 mil wide, DK=3.76, LT = 0.006 @ 1 GHz, planes 0.77 mil thick, 17.2 mil apart, color scale is used to plot peak power flow density (PFD) in W/m² (shown in dB), computed with Simbeor THz):



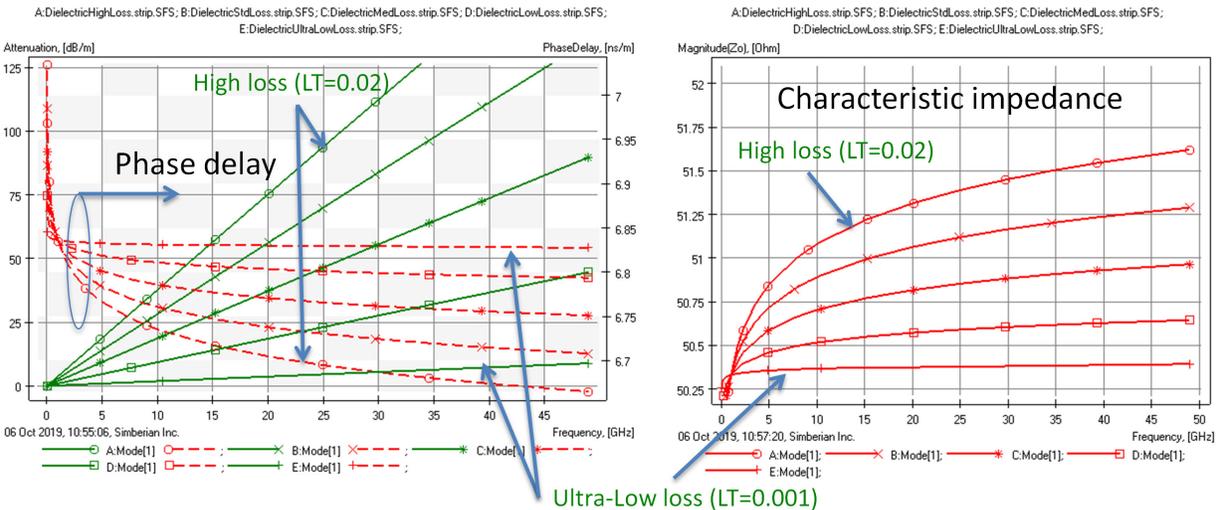
We can see that the signal energy concentrates near the strip edges and between the strip and planes in dielectric. PDF is directed along the conductors into the picture. There is actually no power moving in the direction of the signal within the conductors. **All dielectrics absorb or dissipate the energy – it is important to understand it (was subject of another tutorial [2] from DesignCon 2016).** In general, dielectric properties can be described with the permittivity that is a complex function of frequency (always for real materials!). We call the real part of permittivity as dielectric constant (Dk). Ratio of the negative imaginary part of permittivity to real part is called loss tangent (LT) or dissipation factor (DF). It describes the power loss to heat and dispersion. A universal dielectric model may look as follows (real part is top graph and negative imaginary part is the bottom):



The model is actually real up to 50 GHz (constructed on the base of measured data by fitting) and guessed above it – this is just to show different mechanisms contributing to the losses in dielectrics (imaginary part of permittivity) and dispersion. The conduction losses for PCB and packaging dielectrics are negligibly small – they are responsible for the increase of imaginary part below 100 Hz (this is not a typo). At frequency up to 1 THz we are dealing with the relaxation losses related to electronic polarization of atoms (RC type of circuit – no oscillations). That is modeled as either multipole Debye or wideband Debye models [2]. **That also means that the Dk can only decrease with the frequency at these frequencies.** We are dealing with composite solids here – mostly polymers. Lorentzian terms (oscillating RLC type of circuit) are added for illustrative purpose, to show that the resonant properties of the solid PCB materials are important over 1 THz where Dk may go down because of the resonances. At “normal” frequencies up to 100 GHz dielectric polarization losses can be accurately simulated with the pole-continuous or wideband Debye models. Attenuation per meter for some PCB materials and typical stripline is computed and next (approximately linear dB/length growth with frequency):



As we can see the dielectric choice may have the most profound consequences on the link performance. For 112 Gbps PAM4 link the losses per meter at Nyquist frequency 28 GHz (quarter of bit rate or half of baud rate) may range from 5.1 dB/m for the ultra-low loss dielectric to over 100 dB/m (practically complete loss of signal) for the regular FR-4 type high loss dielectrics. **Note that the ultra-low loss dielectric with LT=0.001 is still much more lossy than dielectrics used in cables.** This is important to know when you make decision on switching from PCB to cables – there are many ways to reduce the losses on PCB interconnects. Causal wideband Debye model is used here [2]. It can be defined with Dk and LT at one frequency point – 1 GHz in this case. The model analytically defines dielectric constant and loss tangent dispersion from 0 up to 100 GHz. The model is causal and includes the dispersion (change with frequency) of the phase delay and characteristic impedance as illustrated below:

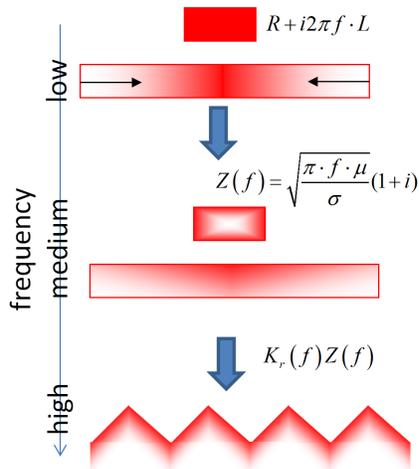


Phase delays are plotted on the left graph on the right axis in ns/m. Characteristic impedances are shown on the right plot in Ohm. This simple numerical experiment demonstrates that not only the frequency-dependent losses are included in the model, but it also captures the dispersion of phase delay and characteristic impedance. The model is not causal if it does not include such dispersion. It also demonstrates that dielectrics with high losses (typical FR-4) have much higher dispersion comparing to

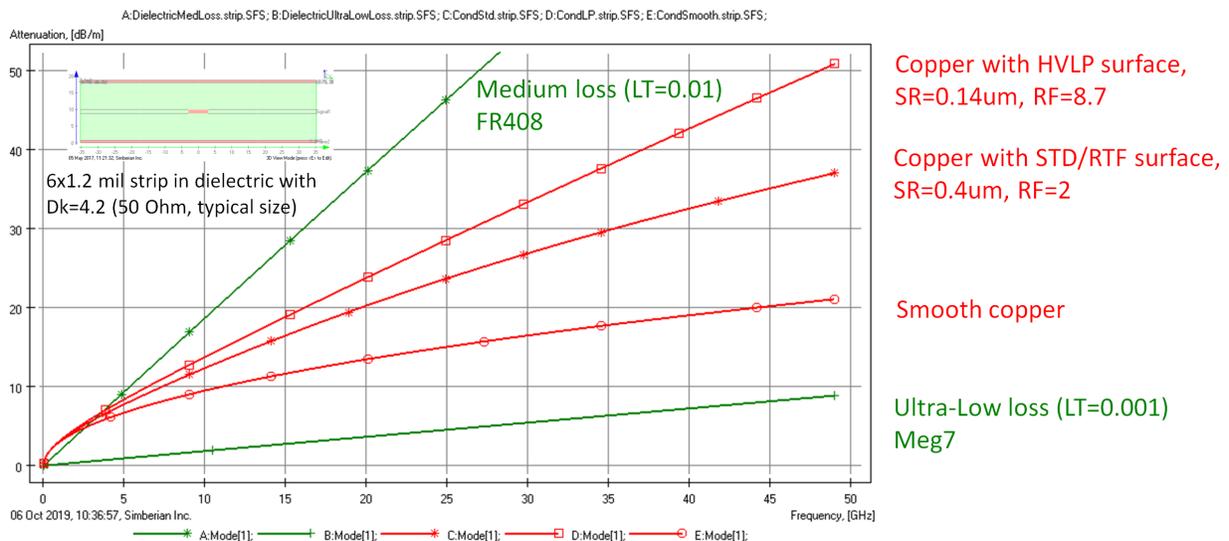
the ultra-low loss dielectrics that do not show much dispersion at the frequencies important for analysis of multi-gigabit interconnects. **Not only the frequency-dependent losses, but also phase dispersion cause signal degradation.** Signal harmonics are attenuated more at high frequencies and travel with different velocity as well.

Considering the conductor losses, the subject was extensively covered in the tutorial [2] and another “How Interconnects Work...” paper [3]. In general, the conductor absorption and dispersion effects can be summarized and illustrated as follows:

- Current crowding below strips
 - Around 10-100 KHz
 - Increases R and decreases L at very low frequencies
- Skin-effect
 - Transition frequencies from 1 MHz to 100 GHz (see chart)
 - Surface impedance boundary conditions (SIBC) for well-developed skin-effect – R and L ~ sqrt(frequency)
- Skin-effect on rough surface
 - May be comparable with skin depth starting from 10 MHz
 - Increases both R and L (and possibly C)
- Ferromagnetic resonances from 2 to 3 GHz (Nickel)
- Plasmonic effects above 1 THz – (Drude model)

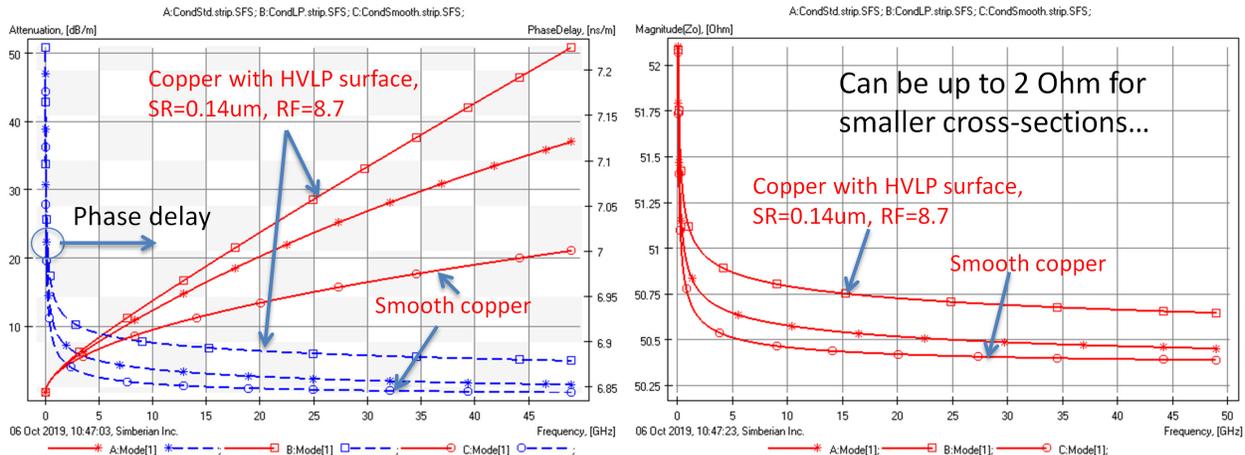


Though, the currents in the conductors flow along the signal propagation direction (and back), the power flow vectors within the conductor always point almost exactly perpendicular to the conductor surface. **Conductors literally absorb or “suck” the energy of the signal and convert it into the heat.** Though, conductors are indispensable part of PCB interconnects (no viable alternatives so far), but there are additional unavoidable losses and dispersion related to them. As in case of dielectrics, the absorption can be illustrated with the losses per meter as shown next:



Dielectric losses for the medium and ultra-low losses are plotted on the same graph as green curves for the comparison. Three red curves are computed for strip width 6 mil (about 0.15 mm) – with smooth

copper (no roughness), with STD or reverse treated copper (middle curve) and with HVLP copper roughness. Parameters for the roughness models are taken from validation projects and were identified with the measurements. We can see that even with smooth copper the conductor losses may exceed the dielectric losses for the ultra-low loss dielectric (valid for a particular cross-section). **It means that the minimal possible losses on PCB are limited mostly by the copper and copper roughness!** To have the losses on PCB closer to cables over similar bandwidth, larger smooth strips must be used (it reduces current density and overall losses). Due to the causality requirements, the conductor losses cause dispersion of the phase delay and characteristic impedance as illustrated next:



Again, if a model does not have dependency of phase delay and impedance from the roughness model parameters, such model is not causal and, thus, may be not accurate enough. Always do the numerical experiments like that, to see what is in the model. See more on the inductive effect of roughness in [3] and [4].

Now, what about the predictability of the absorption or dissipation losses and dispersion? In other words, how to build models that correlate with the measurements? It depends on availability of the frequency-continuous ultra-broadband models for dielectric and conductor roughness. As was demonstrated in [2], dielectric data from laminate manufacturers can be used to construct such models with sufficient accuracy for preliminary analysis or lower data rates (can be defined with numerical experiment). **Dielectric models for higher data rates and for better accuracy must be identified. Parameters for conductor roughness models are usually not available and must be always identified.** Identification with GMS-parameters [5] or SPP Light [6] techniques with separation of dielectric and conductor losses can be used to build dielectric and conductor roughness models. See more on the material model identification automation with Simbeor SDK at [7] and [8].

Finally, here is how to reduce the signal degradation due to the absorption or dissipation losses:

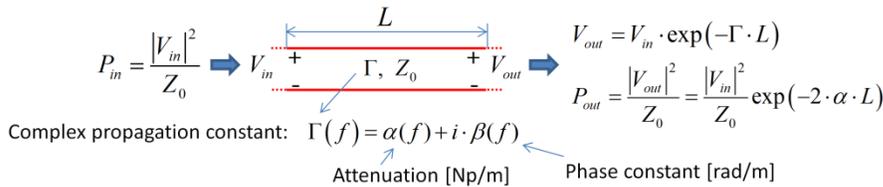
- Use dielectrics with lower Dk and LT (no brainer);
- Use more metal to reduce current density – wider interconnect traces absorb less energy (subject to single mode propagation limit);
- Use conductors without roughness or “engineered” rough surfaces without additional losses;

Energy of generated signals is always turned into heat – in conductors, dielectrics or termination resistors – no matter what we do with the interconnect losses. **However, interconnects with the lower losses reduce the energy required for the signal conditioning and restoration. This is valid under one**

important condition – very low reflections and no coupling. Those two signal degradation factors will be discussed in the next “How interconnects work...” articles.

Appendix:

Interconnect Attenuation and Loss



Power Loss [dB]:

$$10 \cdot \log\left(\frac{P_{in}}{P_{out}}\right) = 10 \cdot \log(\exp(2 \cdot \alpha \cdot L)) = 20 \cdot \log(e) \cdot \alpha \cdot L = \alpha_{dB} \cdot L$$

Attenuation [dB/m]: $\alpha_{dB} = 20 \cdot \log(e) \cdot \alpha \approx 8.686 \cdot \alpha$

Simplified derivation, no reflection losses

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