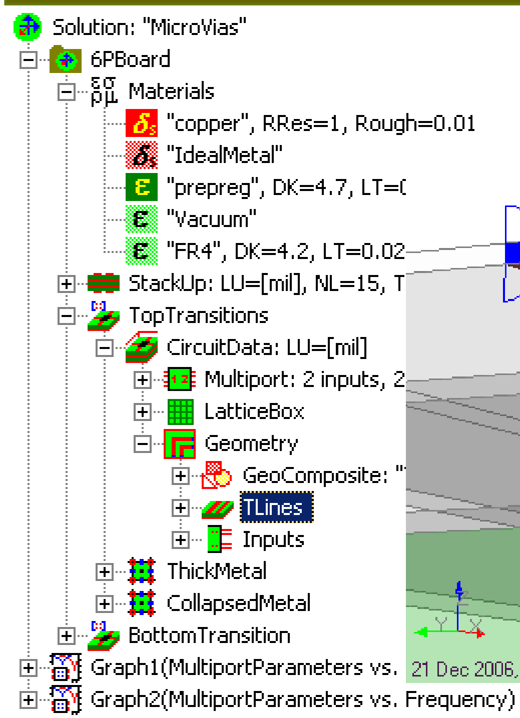
Simberian
Electromagnetic Solutions

Electromagnetic Analysis of Decoupling Capacitor Mounting Structures with Simbeor



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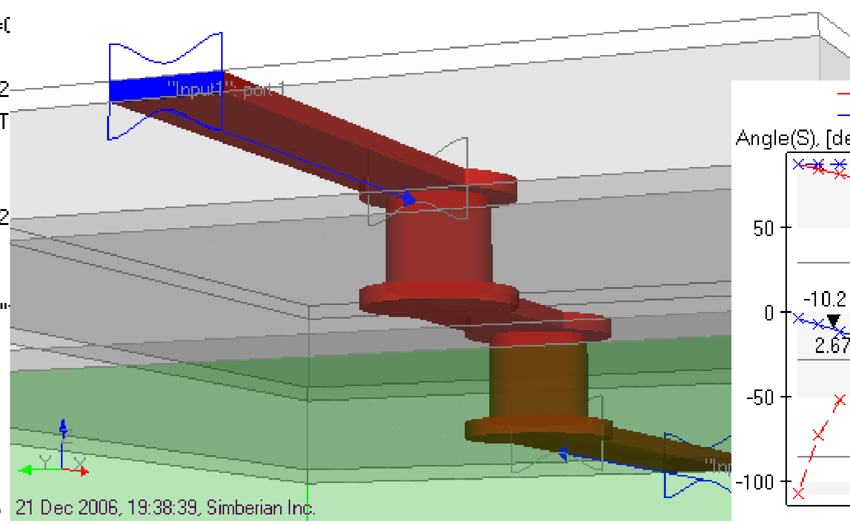

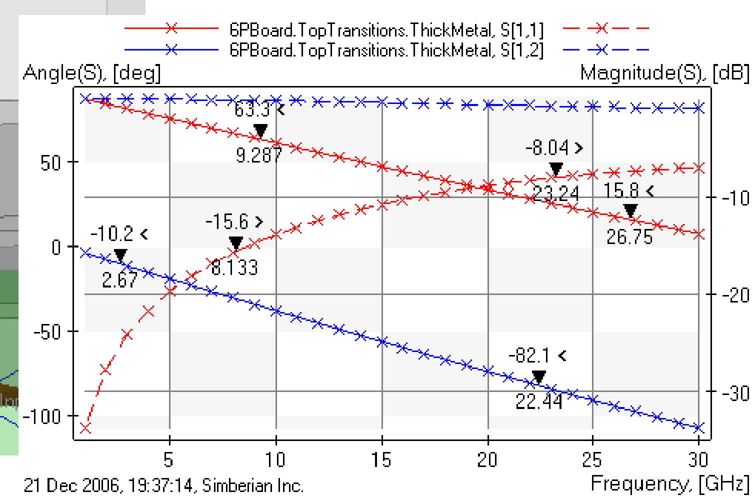

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Overview

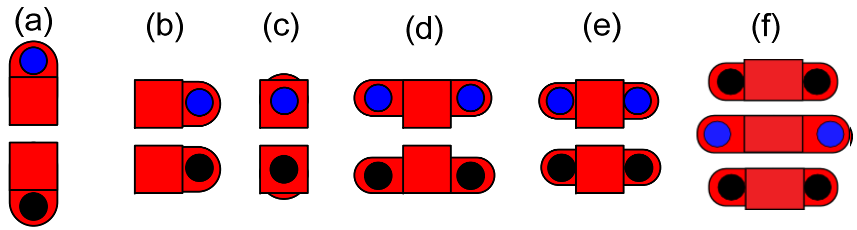
- Introduction
- Investigation of decoupling capacitors mounting structures with plane pair next to the board surface
  - Decomposition
  - Minimal possible inductance investigation
  - Models for mounting structures with 2, 4 and 6 via-holes
- Investigation of mounting structures with plane pair separated from board surface by signal and plane layers
- Conclusion

Introduction

- Power distribution networks (PDN) are usually designed as parallel metal planes with decoupling capacitors connected to them
  - Analysis of the planes is a 2-D problem that can be formulated as 2-D Telegrapher's or Helmholtz's equations (*)
  - There are multiple algorithms and solvers based on 2-D solutions with simplified models for the decoupling capacitors mounting structures
  - Accurate analysis of the decoupling capacitor mounting structure may require a 3-D full-wave analysis
- This example demonstrates how to build 3D full-wave models for the decoupling capacitor mounting structures and how to characterize the mounting inductance
- Simbeor 2007 electromagnetic solver for multilayered circuits is used to generate the results

(*) See the broadband formulation in Y. Shlepnev, Transmission plane models for parallel-plane power distribution system and signal integrity analysis, -22nd Annual Review of Progress in Applied Computational Electromagnetics, 2006, p. 382-389.

Mounting structures to be investigated

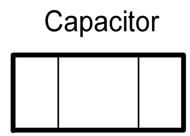


6 different configurations with diameter of vias 12 mil and 20 mil anti-pads:

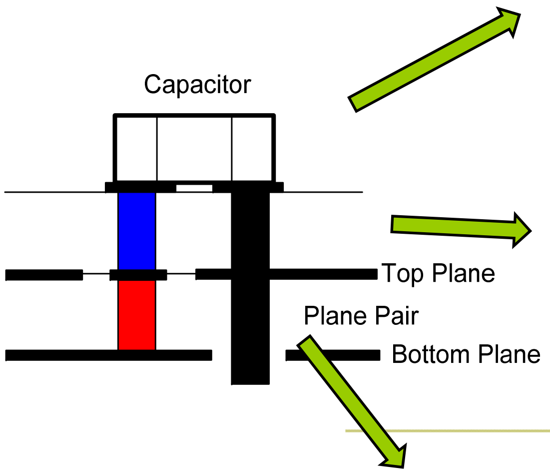
a) 2 vias 60 mil apart with pads for 0402 caps
b) 2 vias 40 mil apart with pads for 0402 caps
c) 2 vias in pads (40 mil apart) for 0402 caps
d) 4 vias with 40 mil pitch with pads for 0402 caps
e) 4 vias with 32 mil pitch with pads for 0402 caps
f) 6 vias with near-circular pattern recommended for 0603 X2Y caps

De-composition of 2-via structure with plane pair close to the board surface

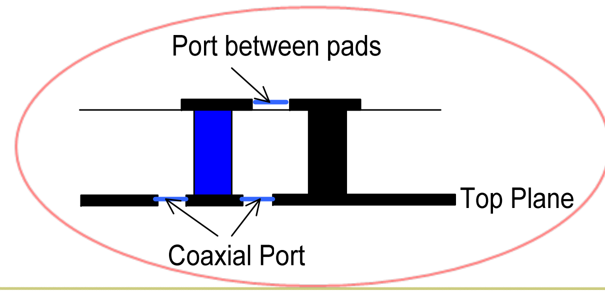
We are going to investigate and build model only for the capacitor mounting structure

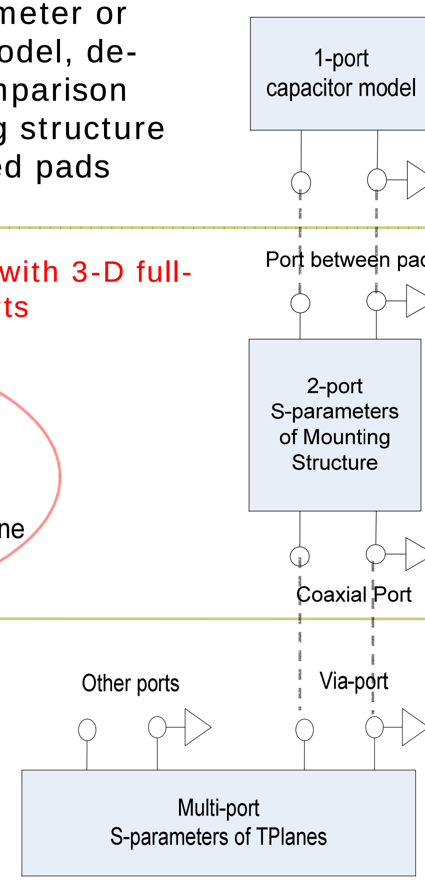


Measured S-parameter or equivalent RLC model, de-embedded by comparison with the mounting structure with short circuited pads



Capacitor mounting structure simulated with 3-D full-wave solver with coaxial and lumped ports

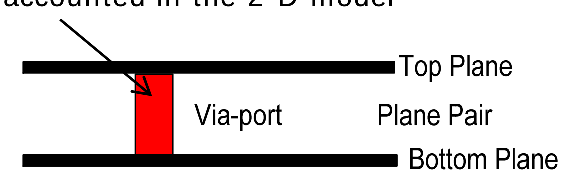




Transmission plane structure

$$\left.\begin{aligned}
&\frac{\partial J_{sx}(\omega)}{\partial x}+\frac{\partial J_{sy}(\omega)}{\partial y}=-Y_{\square}(\omega)\cdot V(\omega)+J_z(\omega)\\
&\frac{\partial V(\omega)}{\partial x}=-Z_{\square}(\omega)\cdot J_{sx}(\omega)\\
&\frac{\partial V(\omega)}{\partial y}=-Z_{\square}(\omega)\cdot J_{sy}(\omega)
\end{aligned}\right\}(x,y)\in\Omega$$

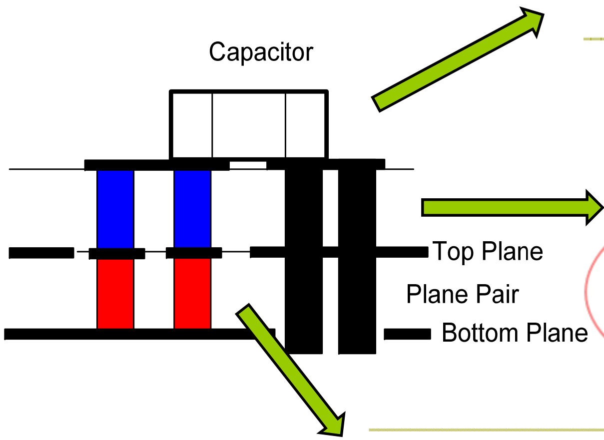
Inductance of this segment of via is accounted in the 2-D model

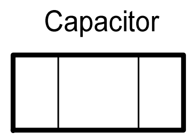


S-parameters of multiport obtained with 2-D full-wave analysis of structure with cylindrical via-ports

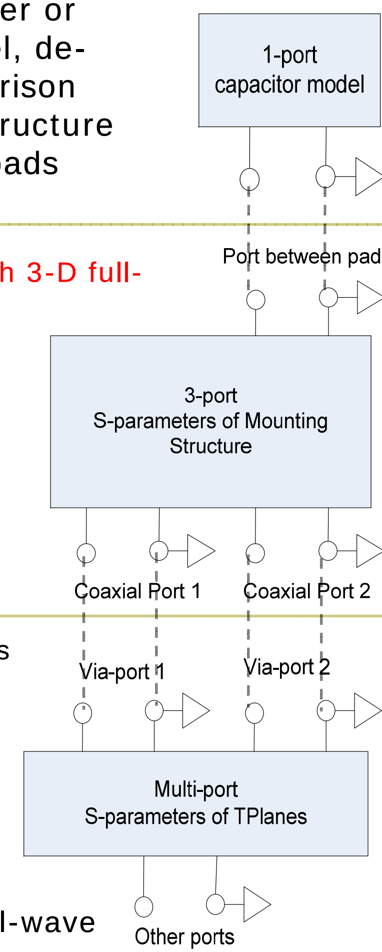
De-composition of 4-via and 6-via structures with plane pair close to the board surface

We are going to investigate and build model only for the capacitor mounting structure

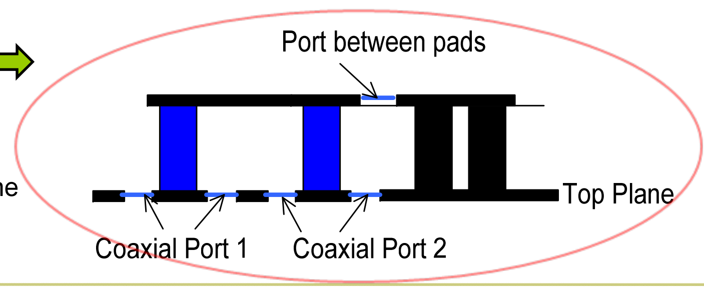




Measured S-parameter or equivalent RLC model, de-embedded by comparison with the mounting structure with short circuited pads



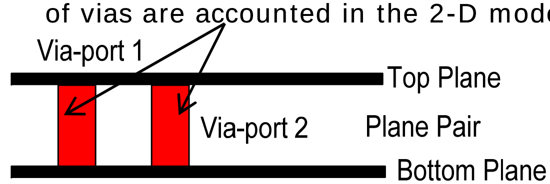
Capacitor mounting structure simulated with 3-D full-wave solver with coaxial and lumped ports



Transmission plane structure

$$
\left.
\begin{aligned}
&\frac{\partial J_{sx}(\omega)}{\partial x} + \frac{\partial J_{sy}(\omega)}{\partial y} = -Y_{\square}(\omega)\cdot V(\omega) + J_z(\omega) \\
&\frac{\partial V(\omega)}{\partial x} = -Z_{\square}(\omega)\cdot J_{sx}(\omega) \\
&\frac{\partial V(\omega)}{\partial y} = -Z_{\square}(\omega)\cdot J_{sy}(\omega)
\end{aligned}
\right\} (x,y)\in\Omega
$$

Self and mutual inductances of these segments of vias are accounted in the 2-D model

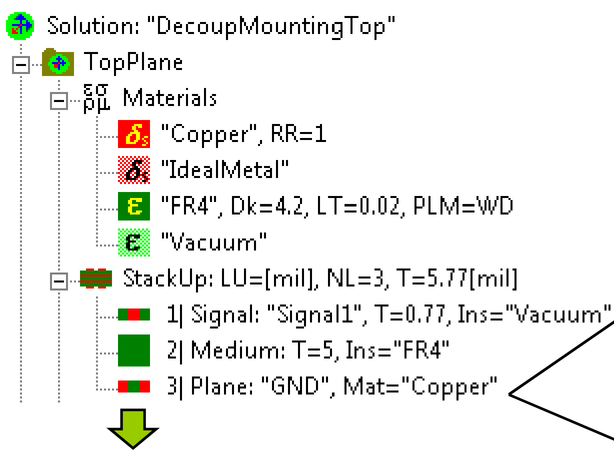


S-parameters of multiport obtained with 2-D full-wave analysis of structure with cylindrical via-ports

Minimal possible inductance investigation

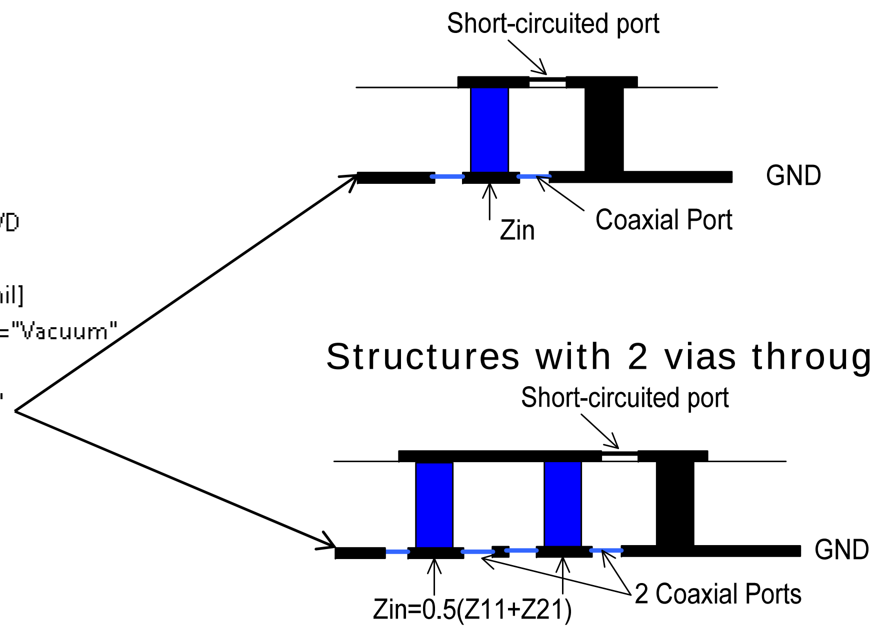
- Describe sub-stack only above the topmost plane
- Short-circuit the port connected to the capacitor with a rectangular conductive patch
- Use coaxial ports in plane and calculate Zin of the mounting structure
- Estimate equivalent effective inductance L(w)=Im(Zin)/(w), w is radial frequency – this is the simplest first-order approximation valid at lower frequencies

Materials and sub-stack:

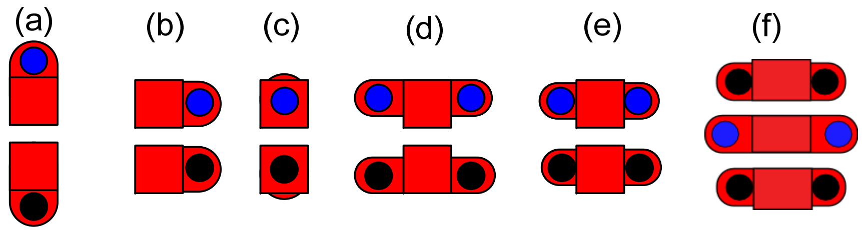


The rest of the stackup is removed for the analysis of the mounting structure

Structures with 1 via through GND plane:

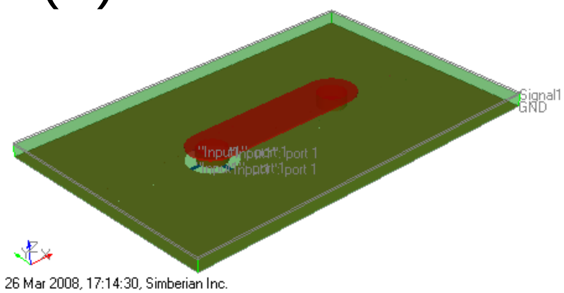


Geometries of circuits for 6 cases

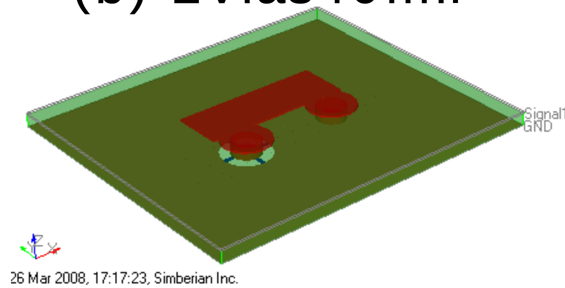


Blue vias end with coaxial ports in plane GND
Black vias connected to the plane GND

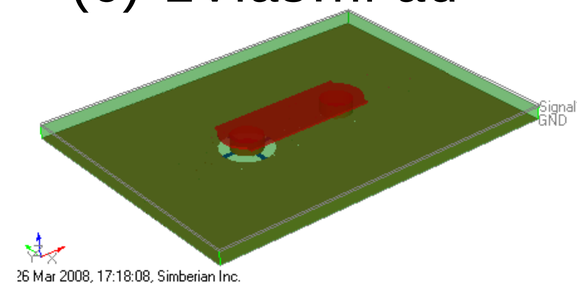
(a) 2Vias60mil



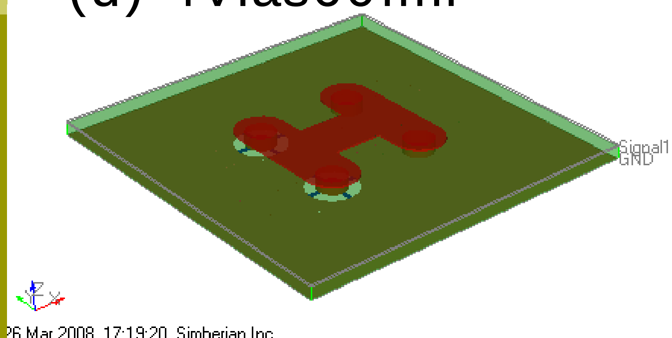
(b) 2Vias40mil



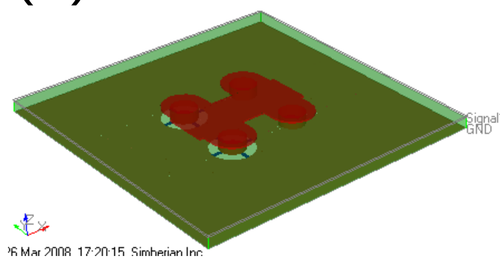
(c) 2ViasInPad



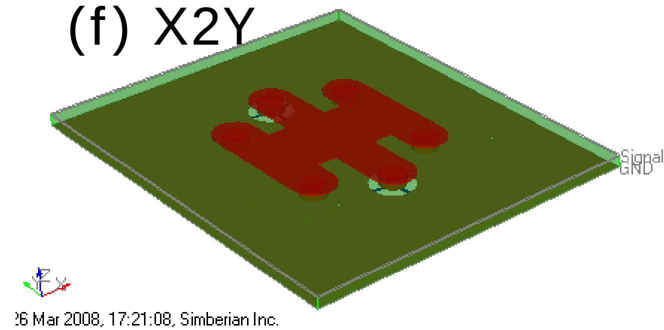
(d) 4Vias60mil



(e) 4ViasBest

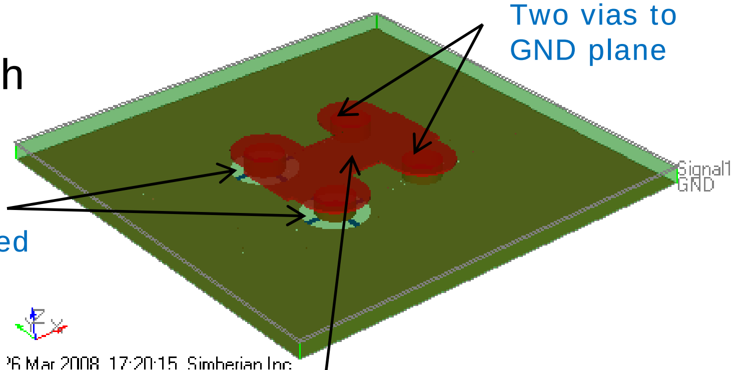


(f) X2Y



Example of geometry description for the circuit (e) 4ViasBest

Geometry created in about 5 min by drawing in 3-D geometry editor on grid with 1 mil truncation



Two vias to GND plane

Coaxial ports in the GND plane connected to two vias

- 4ViasBest
  - CircuitData: LU=[mil], Truncation=1.0[mil]
    - Multiport: 2 inputs, 2 ports
    - LatticeBox
    - Geometry
      - Composite Object, XC=0, YC=0
        - Rectangle: "Signal1", "Copper", W=40, H=20, Xmin=-20, Ymin=-10, Xmax=20, Ymax=10
        - Cylindroid: "GND" to "Signal1", "Copper", XC=-16, YC=-16, D=12
        - Cylindroid: "GND" to "Signal1", "Copper", XC=-16, YC=16, D=12
        - Cylindroid: "GND" to "Signal1", "Copper", XC=16, YC=-16, D=12
        - Cylindroid: "GND" to "Signal1", "Copper", XC=16, YC=16, D=12
        - Ellipse: "Signal1", "Copper", XC=-16, YC=-16, D=20
        - Ellipse: "Signal1", "Copper", XC=-16, YC=16, D=20
        - Ellipse: "Signal1", "Copper", XC=16, YC=-16, D=20
        - Ellipse: "Signal1", "Copper", XC=16, YC=16, D=20
        - Rectangle: "Signal1", "Copper", W=22, H=20, Xmin=-28, Ymin=-10, Xmax=-6, Ymax=10
        - Rectangle: "Signal1", "Copper", W=22, H=20, Xmin=6, Ymin=-10, Xmax=28, Ymax=10
        - Trace: "Signal1", "Copper", W=20, L=32, NV=2
        - Trace: "Signal1", "Copper", W=20, L=32, NV=2
      - TLines
      - Inputs
        - 1: "Input1", 4 Ports, ID=12, OD=20
        - 2: "Input2", 4 Ports, ID=12, OD=20

Short-circuit plate instead of capacitor

4 via-holes

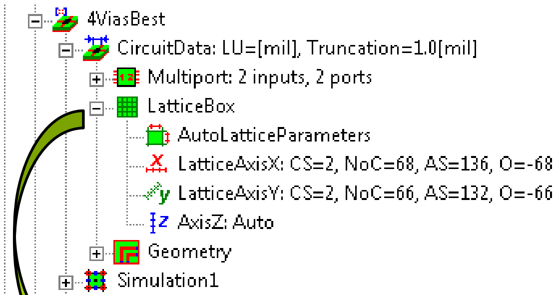
Pads for 4 via-holes in layer Signal1

Capacitor pads in layer Signal1

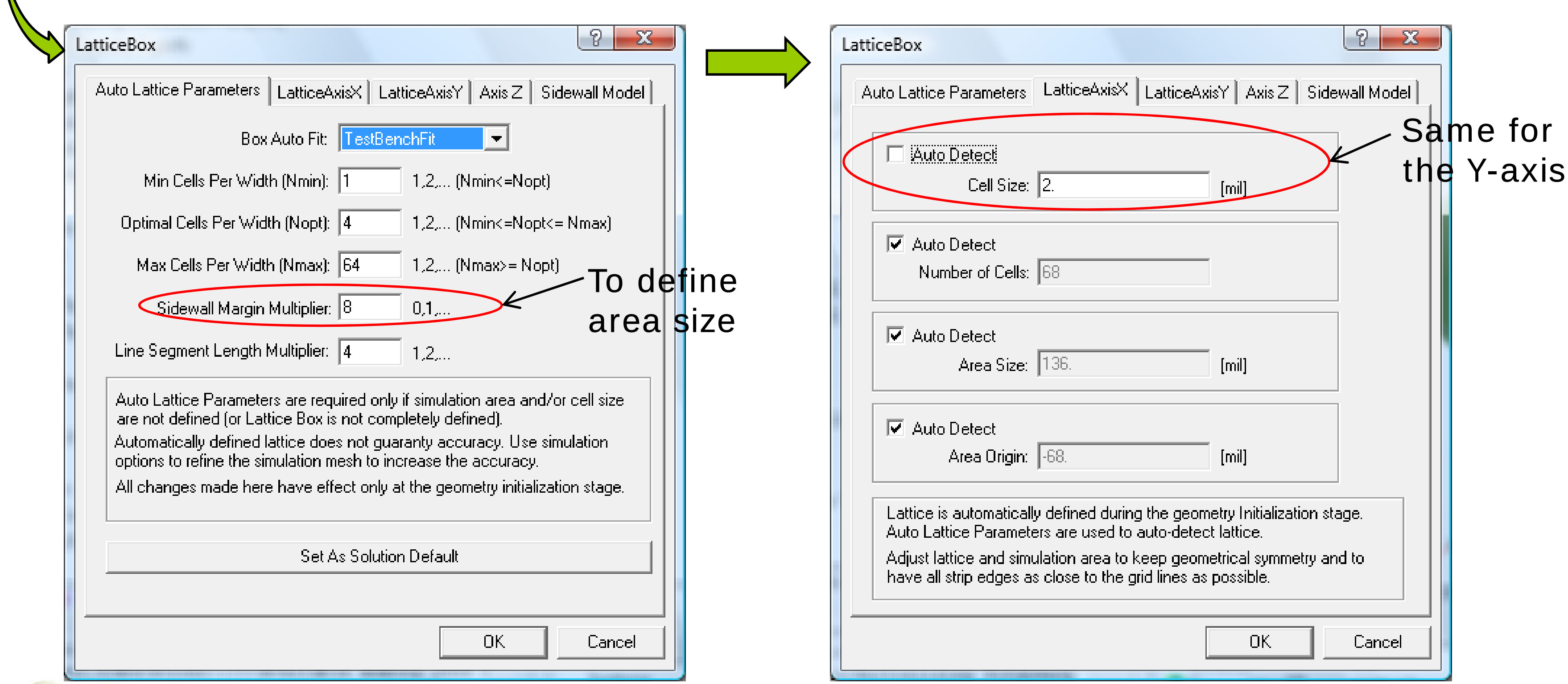
Traces connecting via-hole pads with the capacitor pads in layer Signal1

Two coaxial inputs in layer GND

Simulation area setup (for all circuits)

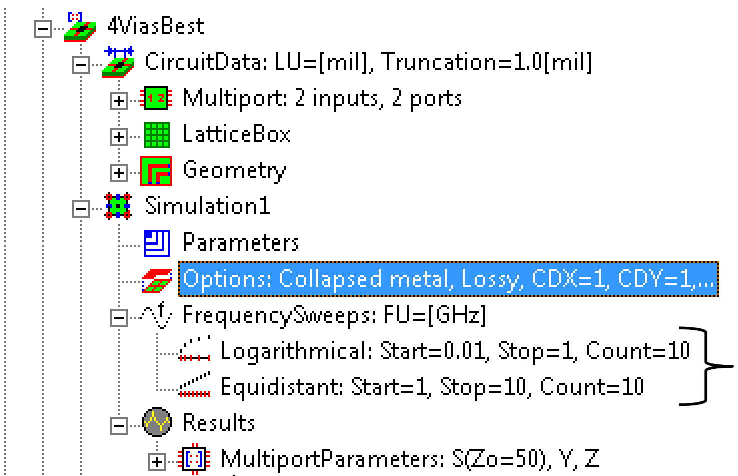


- For consistent comparison of all cases
  - Cell size fixed to 2 mil by 2 mil for X and Y axes
  - Simulation area automatically defined with Sidewall Margin Multiplier equal to 8 to have larger area size

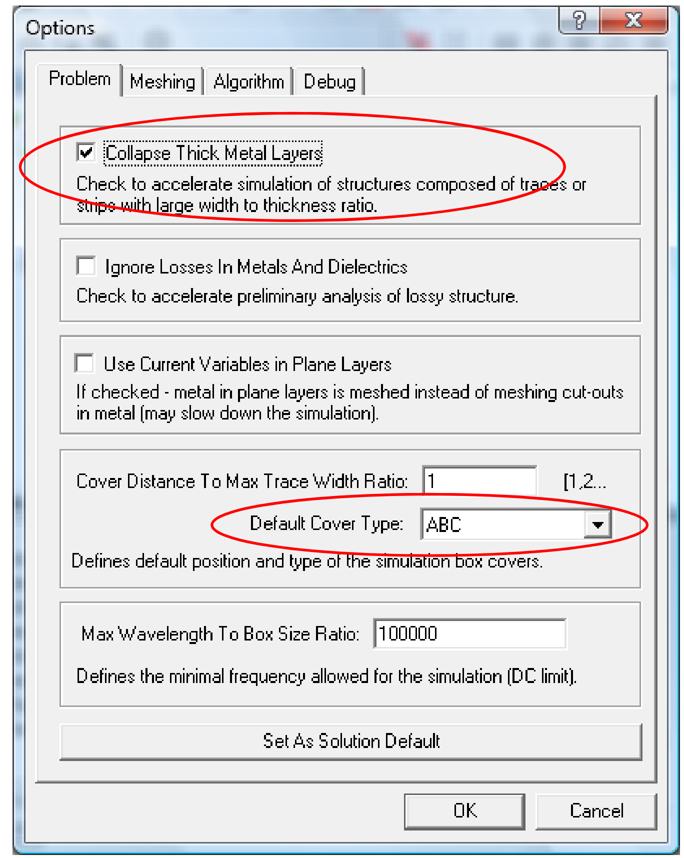


Simulation and results setup

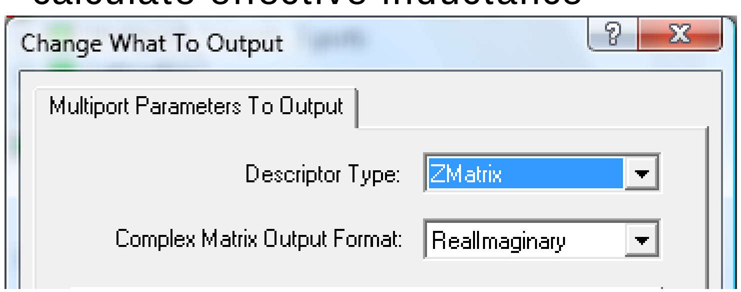
- Model with collapsed plane layers and absorbing boundary conditions above and below the circuit are used



Two frequency sweeps



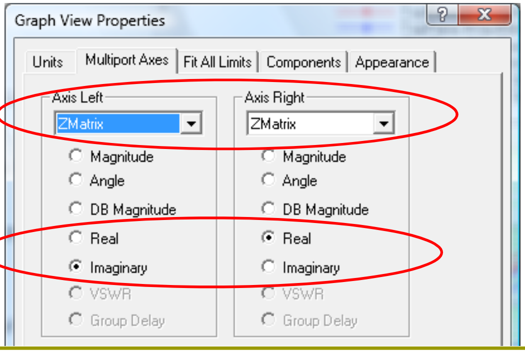
Output Z-matrix into csv-file to calculate effective inductance



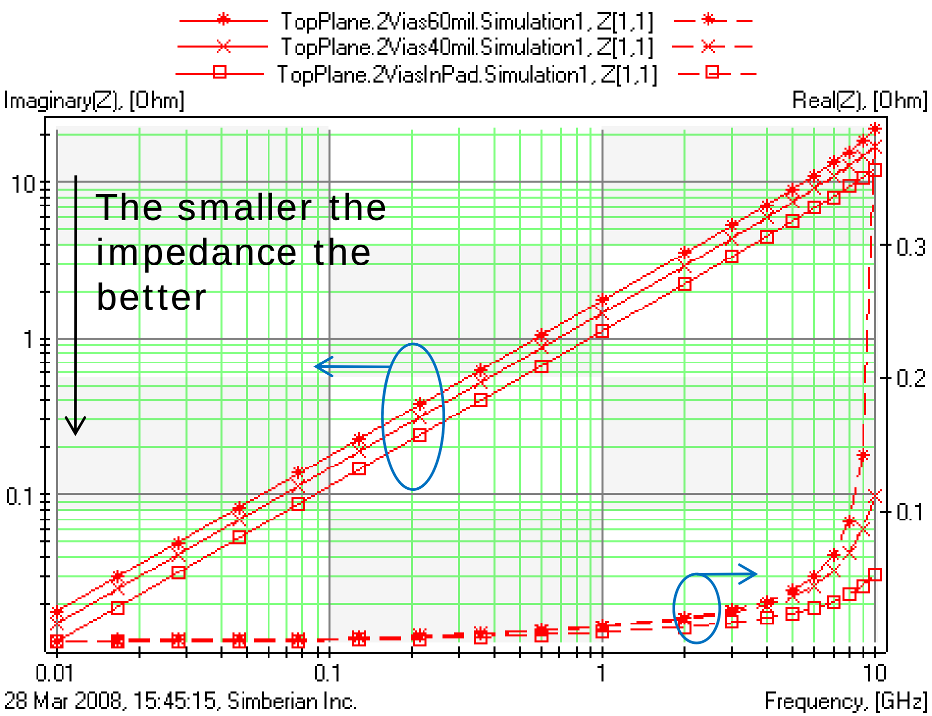
Simulation results

- Simulation takes just few seconds per frequency point at 2 GHz dual core processor

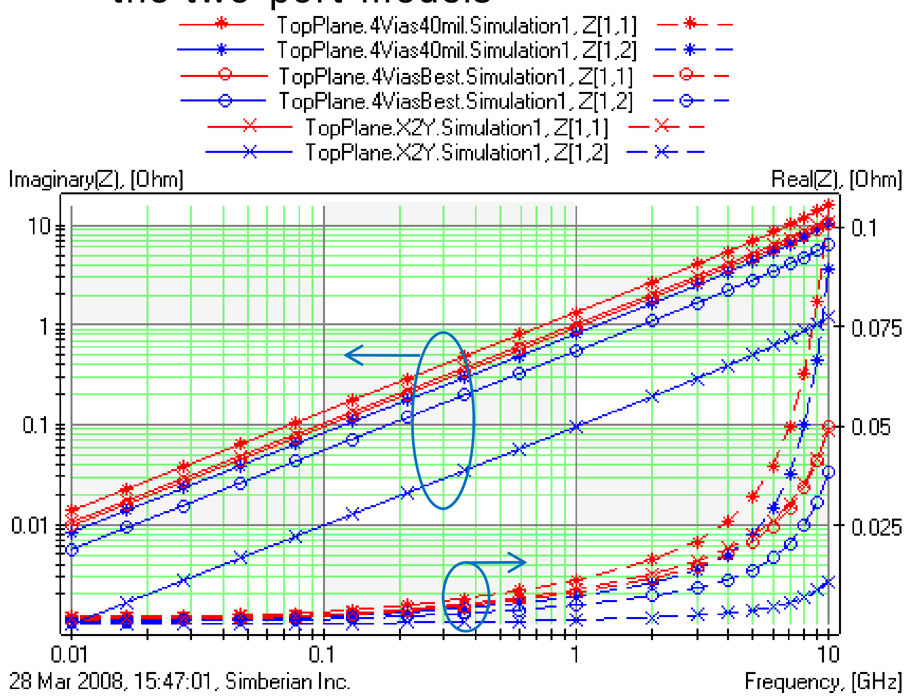
Graph properties to see Z-parameters



Z11 impedances of the one-port models

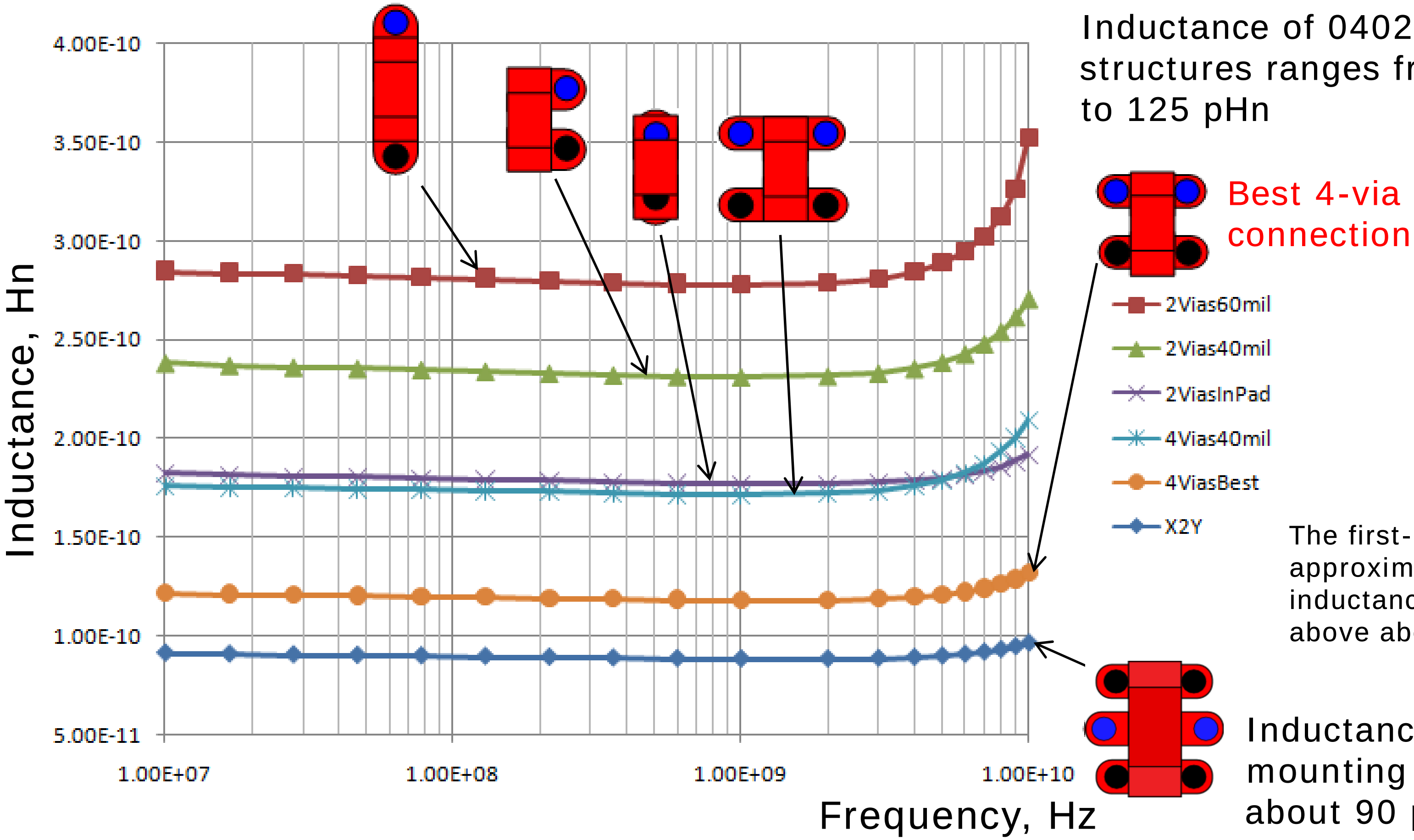


Z11 and Z12 impedances of the two-port models



Comparison of effective inductances of the mounting structures

These are the minimal possible inductances – they do not include the internal inductance of the capacitor and inductance of the via section between the planes!



Inductance of 0402 mounting structures ranges from 285 pHn to 125 pHn

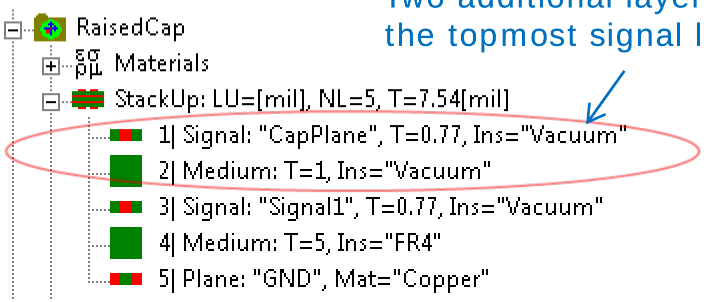
The first-order approximation by inductance is not valid above about 4 GHz

Inductance of X2Y mounting structure is about 90 pHn

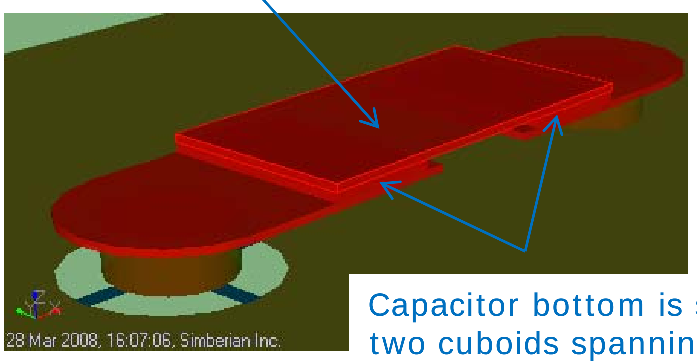
Model for a case with capacitor raised above the board surface

- More complicated models of the mounting structures can be created if necessary

Two additional layers added above the topmost signal layer

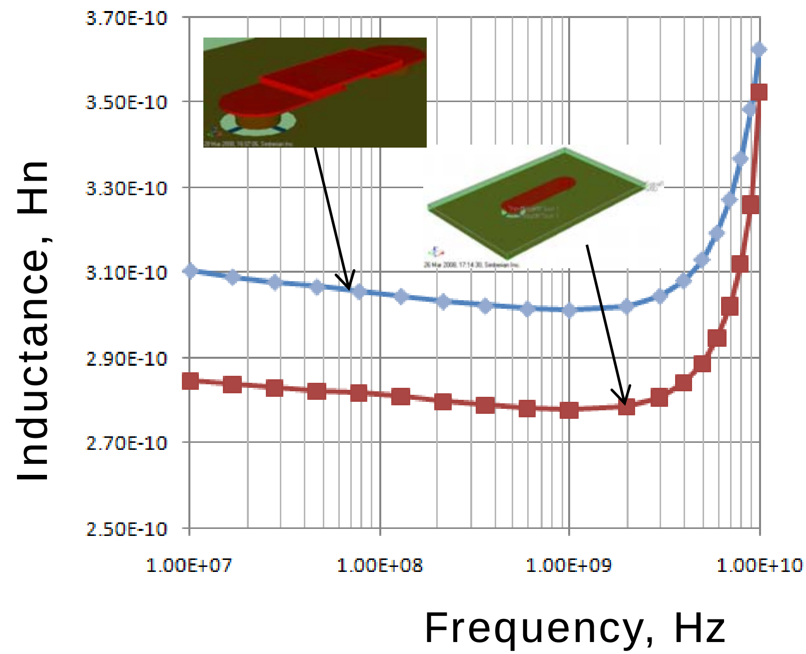


Short-circuiting plate is in layer CapPlane



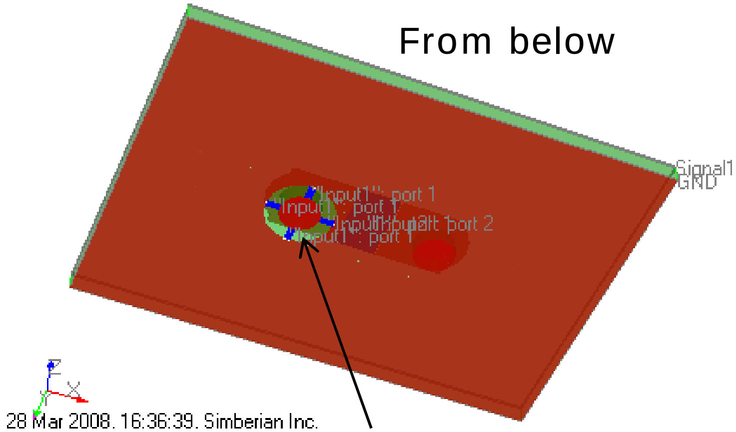
Capacitor bottom is simulated as two cuboids spanning from layer CapPlane to Signal1

With 1 mil spacing between the capacitor bottom and board surface, the inductance increases from 285 pHn to 310 pHn



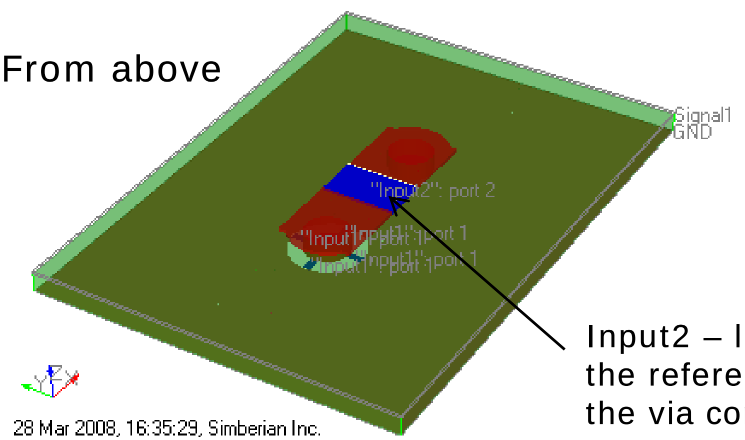
Final multiport S-parameter model of the mounting structure with vias in pads

From below

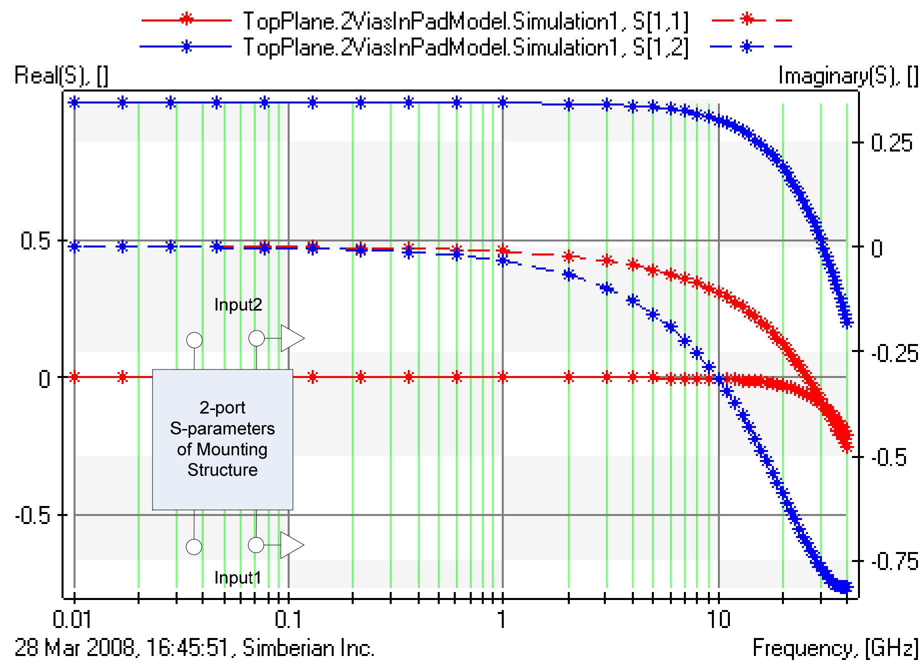


Input1 – coaxial port at the location of via-hole going through GND plane (plane is the reference side of this port)

From above

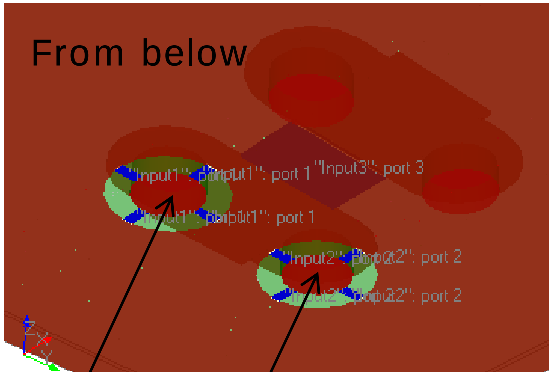


The model has to be connected with the model of a 0402 capacitor at port Input2 and with a 2-D transmission plane model at port Input1

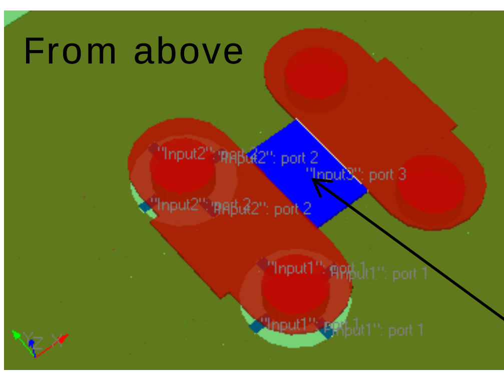


Input2 – lumped X-directed port between the pads with the reference side of the port (highlighted) connected to the via connected to GND

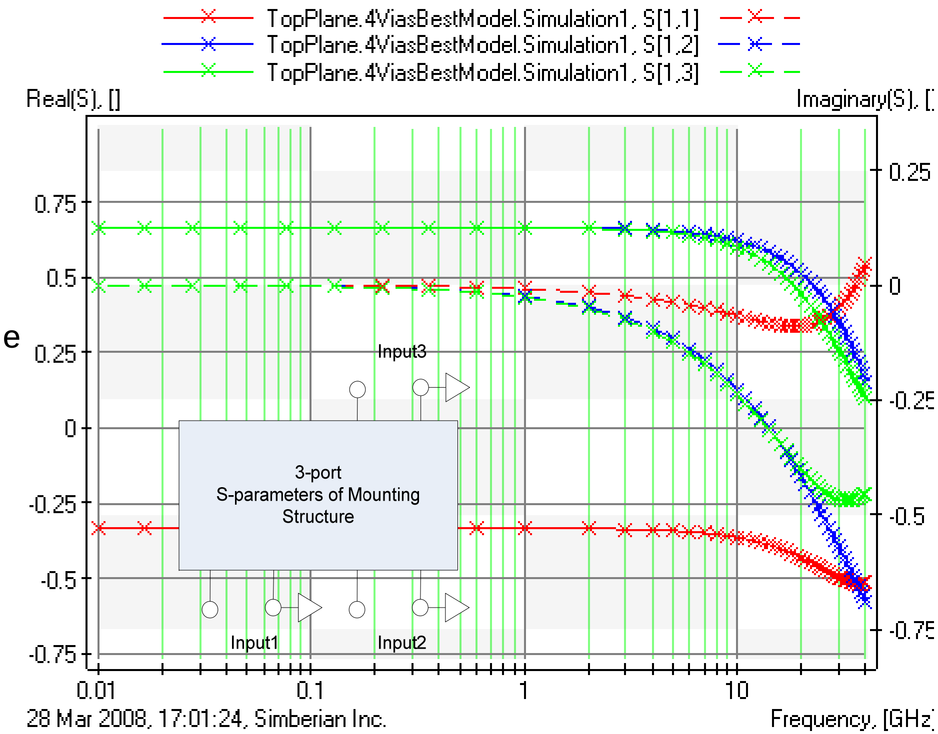
Final multiport S-parameter model of the mounting structure with 4 vias 32 mil apart



Input1 and Input2 – coaxial ports at the location of via-holes going through GND plane (plane is the reference side of these ports)



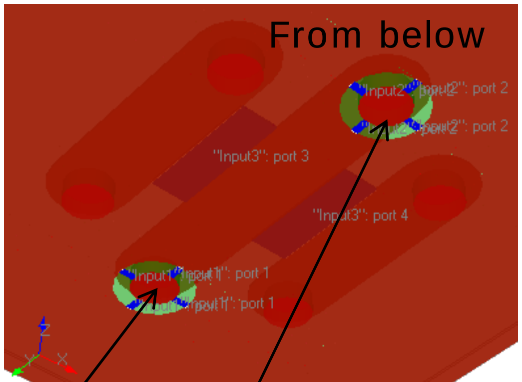
The model has to be connected with the model of a 0402 capacitor at the port Input3 and with a 2-D transmission plane model at ports Input1 and Input2



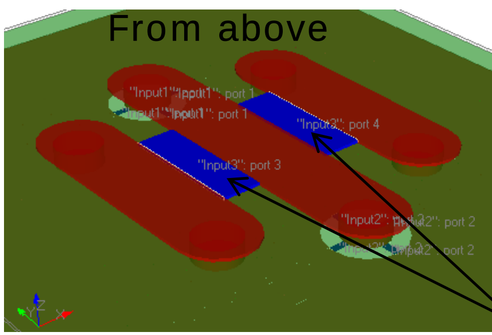
Input3 – lumped X-directed port between the pads with the reference side of the port (highlighted) connected to the vias connected to GND

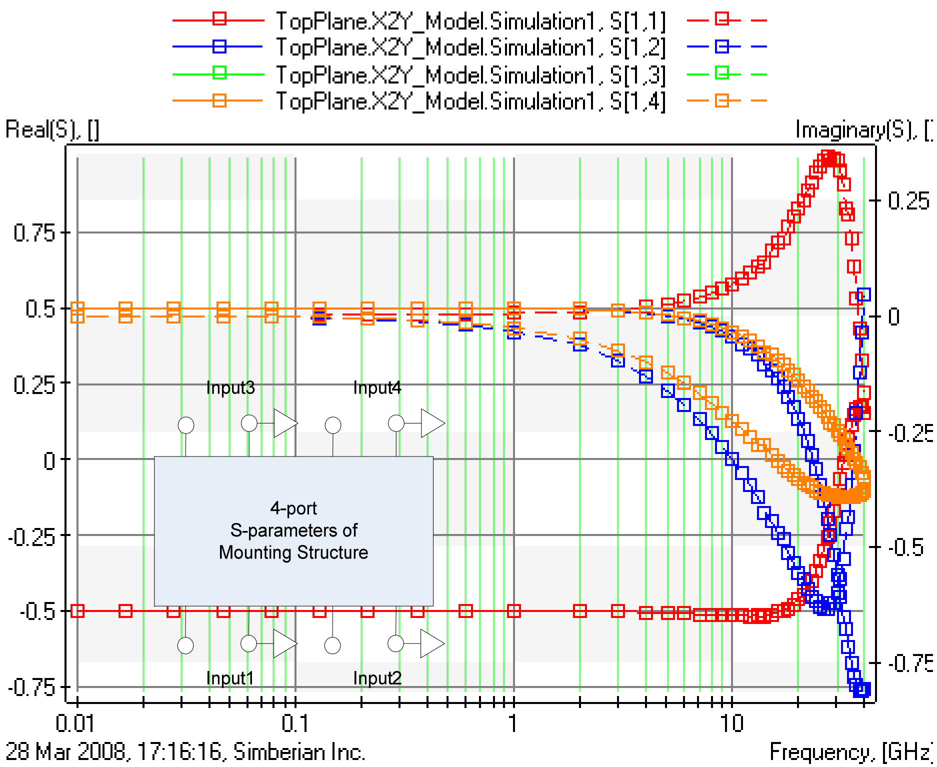
Final multiport S-parameter model of the mounting structure with 4 vias for X2Y

The model has to be connected with the model of the X2Y capacitor (2-port model) at the port Input3 and Input4 and with the 2-D transmission plane model at ports Input1 and Input2



Input1 and Input2 – coaxial ports at the location of via-holes going through GND plane (plane is the reference side of these ports)

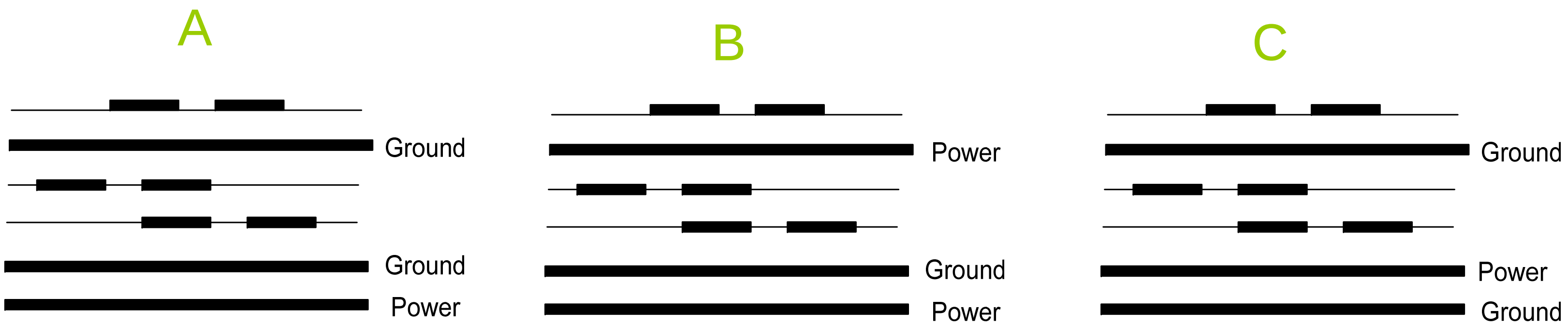




Input3/port 3 and port 4 – two lumped X-directed ports between the pads with the reference sides of the ports (highlighted) connected to the vias connected to GND

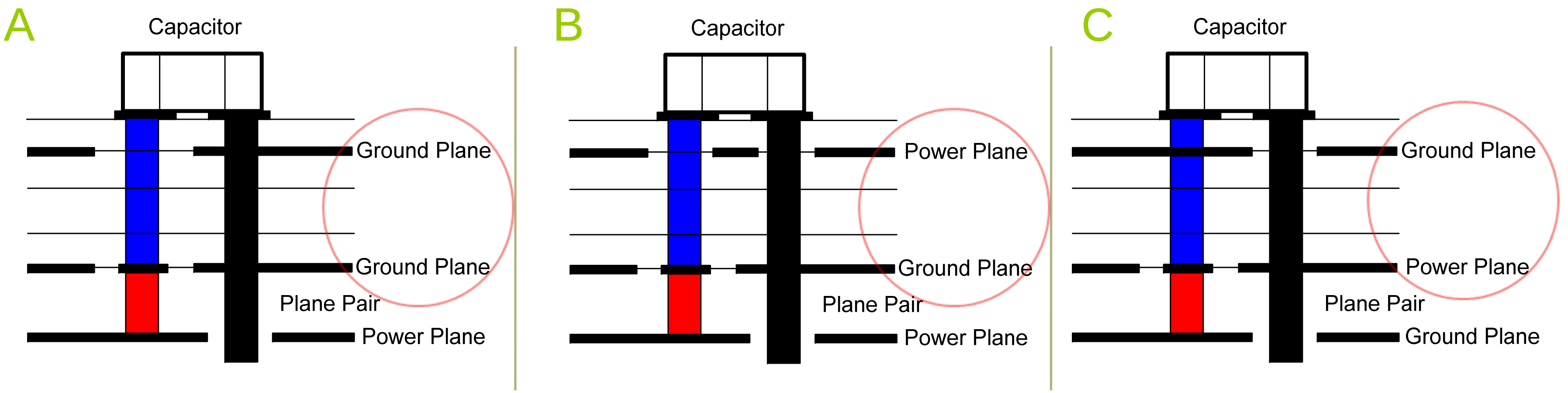
Cases with the decoupled planes shielded from the board surface

- Investigate 3 simple cases with just one plane and 2 additional signal layers between the board surface and plane pair
    A. Top shielding plane is ground and the topmost pane in the PDN plane pair is ground plane
    B. Top shielding plane is power plane and the topmost pane in the PDN plane pair is ground plane
    C. Top shielding plane is ground and the topmost pane in the PDN plane pair is power plane

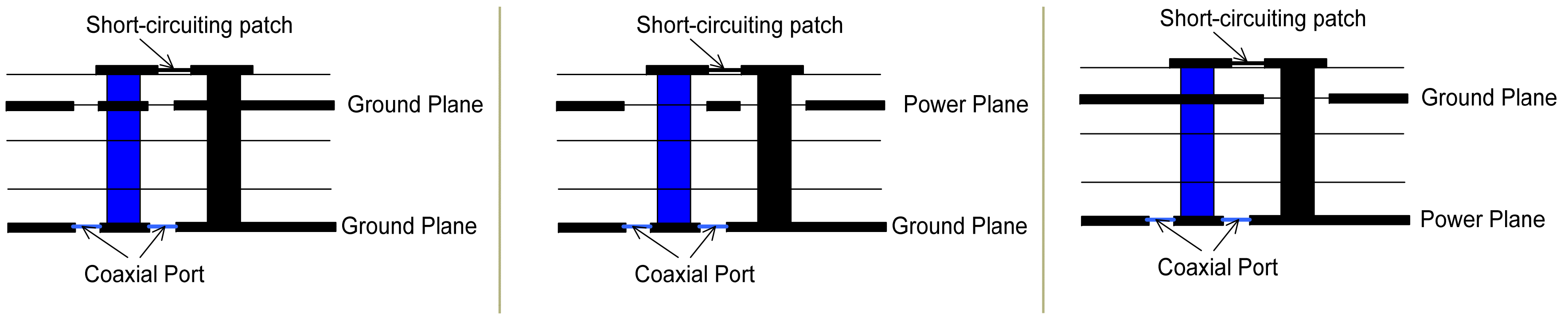


Only the portion of stackup above the topmost plane in the plane pair will be investigated – thus only portion of the stackup is shown here

Models for mounting structures with planes shielded from the board surface

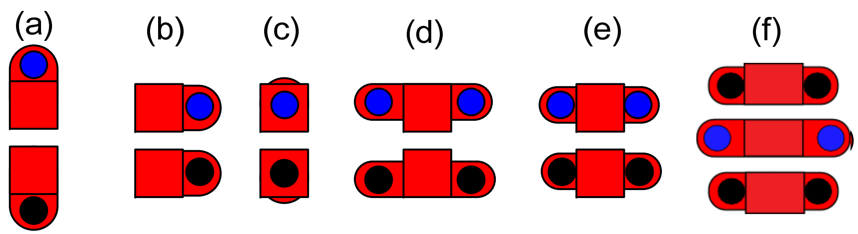


Capacitor mounting structure to be simulated to investigate the minimal possible mounting inductance



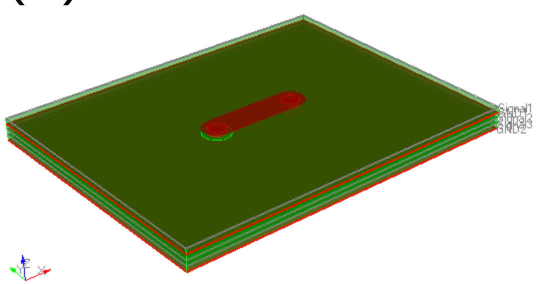
Only models for mounting structures with 2-vias are shown here.
Mounting structures with 4 and 6 vias are created in similar way and contain 2 coaxial ports
Final 2-port, 3-port and 4-port models for the mounting structures can be produced similar to the case with planes next to the board surface (see examples of the models in the solution files)

Geometries of circuits for 6 mounting structures with different connectivity to the planes (A,B,C)

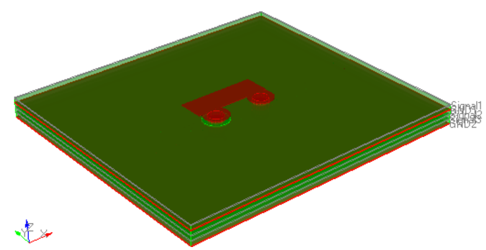


Blue vias end with coaxial port(s) in the bottommost planes
Black vias are connected to the bottommost planes

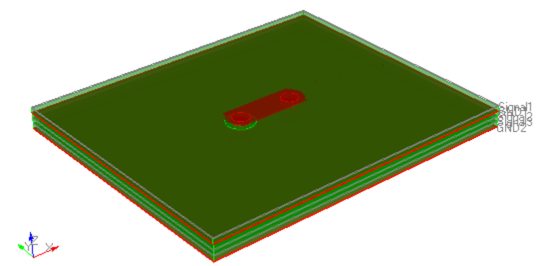
(a) 2Vias60mil



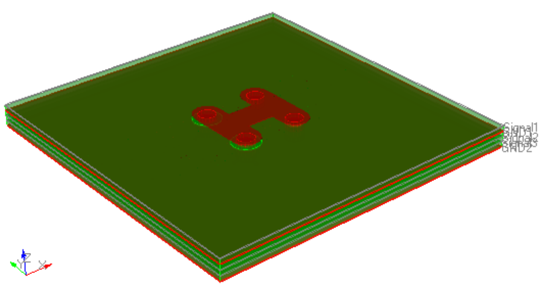
(b) 2Vias40mil



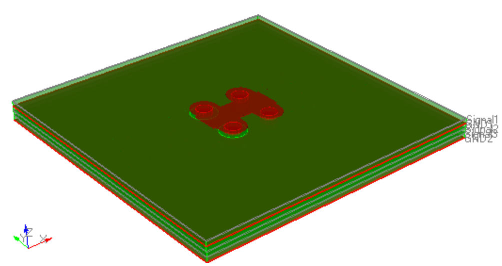
(c) 2ViasInPad



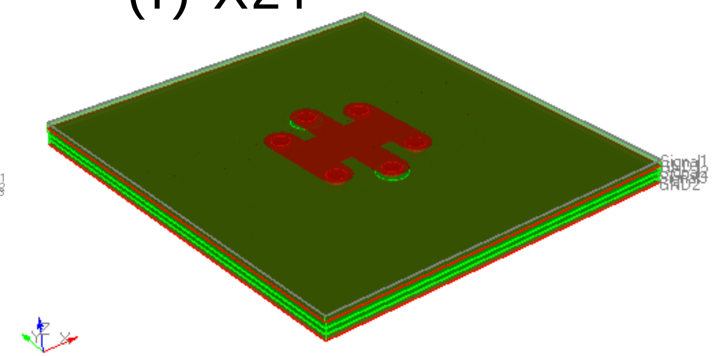
(d) 4Vias60mil



(e) 4ViasBest

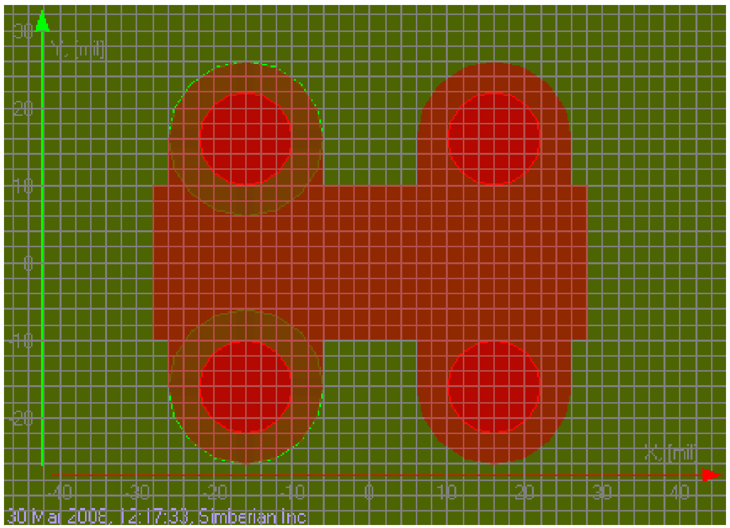


(f) X2Y

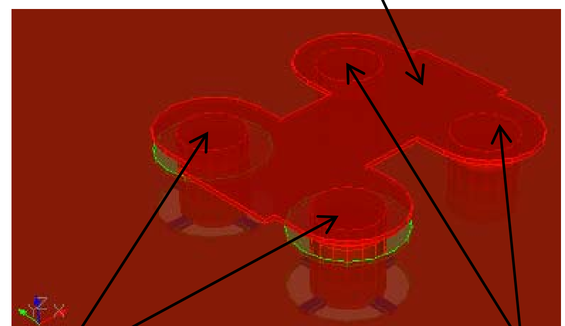


Case A: Example of geometry description for circuit (e) 4ViasBest

2x2 mil cell size – everything aligned to the grid



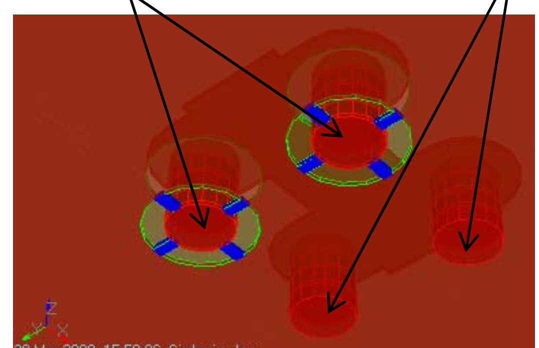
Layer Signal1: 4 via-hole pads, two capacitor mounting pads and short-circuiting plate in the middle



View from above

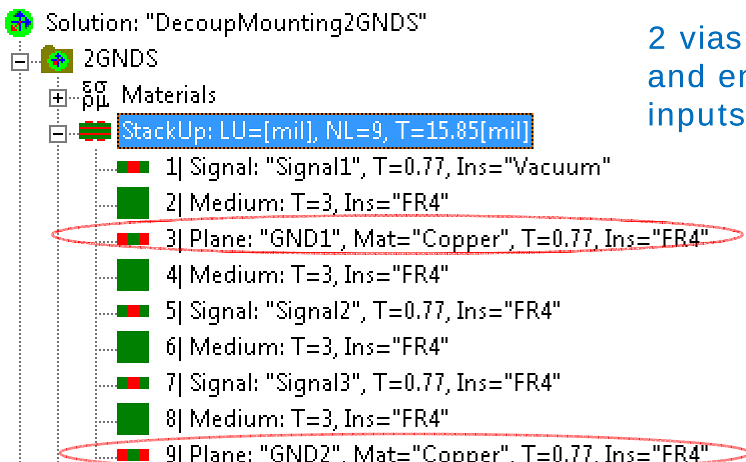
2 vias bypassing plane GND1 and ending with 2 coaxial inputs/ports in GND2

2 vias connected to both planes GND1 and GND2



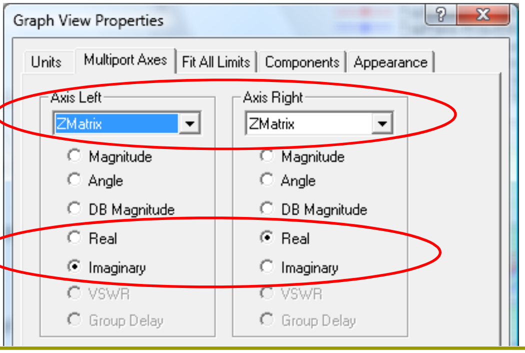
View from below

Stackup section above the topmost plane in the plane pair



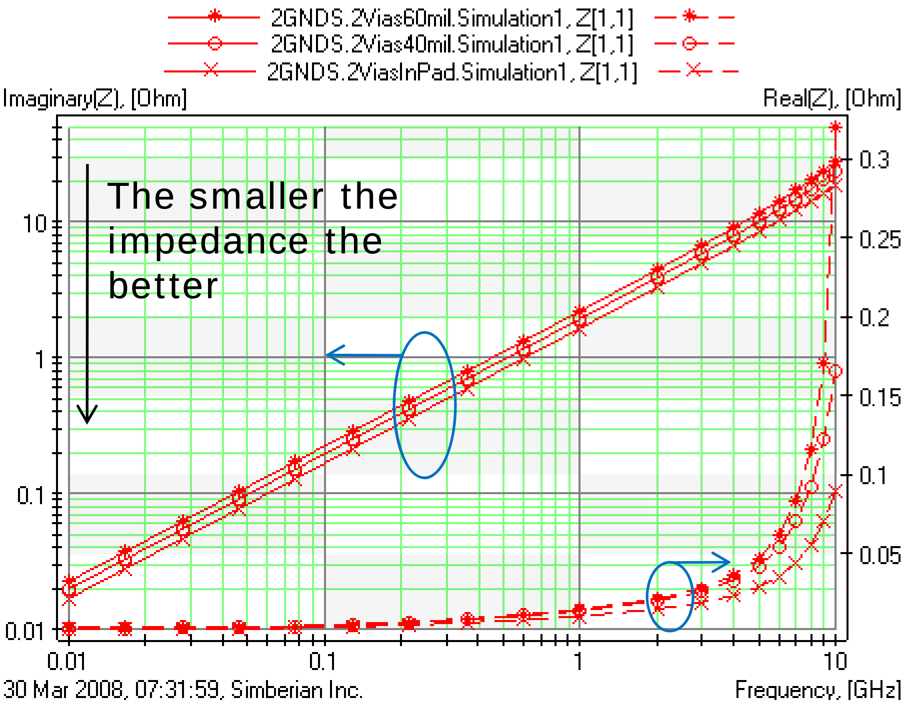
Case A: Simulation results

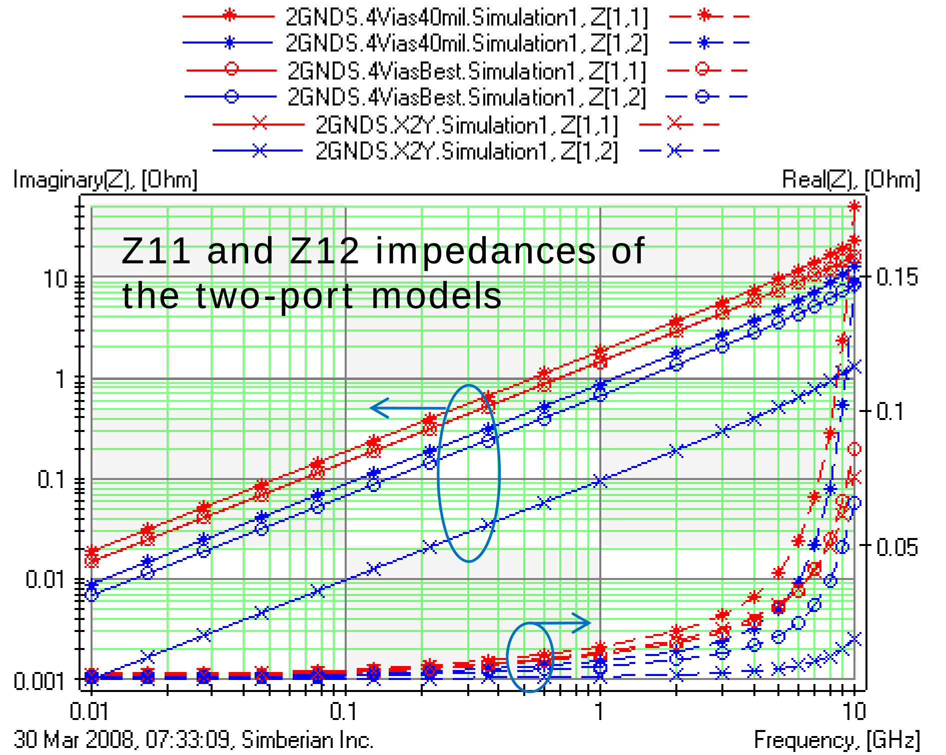
Graph properties to see Z-parameters



- Simulation takes few seconds per frequency point at 2 GHz dual core processor

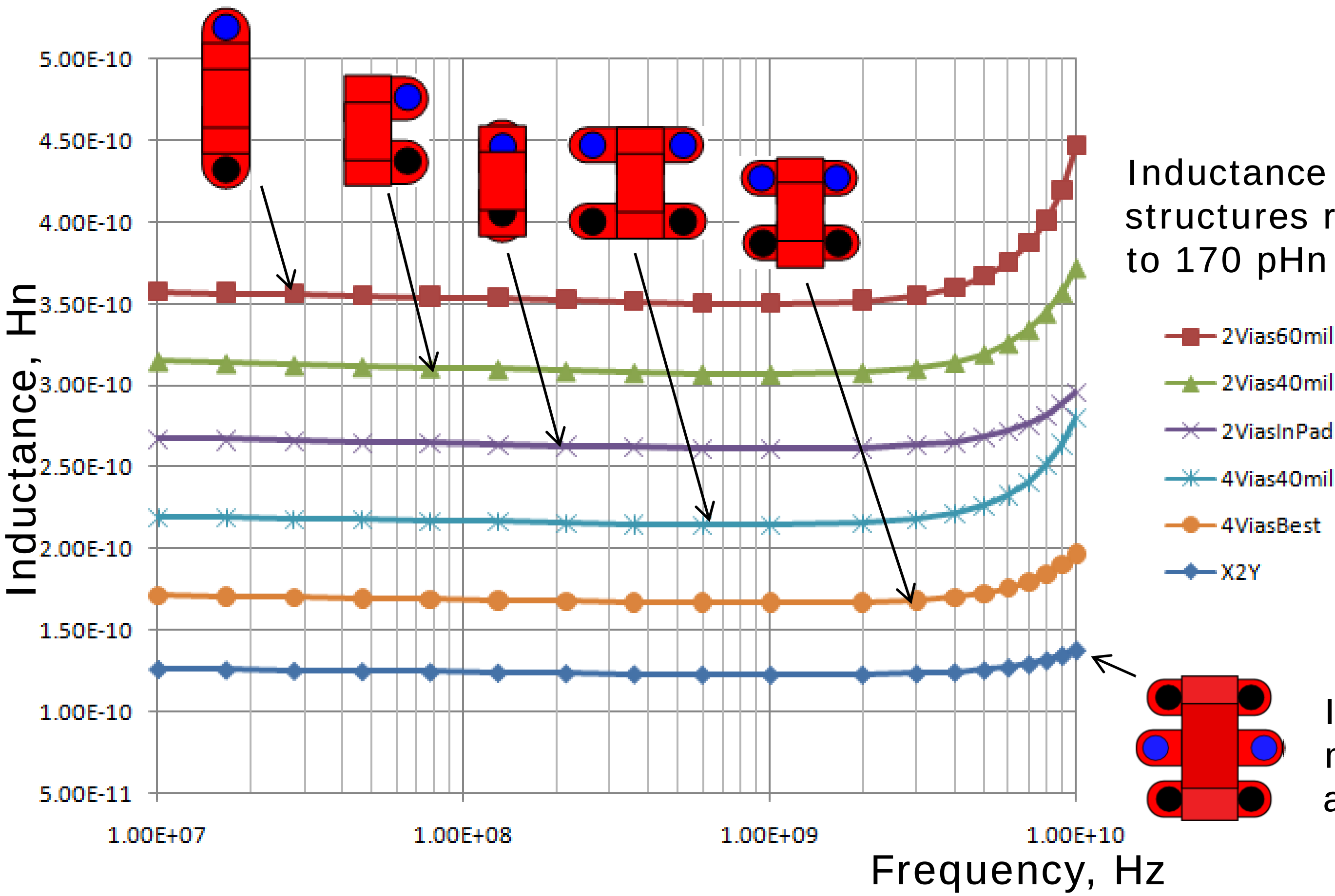
Z11 impedances of the one-port models





Case A (ground-ground): Comparison of the effective inductances of the mounting structures

These are the minimal possible inductances – they do not include the internal inductance of the capacitor and inductance of the via section between the planes!



Inductance of 0402 mounting structures ranges from 360 pHn to 170 pHn (at low frequencies)

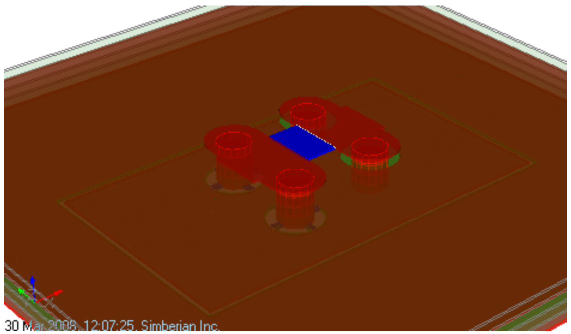
The first-order approximation by inductance is not valid above about 4 GHz

Inductance of X2Y mounting structure is about 125 pHn

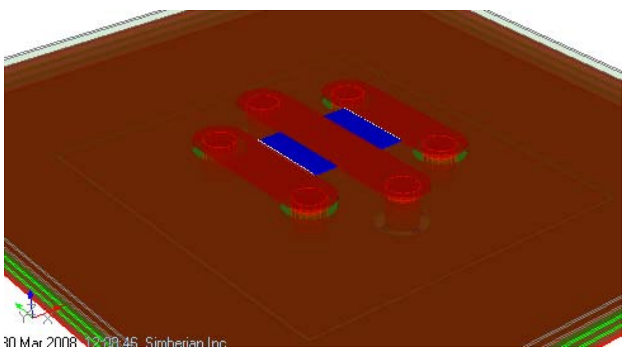
Case A: Final 3-port and 4-port S-parameter models of mounting structures

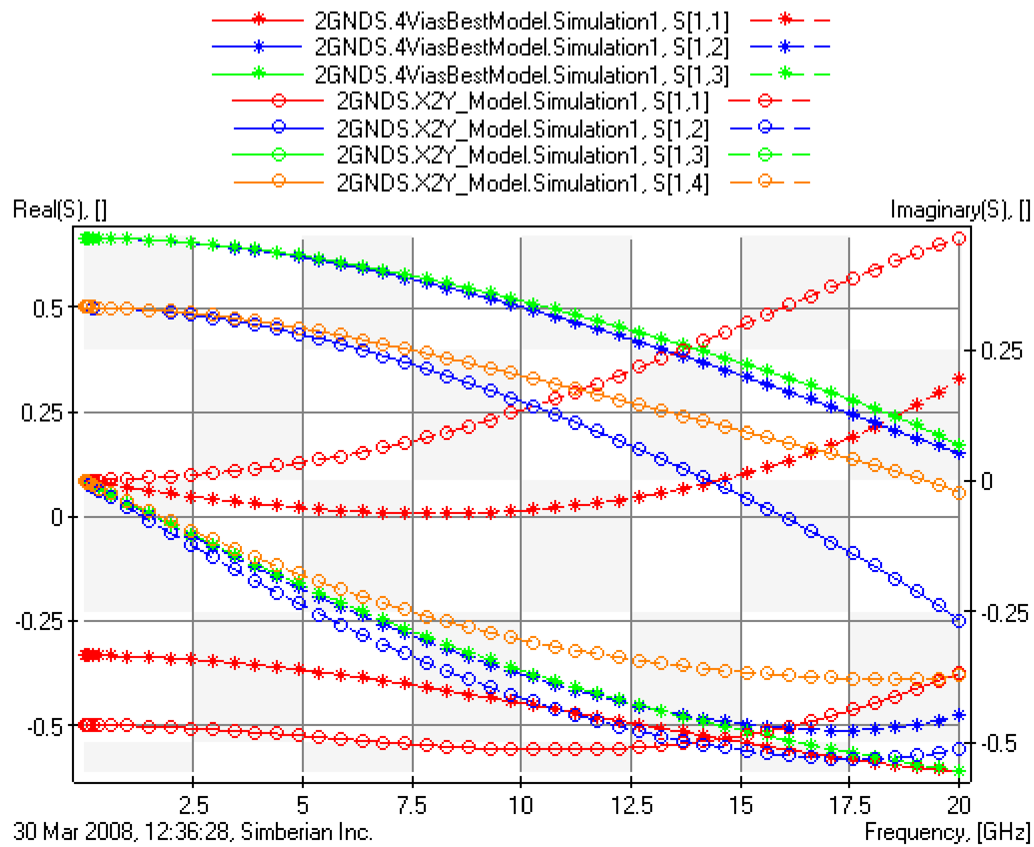
- The model has to be connected by lumped ports in the top layer with a capacitor model and by coaxial ports with a model of transmission planes

4ViasBestModel: 3-port



X2Y_Model: 4-port

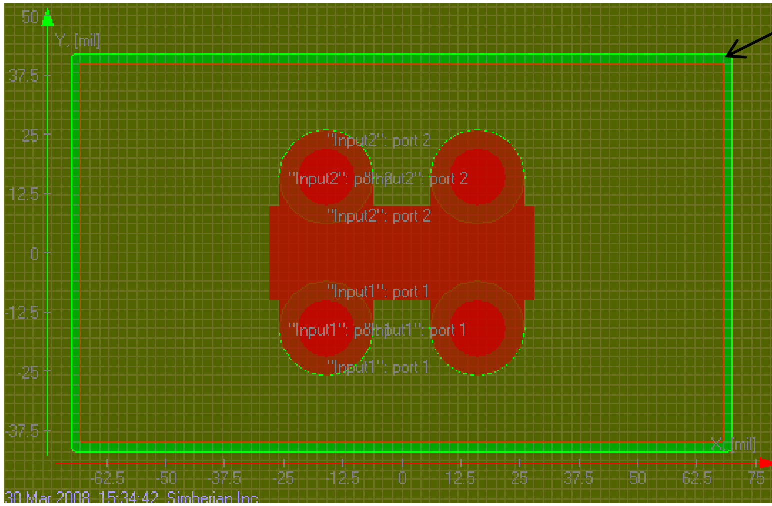




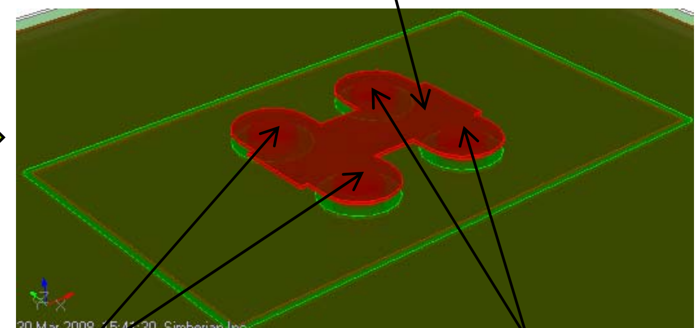
Case B: Example of geometry description for the circuit (e) 4ViasBest

2x2 mil cell size – everything aligned to the grid

Rectangular moat in plane V1 for isolation

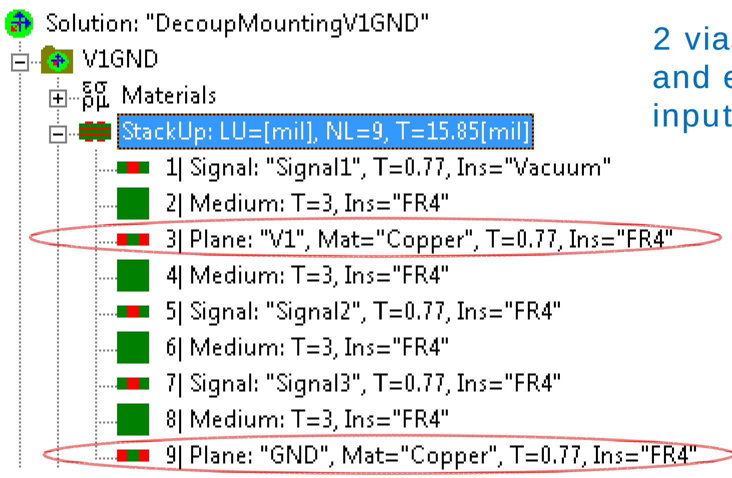


Layer Signal1: 4 via-hole pads, two capacitor mounting pads and short-circuiting plate in the middle



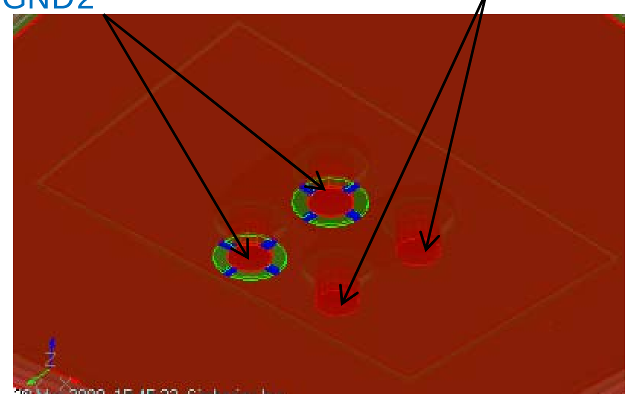
View from above

Stackup section above the topmost plane in the plane pair



2 vias bypassing plane GND1 and ending with 2 coaxial inputs/ports in GND2

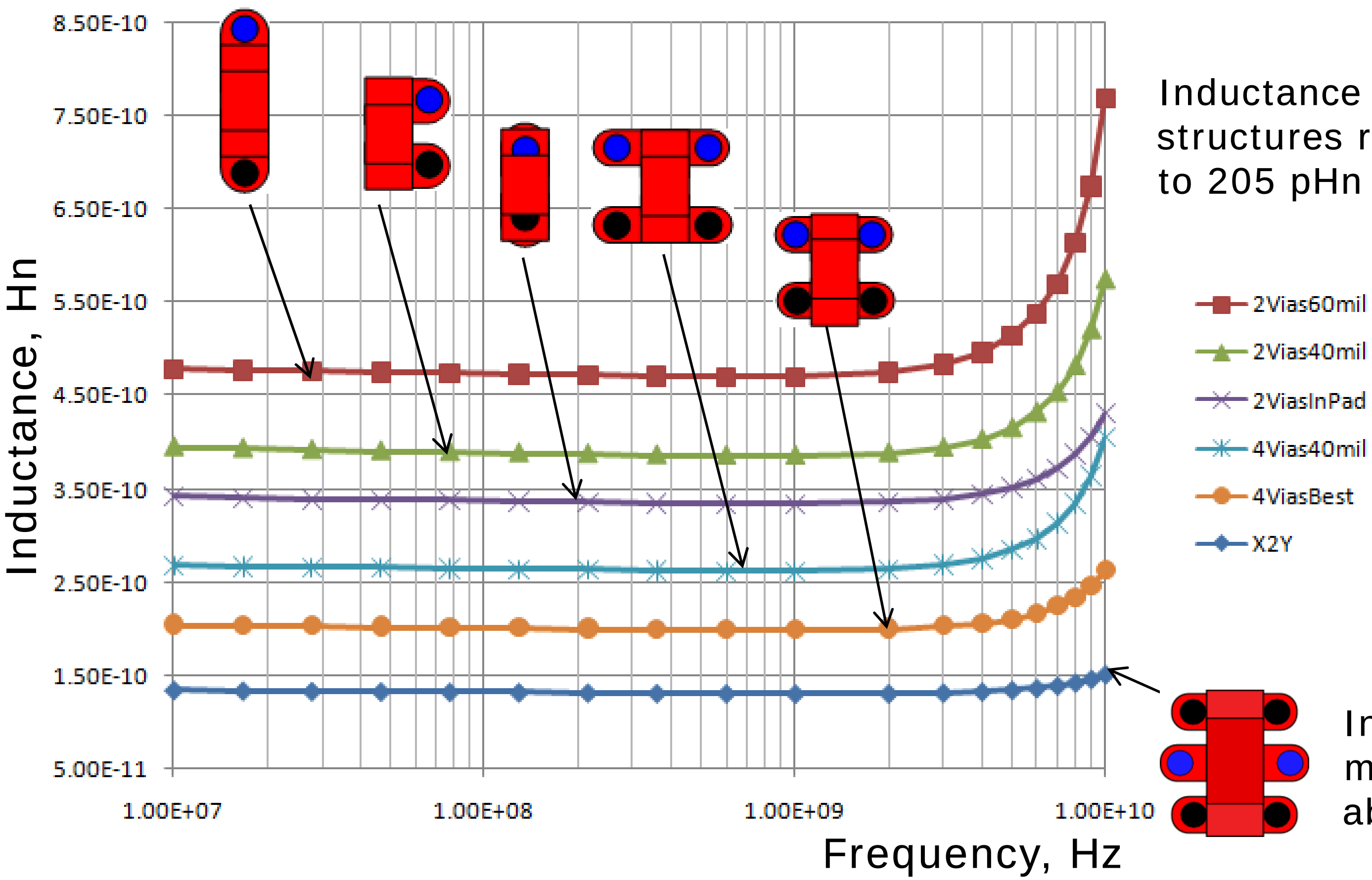
2 vias passing plane V1 and connected plane GND



View from below

Case B (power-ground): Comparison of effective inductances of the mounting structures

These are the minimal possible inductances – they do not include the internal inductance of the capacitor and inductance of the via section between the planes!



Inductance of 0402 mounting structures ranges from 480 pHn to 205 pHn (at low frequencies)

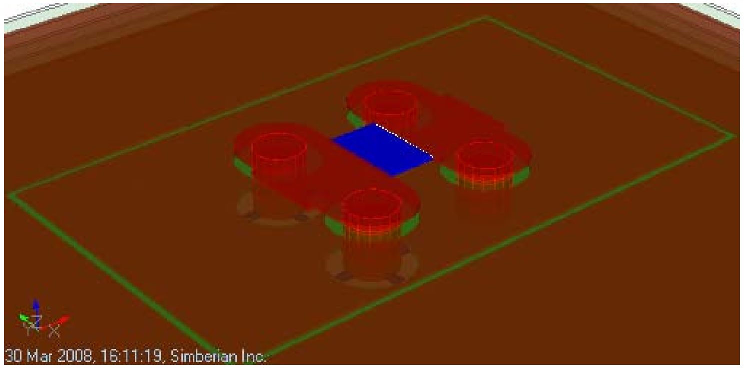
The first-order approximation by inductance is not valid above about 4 GHz

Inductance of X2Y mounting structure is about 135 pHn

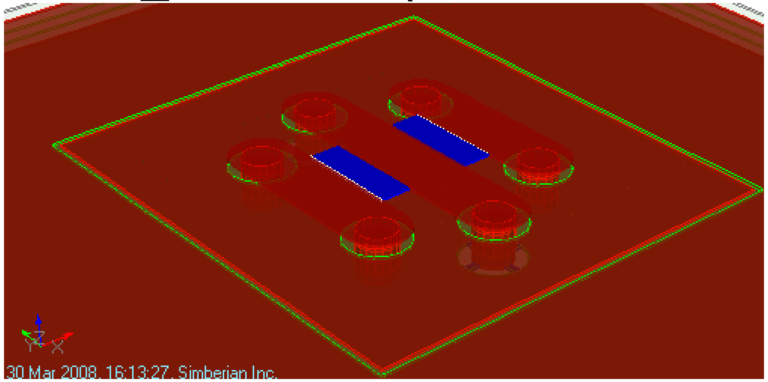
Case B: Final 3-port and 4-port S-parameter models of mounting structures

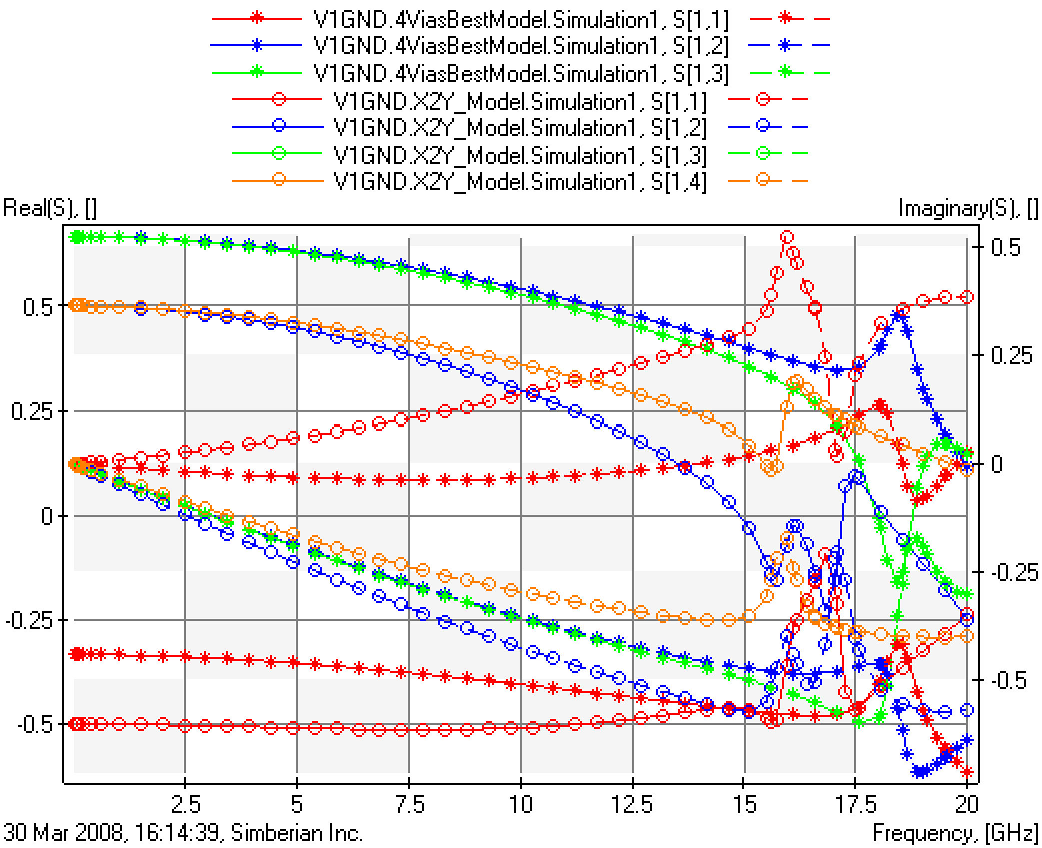
- The model has to be connected by lumped ports in the top layer with the capacitor model and by coaxial ports with a model of transmission planes

4ViasBestModel: 3-port



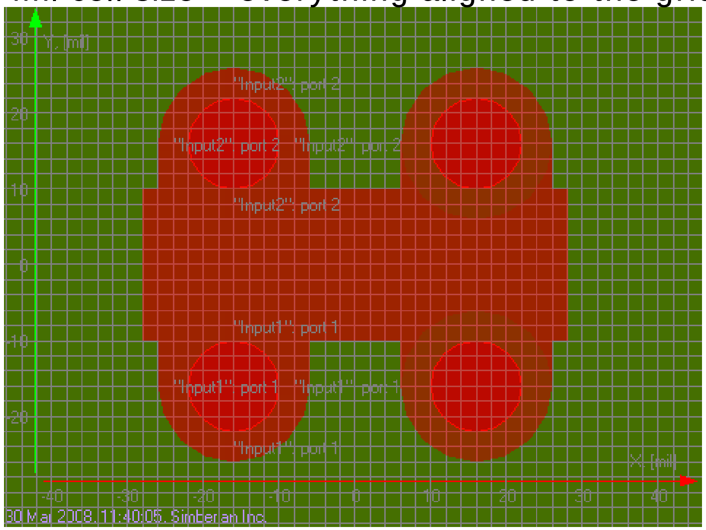
X2Y_Model: 4-port



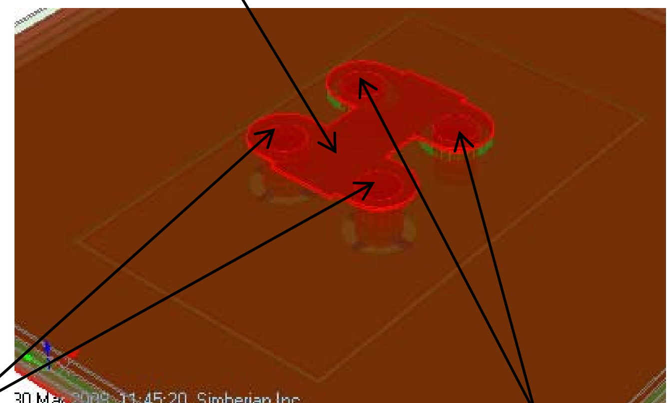


Case C: Example of geometry description for the circuit (e) 4ViasBest

2x2 mil cell size – everything aligned to the grid



Layer Signal1: 4 via-hole pads, two capacitor mounting pads and short-circuiting plate in the middle



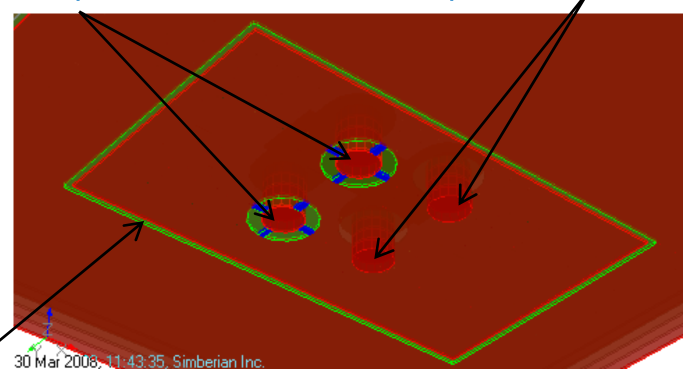
View from above

Stackup section above the topmost plane in the plane pair

Solution: "DecoupMountingGNDV1"
V1GND
Materials
StackUp: LU=[mil], NL=9, T=15.85[mil]
1| Signal: "Signal1", T=0.77, Ins="Vacuum"
2| Medium: T=3, Ins="FR4"
3| Plane: "GND", Mat="Copper", T=0.77, Ins="FR4"
4| Medium: T=3, Ins="FR4"
5| Signal: "Signal2", T=0.77, Ins="FR4"
6| Medium: T=3, Ins="FR4"
7| Signal: "Signal3", T=0.77, Ins="FR4"
8| Medium: T=3, Ins="FR4"
9| Plane: "V1", Mat="Copper", T=0.77, Ins="FR4"

2 vias connected to plane GND and ending with 2 coaxial inputs/ports in plane V1

2 vias bypassing plane GND and connected to plane V1

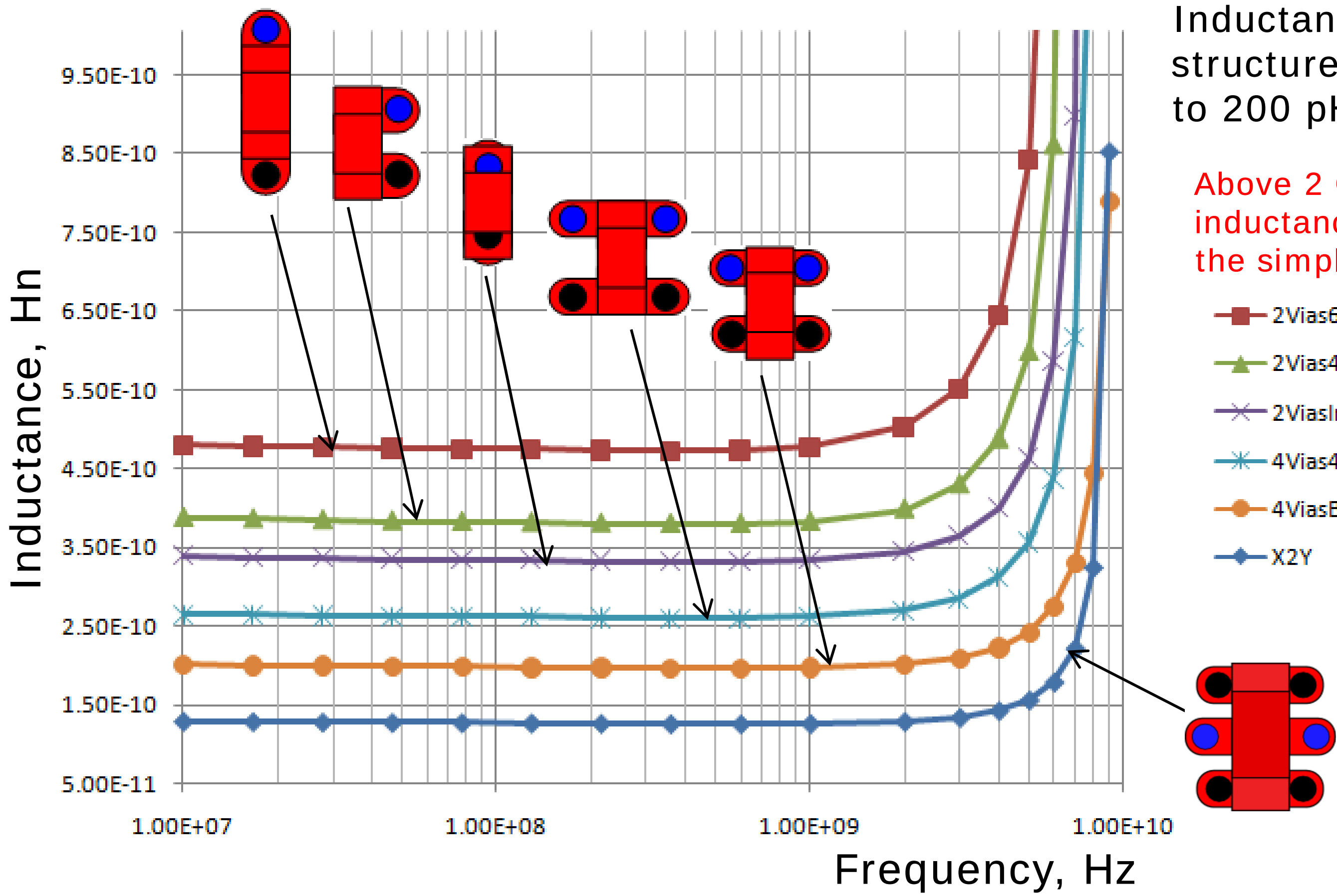


View from below

1-cell wide moat in plane V1 (void trace)

Case C (ground-power): Comparison of effective inductances of the mounting structures

These are the minimal possible inductances – they do not include the internal inductance of the capacitor and inductance of the via section between the planes!



Inductance of 0402 mounting structures ranges from 480 pHn to 200 pHn (at low frequencies)

Above 2 GHz the effective inductance grows rapidly – the simple approximation fails!

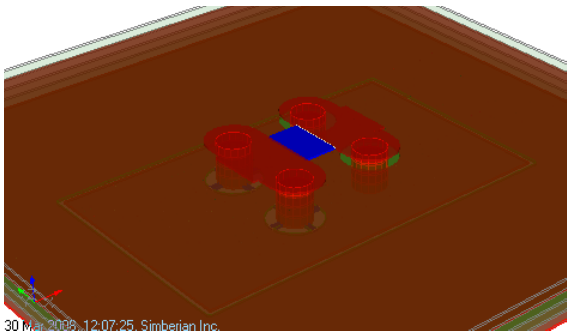
The first-order approximation by inductance is not valid above about 2 GHz

Inductance of X2Y mounting structure is about 130 pHn

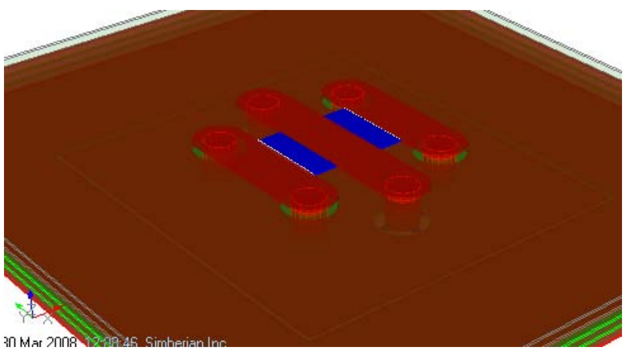
Case C: Final 3-port and 4-port S-parameter models of the mounting structures

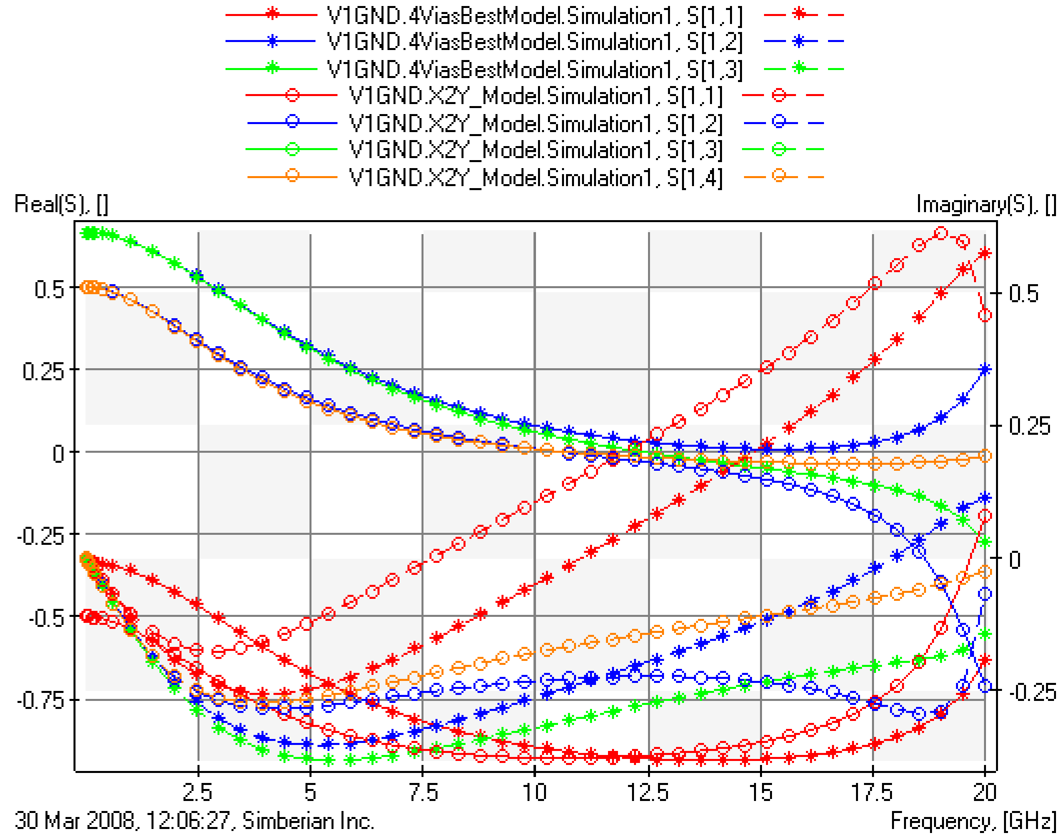
- The model has to be connected by lumped ports in the top layer with a capacitor model and by coaxial ports with a model of transmission planes

4ViasBestModel: 3-port



X2Y_Model: 4-port





Conclusion

- Examples of what-if analysis of different decoupling capacitors mounting structures with Simbeor solver have been provided
- Quantitative analysis shows how different capacitor mounting and stackup solutions can significantly affect the overall inductance of the decoupling structure
- Final models extracted with Simbeor solver can be used with a 2-D plane solver to increase accuracy of the decoupling analysis
  - It has to be done only for the high-frequency capacitors and number of mounting geometries is usually very limited per board
- Geometry description and problems set-up in Simbeor took approximately 4 hours, simulation times for each case were within minutes

Solutions and contact

- Solution files are available for download from the simberian web site
  - http://www.simberian.com/AppNotes/Solutions/DecapMountingStructures_2008_01.zip
- Send questions and comments to
  - General: info@simberian.com
  - Sales: sales@simberian.com
  - Support: support@simberian.com
- Web site www.simberian.com