Simberian
Electromagnetic Solutions

Analysis of via-hole cross-talk and reflection loss for BGA break-out

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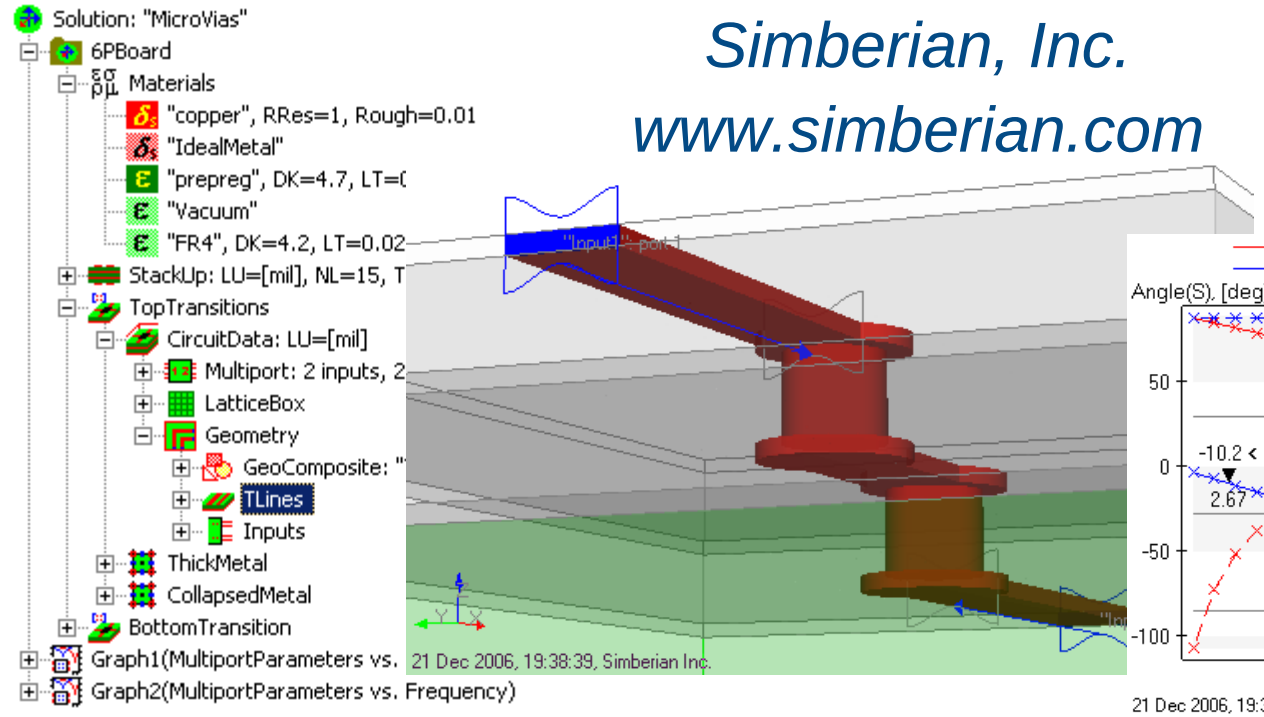
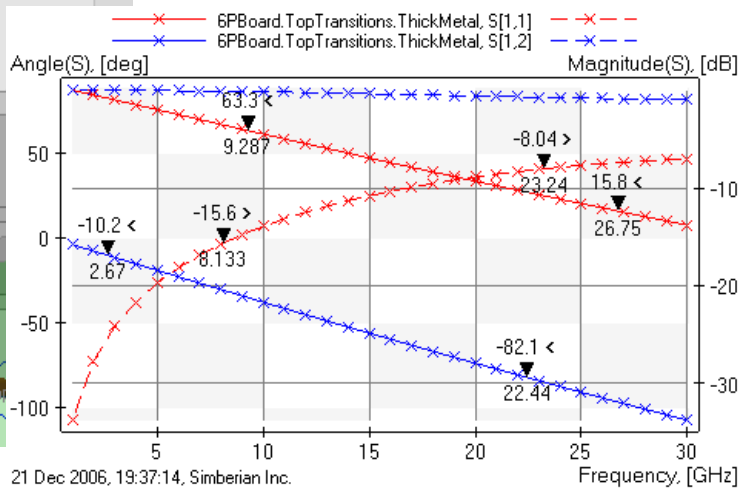
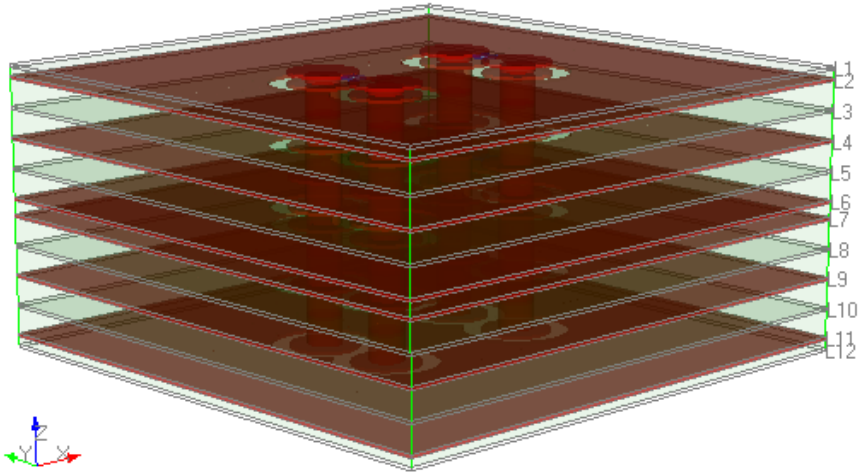




Original configuration of two pairs of via-holes in BGA break-out area on 12-layer PCB

Example PCB_MCM/ XViasOptimization/ XViasOptimization.esx

- StackUp: LU=[mil], NL=23, T=63.64
  - 1| Signal: "L1", T=0.77, Ins="Vacuum"
  - 2| Medium: T=1.7, Ins="1086 LD Prepreg"
  - 3| Plane: "L2", Mat="Copper", T=0.77, Ins="1506 Prepreg"
  - 4| Medium: T=6, Ins="1506 Prepreg"
  - 5| Signal: "L3", T=0.77, Ins="1506 Prepreg"
  - 6| Medium: T=6, Ins="Core"
  - 7| Plane: "L4", Mat="Copper", T=0.77, Ins="1506 Prepreg"
  - 8| Medium: T=6, Ins="1506 Prepreg"
  - 9| Signal: "L5", T=0.77, Ins="1506 Prepreg"
  - 10| Medium: T=6, Ins="Core"
  - 11| Plane: "L6", Mat="Copper", T=0.77, Ins="1080 Prepreg"
  - 12| Medium: T=3, Ins="1080 Prepreg"
  - 13| Plane: "L7", Mat="Copper", T=0.77, Ins="1080 Prepreg"
  - 14| Medium: T=6, Ins="Core"
  - 15| Signal: "L8", T=0.77, Ins="1506 Prepreg"
  - 16| Medium: T=6, Ins="1506 Prepreg"
  - 17| Plane: "L9", Mat="Copper", T=0.77, Ins="1506 Prepreg"
  - 18| Medium: T=6, Ins="Core"
  - 19| Signal: "L10", T=0.77, Ins="1506 Prepreg"
  - 20| Medium: T=6, Ins="1506 Prepreg"
  - 21| Plane: "L11", Mat="Copper", T=0.77, Ins="1506 Prepreg"
  - 22| Medium: T=1.7, Ins="1086 LD Prepreg"
  - 23| Signal: "L12", T=0.77, Ins="Vacuum"
- DifVias

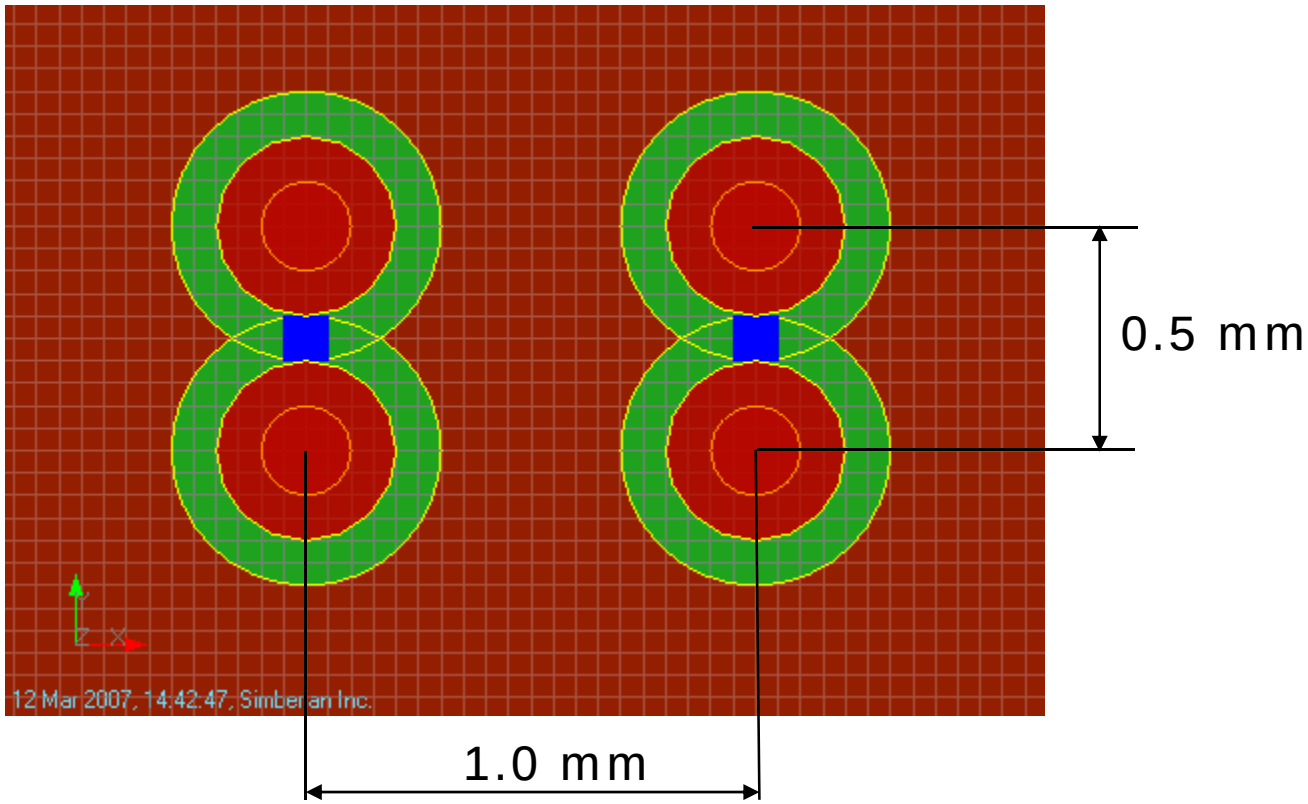


12 Mar 2007, 14:38:05, Simberian Inc.

- ViaXtalk2
  - Materials
    - "Copper", RR=1
    - "IdealMetal"
    - "1506 Prepreg", Dk=4.1, LT=0.01, PLM=WD
    - "Vacuum"
    - "1086 LD Prepreg", Dk=4.1, LT=0.01, PLM=WD
    - "1080 Prepreg", Dk=4.1, LT=0.01, PLM=WD
    - "Core", Dk=4.2, LT=0.02, PLM=WD
  - StackUp: LU=[mil], NL=23, T=63.64
  - DifVias
    - CircuitData: LU=[mm]
    - Simulation1

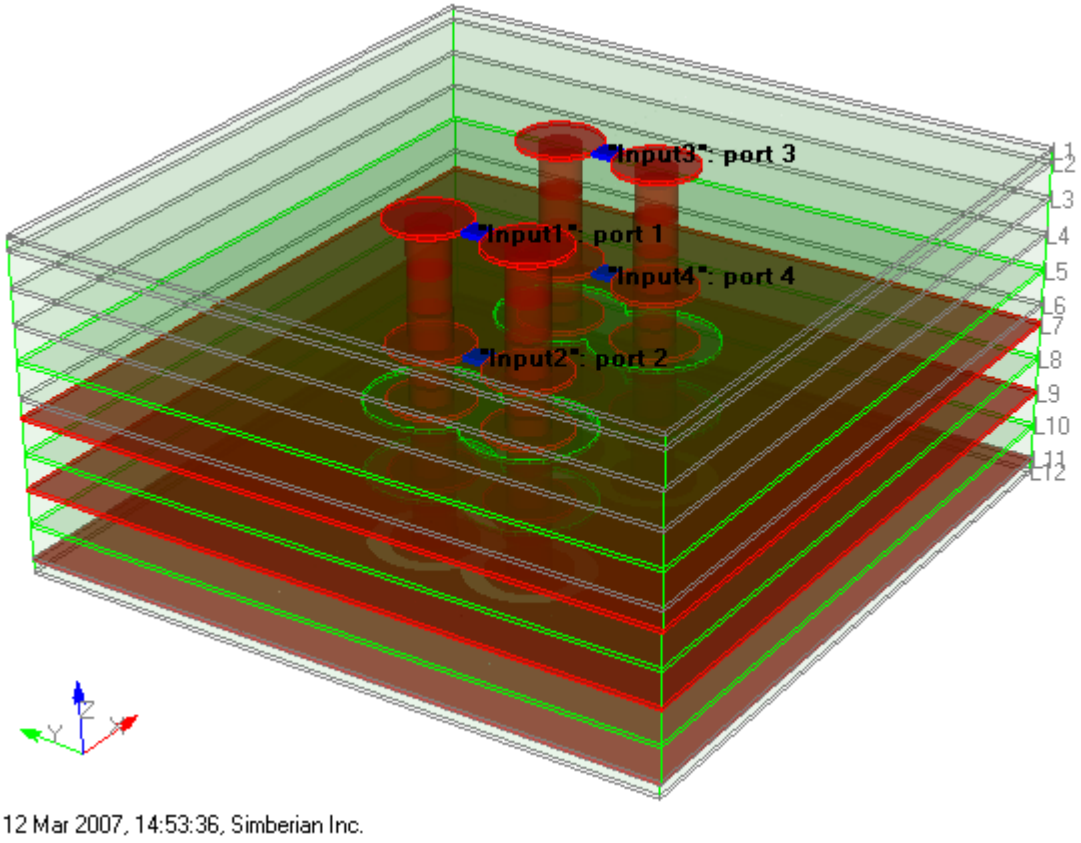
Two pairs of vias side-by-side 1 mm apart

Lattice cell size is 0.05 mm; Anti-pads with diameter 0.6 mm in all plane layers; Pads with diameter 0.4 mm in all plane layers and in layers L1 and L5; Via barrels 0.2 mm

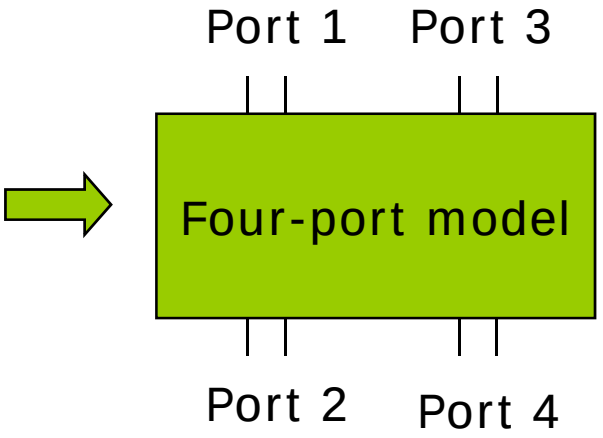


View of four ports in layers L1 and L5

Ports are similar to measurement probes an created for differential excitation of two vias at layers L1 and L5



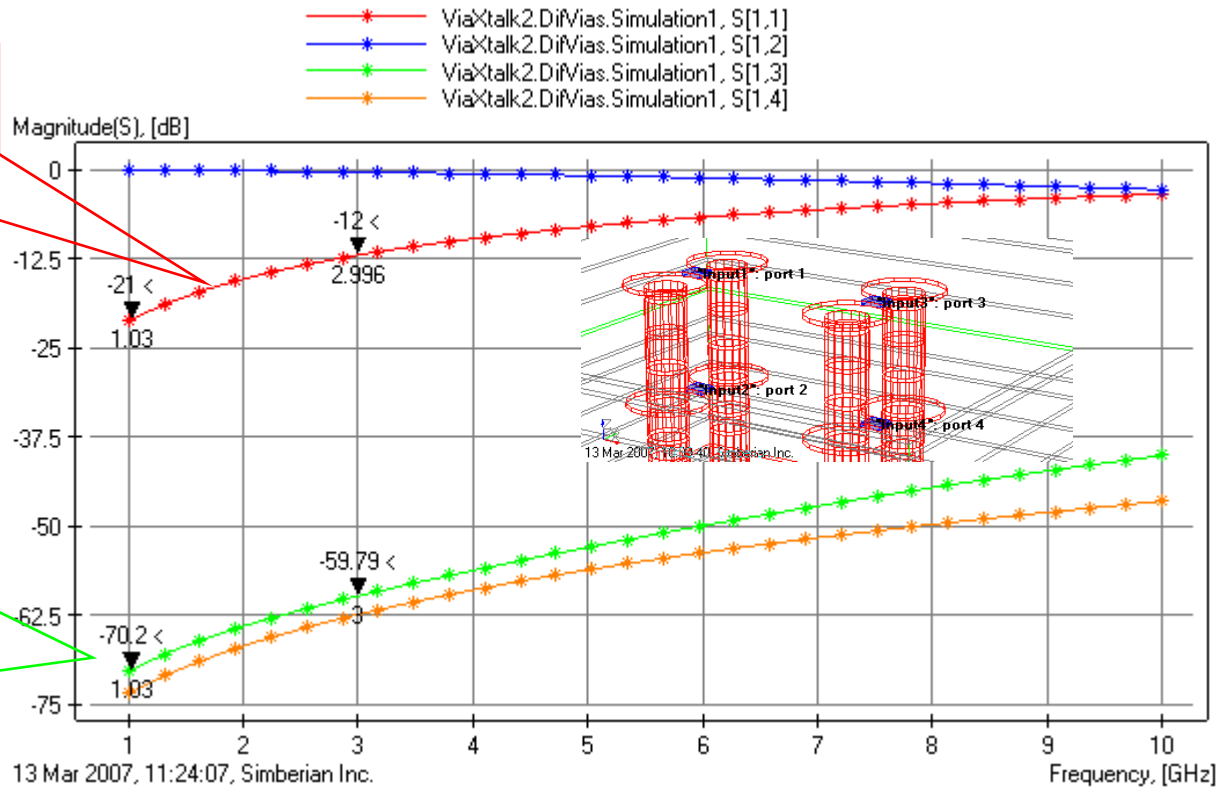
Extract only differential to differential multiport parameters, normalize S-parameters to 100 Ohm



Via reflection loss and cross-talk

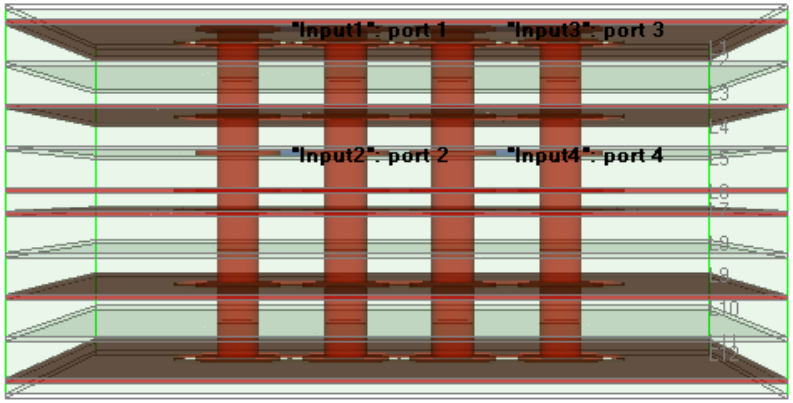
High reflection loss because of via stubs and additional capacitance between pads and to the planes

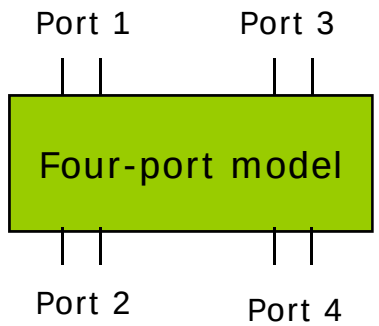
Very low near and far end cross-talk because of large distance between vias and the plane shielding effect

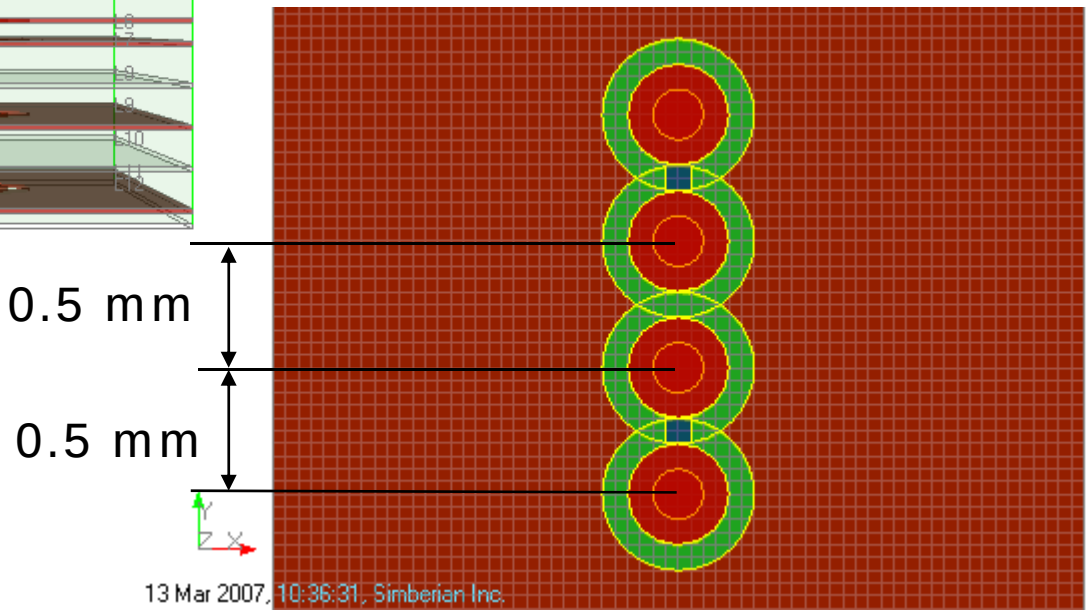


Two pairs of vias in a row: Configuration 1

Lattice cell size is 0.05 mm; Anti-pads with diameter 0.6 mm in all plane layers; Pads with diameter 0.4 mm in all plane layers and in layers L1 and L5; Via barrels 0.2 mm



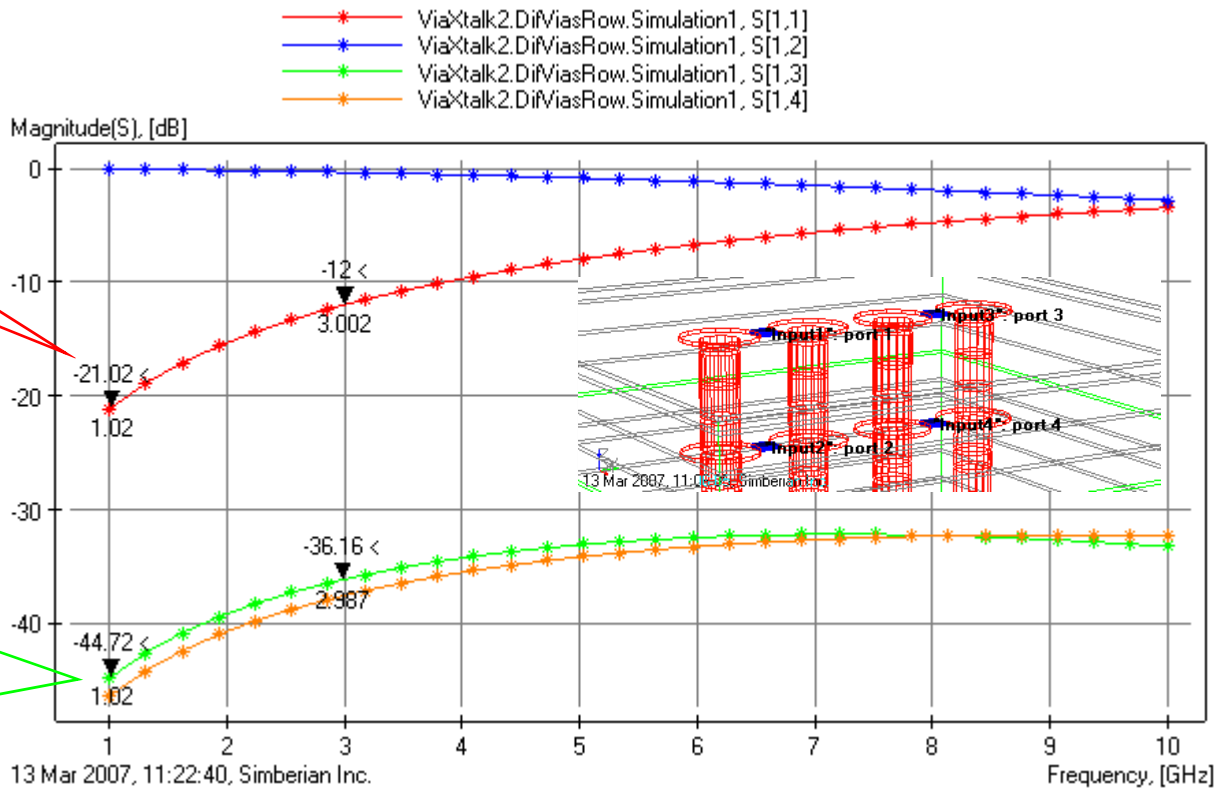




Via reflection loss and cross-talk

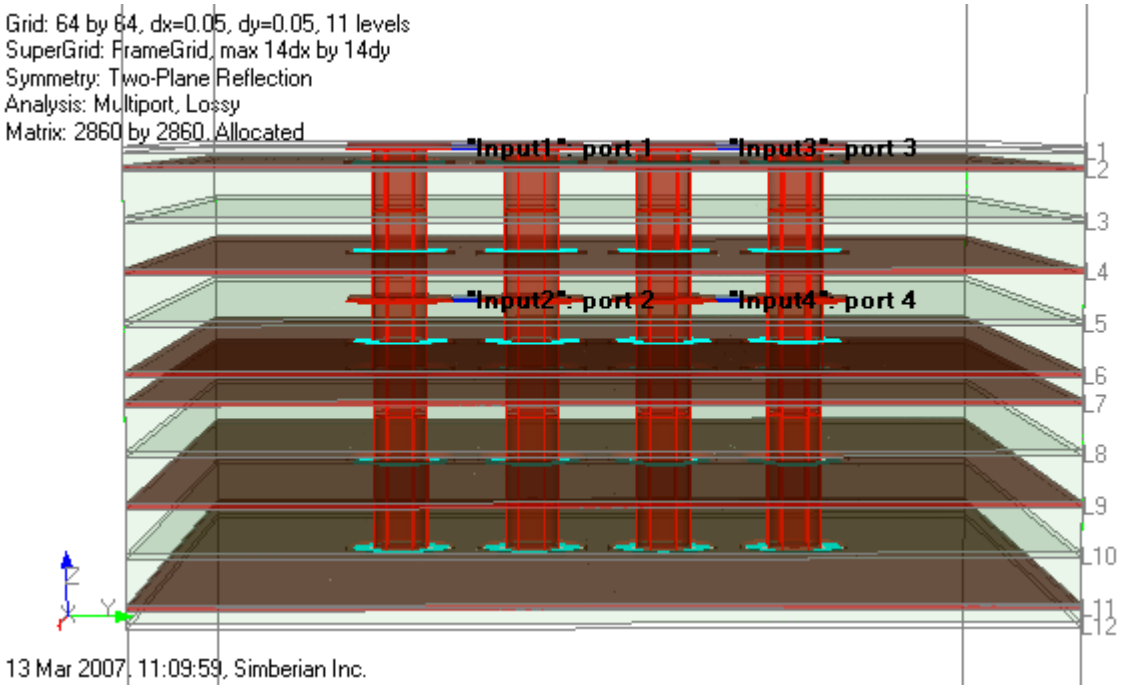
High reflection loss because of via stubs and additional capacitance to the planes

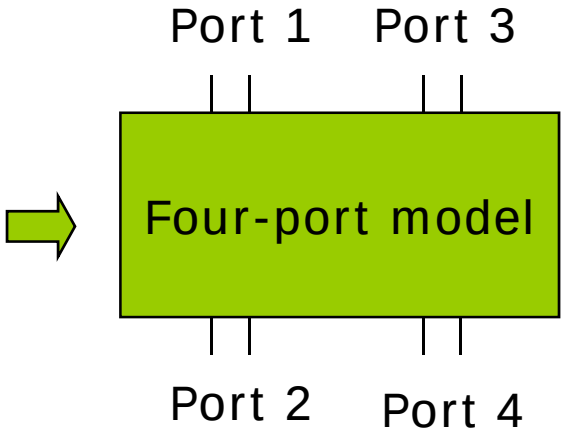
Higher near and far end cross-talk because of proximity of multiple pads



Two pairs of vias in a row: Configuration 2

Lattice cell size is 0.05 mm; Anti-pads with diameter 0.42 mm in all plane layers; Pads with diameter 0.4 mm only in layers L1 and L5; Via barrels 0.2 mm

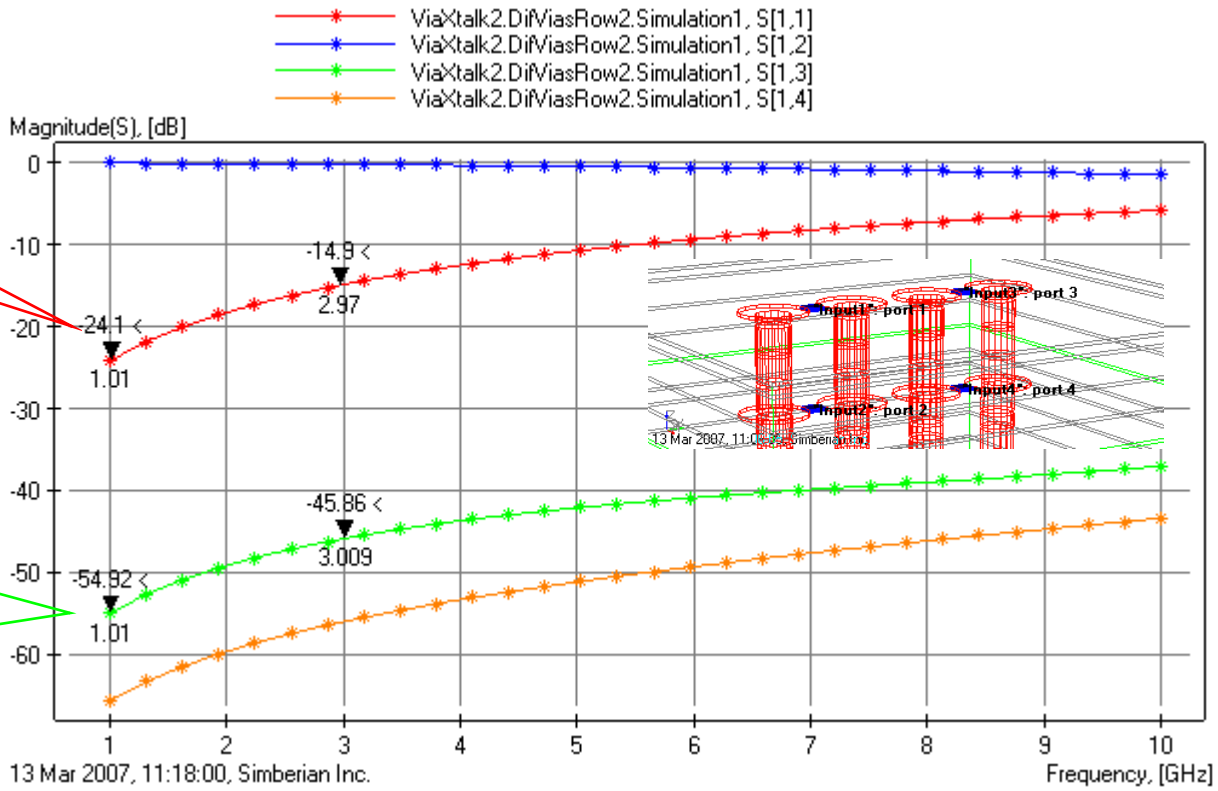




Via reflection loss and cross-talk for configuration 2 (optimized pads)

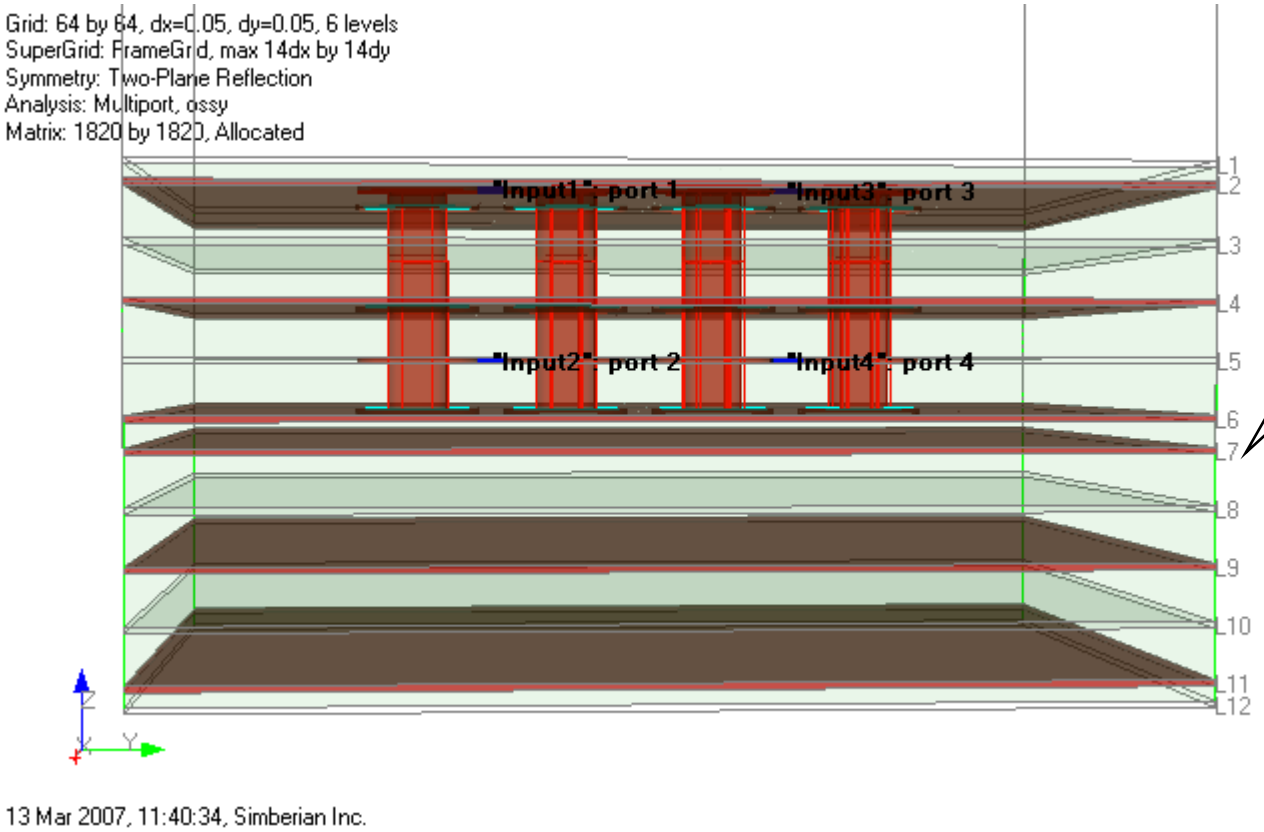
Lower reflection loss because of lower overall capacitance between the vias

Lower near and far end cross-talk because of lower capacitance between the remaining pads



Two pairs of vias in a row without via-stubs: Configuration 3

Lattice cell size is 0.05 mm; Anti-pads with diameter 0.42 mm in plane layers L2, L4 and L6; Pads with diameter 0.4 mm only in layers L1 and L5; Via barrels 0.2 mm

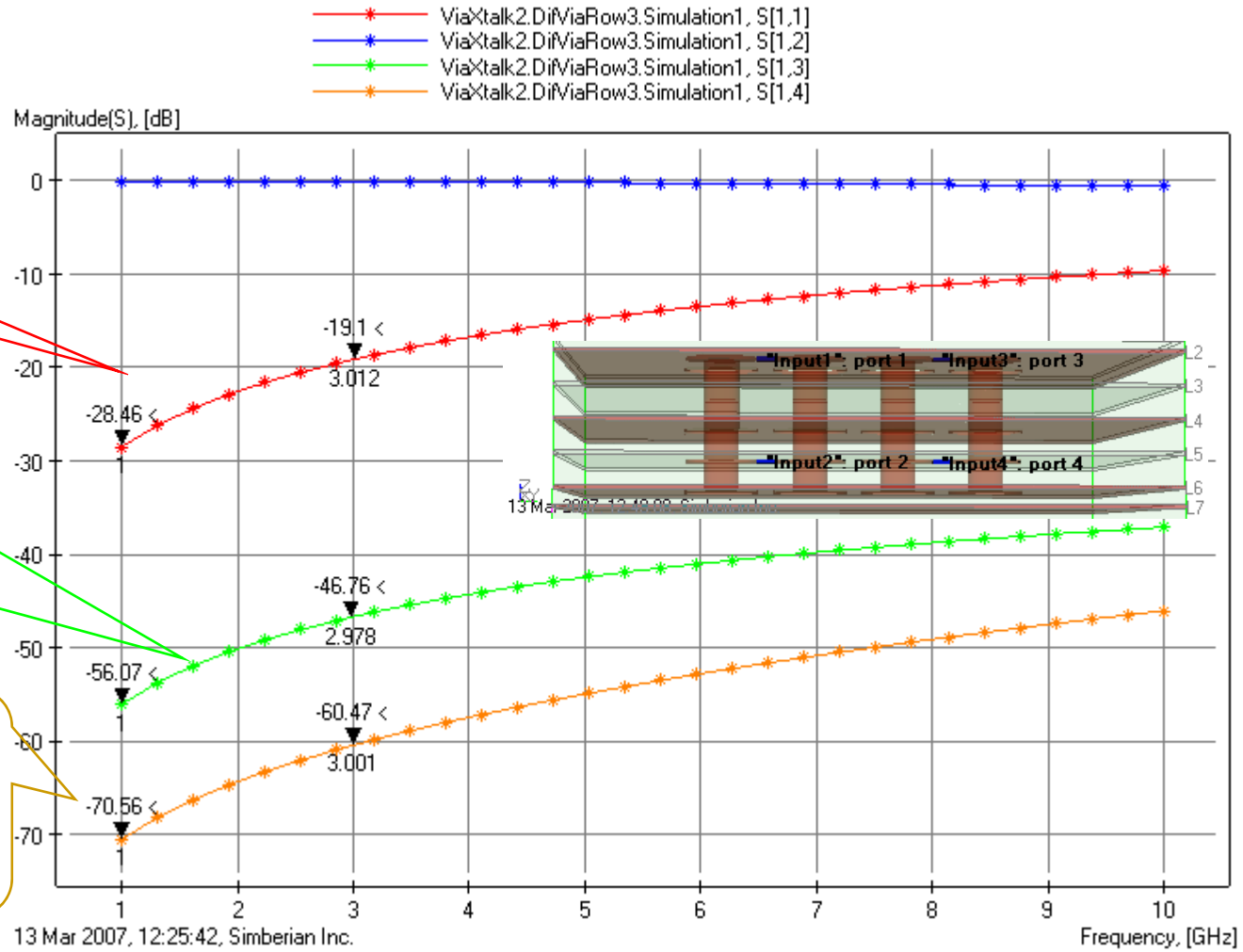


Via reflection loss and cross-talk for configuration 3 (no via-stubs)

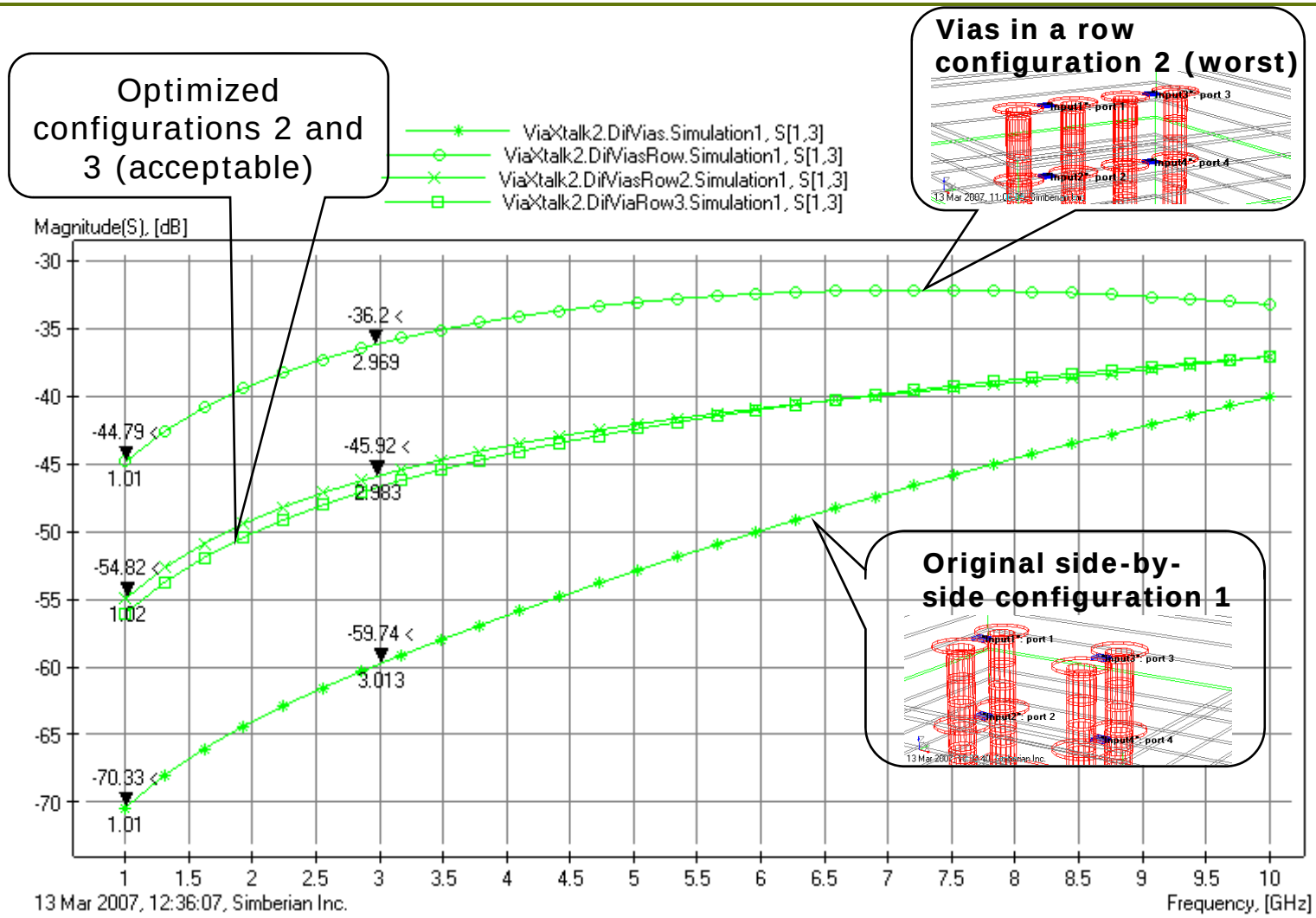
Lower reflection loss because of lower overall capacitance between the vias

Lower near end cross-talk because of lower capacitance between the remaining pads

Very low far end cross-talk because of lower capacitance between the pads in L5



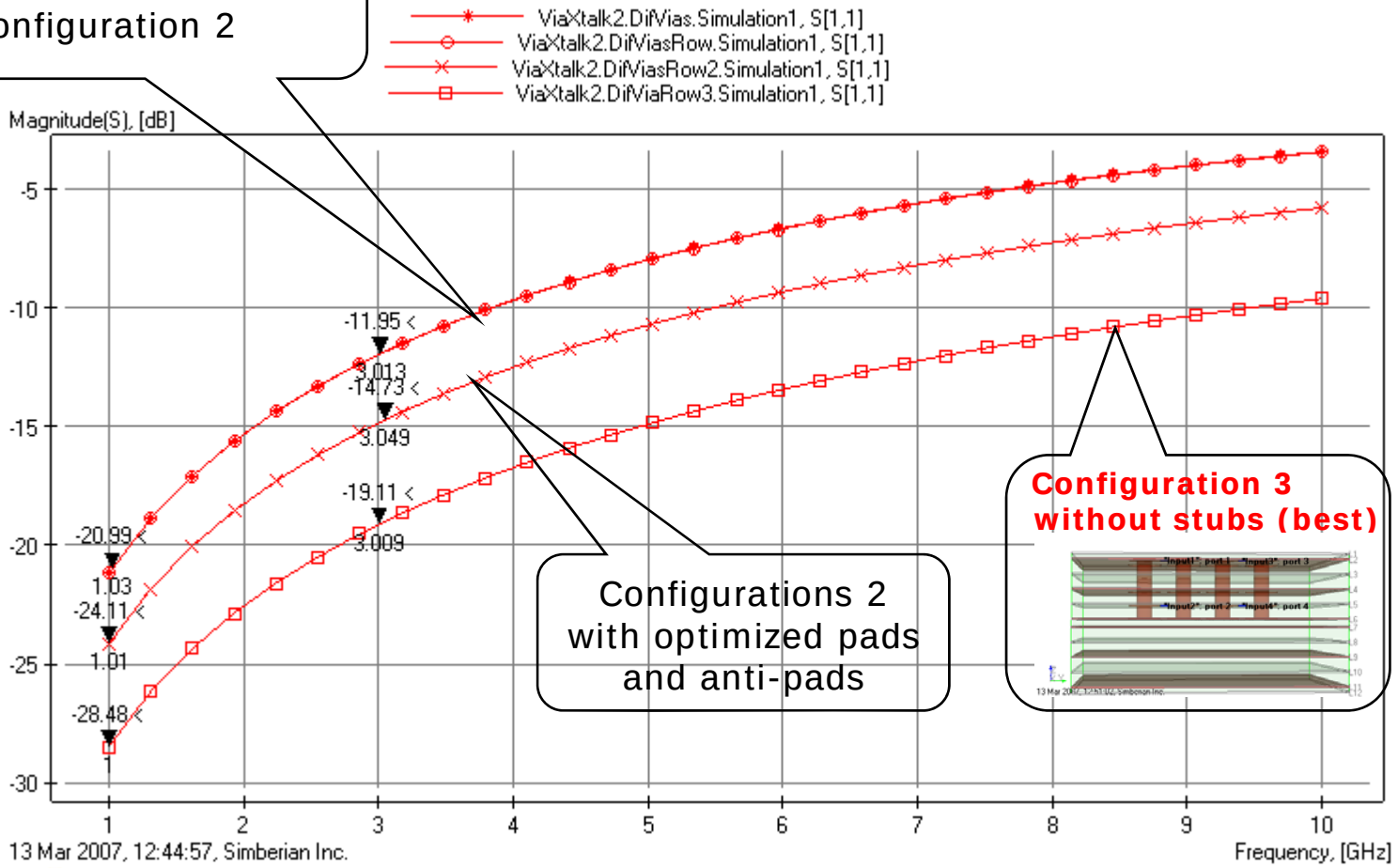
Comparison of all three configurations: Near-end crosstalk



Comparison of all three configurations: Reflection loss

Original side-by-side configuration 1 and vias in a row configuration 2

Configuration without stubs is the best out of 3 configurations but it is still not optimal above 3 GHz!



Solution and contacts

- Solution XViasOptimization.esx and project files, used to illustrate these notes, are available after installation of Simbeor 2007 in My Documents / Simbeor Solutions / PCB_MCM / XViasOptimization
- Send questions and comments to
  - General: info@simberian.com
  - Sales: sales@simberian.com
  - Support: support@simberian.com
- Web site www.simberian.com