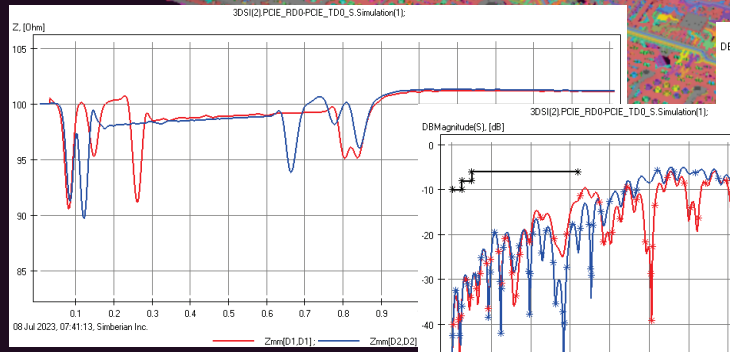
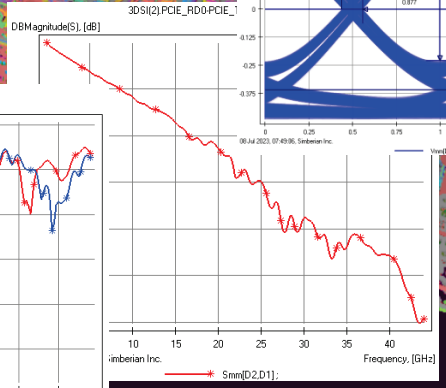
Simbeor - [Board Analyzer 2D: Project(1)-ERC]

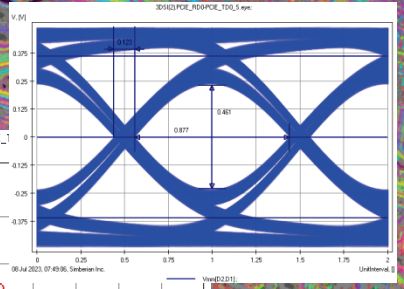
3D:Project(1)-3DSI | MultiVia(1) | MultiVia(2) | MPT(1) | MPT(2) | MPT(3) | 3DSI(1):PCIE_RD0-PCIE_TD0_S - RL | 3DSI(1):PCIE_RD0-PCIE_TD0_S - IL | 3DSI(1):PCIE_RD0-PCIE_TD0_S TDT | 3DSI(1):PCIE_RD0-PCIE_TD0_S

Simbeor

Electromagnetic Signal Integrity Software to Design Predictable PCB/Packaging Interconnects







Link/Net Browser

pcie_r

S	T	Net
☐		PCIE_RD0N
☐		PCIE_RD0P
☐		PCIE_RD1N
☐		PCIE_RD1P

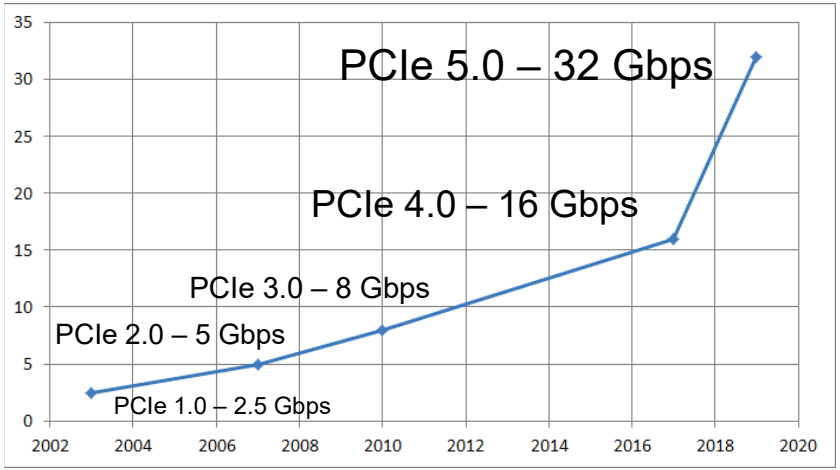
Clear Selection (Esc)

X,[?]: | Y,[?]: | Net: MAIN_CHASSIS_GND [825] | FPS: 11 (10807035,960) | License: Complete with all PCB translators

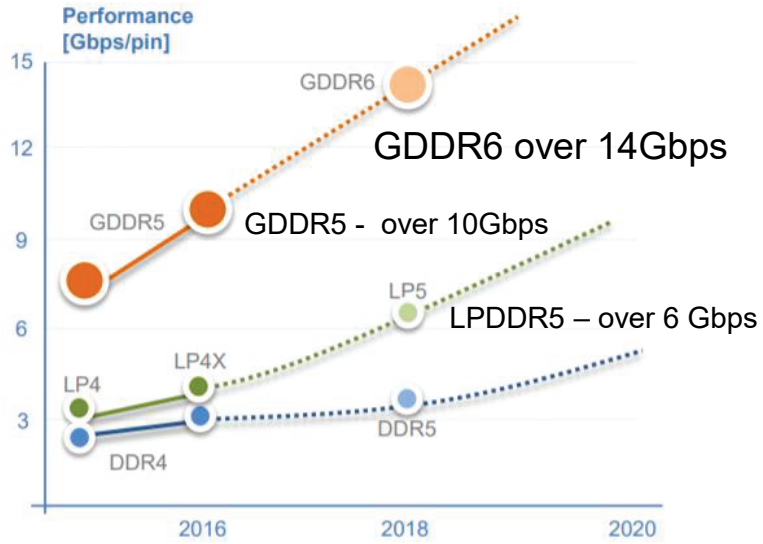
Data rates in consumer/communication electronics

PCI Express and DDR will probably dominate in all types of electronics;
Runners up: USB, Ethernet, SAS, InfiniBand, CEI…

Data rate per single link (Package/PCB)



Data rates double almost every 3 years
Around 1 billion devices will run on PCIe5 in 2-3 years
(M. Mazumder, Intel Corp. – DesignCon 2019)



[source : B. Koo, DesignCon 2019,
HOT Chips, SAMSUNG]

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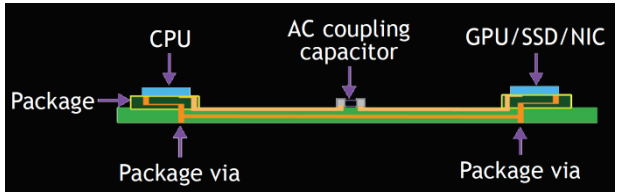
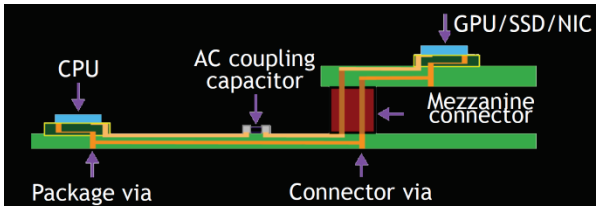
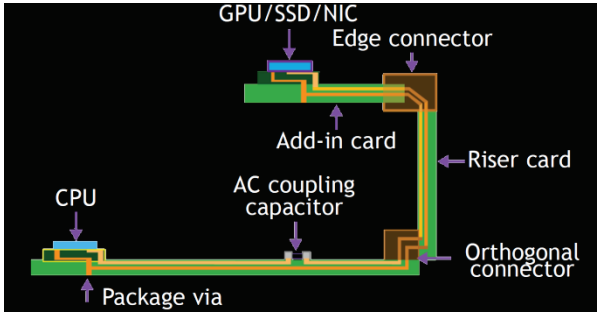
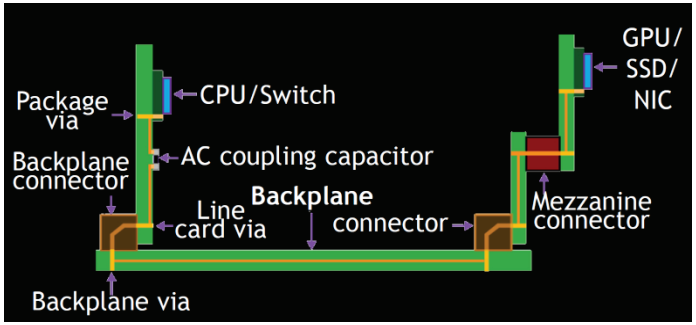
Typical PCIe Architectures









PCB design task: make sure that PCB interconnects and complete link satisfy compliance metrics for a particular standard (loss, reflections, crosstalk, mode conversion, COM, BER, ERL…)
It requires electromagnetic models for transmission lines and discontinuities

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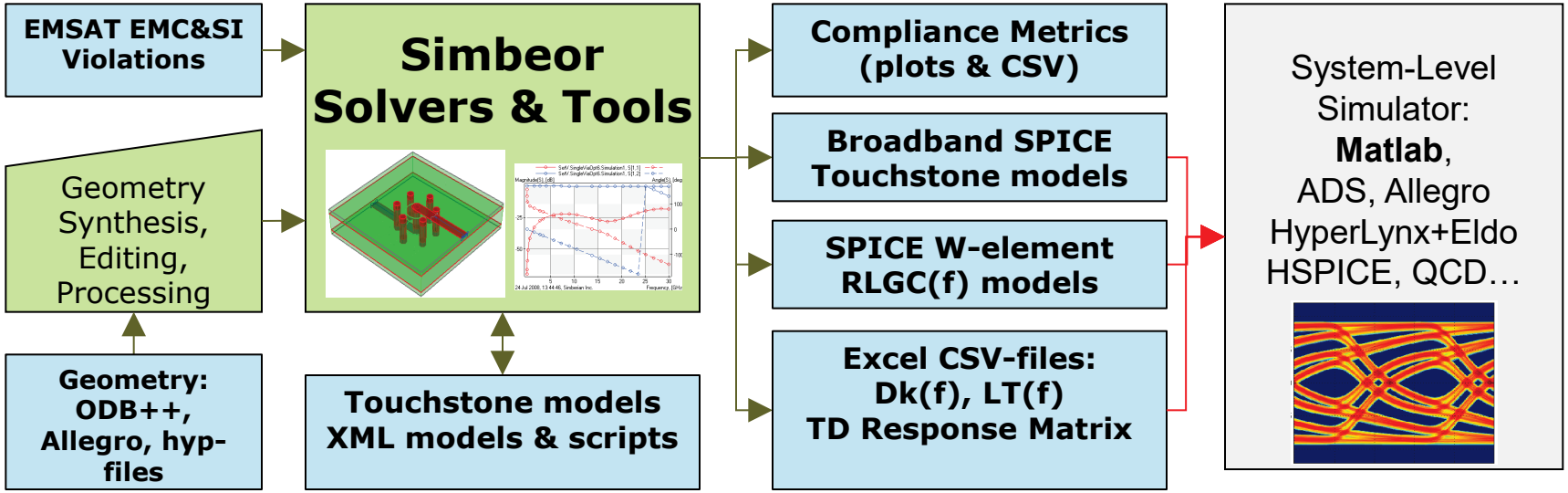
Simbeor is complete solution for ALL PCB/packaging interconnect design tasks

*Simbeor enables **geometry synthesis** for controlled impedance transmission lines and via-holes, has **geometry import** and selection capabilities, and **3D geometry editor***



Simbeor is one-stop solution for passive interconnect pre and post-layout analyses with advanced electromagnetic models, for macro-modeling and material parameters identification tasks, and de-embedding

All Simbeor technologies are now available in Simbeor SDK!

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Simbeor Applications

- Universal Signal Integrity Analysis
  - Simulation-based advanced Electrical Rule Checking (ERC)
  - Pre-layout and automated post-layout analysis with 3D EM models
  - S-parameters, Losses, Reflections, Crosstalk, TDR/TDT, Eye Diagram, Single Bit or Symbol Response (SBR or SSR), Pulse Response
  - Viaholes, component pads geometry and complete link tuning optimization
  - Dielectric and conductor roughness model identification
- SerDes Channel Design (Serial Interconnects)
  - Standard Compliance Metrics (SCM - IL, RL, ILD, PSXT, MDXT, ICR, ICN): Simbeor only
  - Channel Operating Margin (COM) – Simbeor with Matlab
  - Bit Error Rate (BER) with IBIS AMI – Simbeor with PyBERT, or Matlab + SI Toolkit, or ADS Core + HSD Ckt Sim, or HyperLinx LineSim + IBIS-AMI
- DDRx Interface Design (Parallel Interconnects)
  - Delay and Reflections: Simbeor only
  - Analysis with IBIS models: Simbeor with or Matlab + SI Toolkit, or ADS Core + Mem. Designer, HyperLynx LineSim

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Universal Signal Integrity Analysis

- Simulation-based advanced Electrical Rule Checking (ERC)
- Pre-layout analysis and optimization of viaholes, component pads and complete link
- Automated post-layout analysis with fast EM and 3D EM models
- S-parameters, Losses, Reflections, Crosstalk, TDR/TDT, Pulse Response, Single Bit or Symbol Response (SBR or SSR), Eye Diagram
- Solution space exploration and machine learning applications
- Dielectric and conductor roughness model identification, to have analysis to measurement correlation

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SerDes - Serial Interface

- Standard Compliance Metrics (SCM) – Simbeor Only
  - S-parameters, IL, RL, ILD, PSXT, MDXT, ICR, ICN
- Channel Operating Margin (COM) – Simbeor + Matlab
- Bit Error Rate (BER) with IBIS AMI – Simbeor + one of the following tools:
  - PyBERT (free);
  - **Matlab + Signal Integrity Toolkit (most comprehensive and cost-efficient);**
  - KeySight ADS Core + HSD Ckt Sim (most versatile);
  - Siemens HyperLinx LineSim with IBIS AMI;
  - Synopsys HSPICE

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DDRx - Memory Interface

- Delay and Reflections - Simbeor Only
- Analysis with IBIS models - Simbeor and one of the following tools:
  - **Matlab + Signal Integrity Toolkit (most comprehensive and cost-efficient);**
  - KeySight ADS Core + Memory Designer (most versatile);
  - Siemens HyperLinx LineSim;
  - Synopsys HSPICE

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Simbeor Main Advantages

- **Accurate** - ensured with validation projects – just some validation projects are published at www.simberian.com
- **Productive** – fast de-compositional EM analysis + domain decomposition + distributed computing
- **Easy to Use** – tools with integrated intuitive interface, well documented SDK with examples and multiple kits
- **Scalable** – interfaces to all components in C, Matlab, Python, post-layout automation with Lua
- **Embeddable** – SDK can be used in other tools and apps

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Simbeor Solvers and Algorithms

- **Simbeor SFS** – unique quasi-static field solver for large t-line cross-sections (any planar cross-section)
  - MoM, supports all dispersive isotropic material and roughness models
  - Used for S-parameters computation or creates Tabulated W-element models for transmission line
- **Simbeor 3DML** – full-wave 3D analysis tool for multi-layered geometries
  - Hybrid solver: Method of Lines + Trefftz Finite Elements + Method of Simultaneous Diagonalization (de-embedding)
  - Analysis of discontinuities and transmission lines with high-frequency (non-TEM) dispersion and anisotropy (any planar cross-section), interconnects with meshed planes
- **Simbeor 3DTF** – full-wave 3D analysis with Trefftz finite elements for discontinuities and non-TEM transmission lines, interconnects with meshed planes (high bandwidth memory applications), interconnects on ICs, PI problems,…
- **Simbeor 3DML and 3DTF** solvers are accelerated with domain decomposition and parallelized locally and with distributed computing (includes cloud computing framework)
- Fast EM solver for low-reflection via geometry synthesis or via delay evaluation (**fast via models** with infinite planes)
- **Linear Network Solvers** – unique port-based analysis
  - 7 solvers for FD and TD analysis of multiport networks based on Y or S-parameters – sparse solvers for extremely large networks
  - **Complete link analysis, material parameters identification, test fixture extraction and de-embedding capabilities**
- **Rational Compactor** – converts discrete S-parameter models into frequency-continuous rational macro-models – generate BB SPICE models for any network described with S-parameters
- **Copper Helper** – set of proprietary algorithms for fast PCB/packaging geometry processing, visualization and SI/PI model building (multiple orders of magnitude faster then any commercial analog)

All solvers and algorithms are available in Simbeor THz as well as in Simbeor SDK!

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Simbeor Tools

- **Touchstone Analyzer™** – S-parameters plotting, quality assurance and macro-modeling (available in SDK)
- **Transmission line wizard** – fast synthesis of any single-ended and differential line geometry (strip, micro-strip, CPW, CBCPW,…, available in SDK)
- **Via Analyzer™** – fast synthesis of via-holes and launches geometry (available in SDK)
- **Multi-layered Geometry Editor** for pre and post-layout analyses
- **Linear Network Editor** to draw multiport networks (link path models)
- **SiTune™** – via, t-line geometry, linear network optimization, material model identification (available in SDK)
- **Eye Analyzer™** - measurements on eye diagram (available in SDK)
- **ICN Analyzer™** - for Integrated Cross-talk Noise (ICN) computation (available in SDK)
- **Board Analyzer™** - tools for unique post-layout de-compositional electromagnetic analysis
  - **DeComposer™** - automatic decomposition for post-layout analysis of coupled and skewed links into t-lines and discontinuities with precise handling of reference discontinuities
  - **SI Compliance Analyzer™** - unified interface for model-based ERC, Fast SI and 3D SI analyses
- **Violation Browser™** - viewer for ERC violations from SI Compliance Analzyer and EMSAT (IBM) rule checkers
- **SPP Analyzer™** – material model identification with TDT or short pulse measurements (IBM)
- **T-Resonator Analyzer™** – extraction of loss tangent with T-resonator (available in SDK)
- **SDK Kits for Matlab** – AdvMaterialKit, MLKit, TLineKit, SIPlotKit, ViaDevKit, AdvXTalkKit, FEW_Kit, AdvViaKit…

All tools are integrated in Simbeor THz and all are available in Simbeor SDK (except BA)!

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Simbeor SI Compliance Analyzer

- **Unique one-stop solution for all compliance validation needs**
- Electrical Rule Checking: 2D Field Solver + Fast Via Models
  - Model-based SI link defect checking – localization, reference and impedance continuity, crosstalk
  - Interactive analysis of links in fraction of a second or thousands of links with automation
- Fast SI: De-composition + 2D Field Solver + Fast Via Models
  - Basic signal integrity analysis: crosstalk, losses, delay and skew for slow signals (<10 Gpbs, >100 ps rise time)
  - Interactive analysis of links in seconds or hundreds of links with automation
- 3D SI – De-composition + Field Solver (2D or 3D) + 3D Full Wave EM
  - Advanced Signal Integrity Analysis of PCB/Packaging Interconnects (unlimited data rates, accuracy depends on geometry, materials and link localization)
  - Interactive analysis of links in minutes or hundreds of links with automation

All types of analyses are automated in Simbeor THz with Lua and interface to Matlab and Python!

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Simbeor SDK

- Simbeor SDK is dynamic link libraries with API in C language for programming or scripting in C/C++, Matlab and Python
- It provides access to all Simbeor solvers and all tools, except Board Analyzer, and can be used for…
  - **material model identification** – single case or extraction of statistical models
  - **design automation** – scripted EM analysis, geometry synthesis, complete link analysis…
  - **machine learning** – training or complimenting machine learning algorithms…
  - **integration into other EDA tools** (such as Stack Manager in Altium Designer)

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Typical Use of Simbeor

- **Dielectric and conductor roughness** model identification (4 methods) – to ensure accuracy of interconnect analysis
- **Pre-layout de-compositional electromagnetic analysis** or PCB/packaging interconnects
  - Stackup design – t-line synthesis/analysis for all PCB/packaging applications (no restriction)
  - Viahole design for low-speed applications (based on fast EM solver, coming up)
  - Broadband viahole optimization for serial or point-to-point links (use of 3DML and 3TDF solvers and optimization, coming up)
  - Impedance, loss, mode conversion, reflection (vias) and cross-talk control during layout process

- **Automatic post-layout de-compositional electromagnetic analysis** or PCB/packaging interconnects – the Holy Grail of the post-layout analysis
  - Complete link analysis: S-parameters, compliance metrics, TDR/TDT, eye diagrams, pulse response
- **Post-layout analysis automation with Lua**, to ensure compliance and consistency of design iteration (new in Simbeor 2022.03)
- **Scripting in C/C++/Matlab/python** for pre-layout design automation, material identification and machine learning

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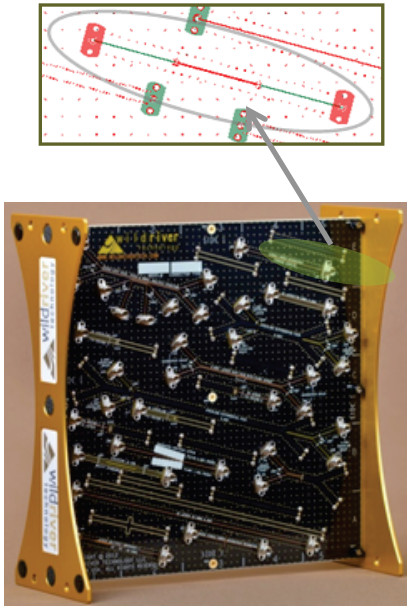
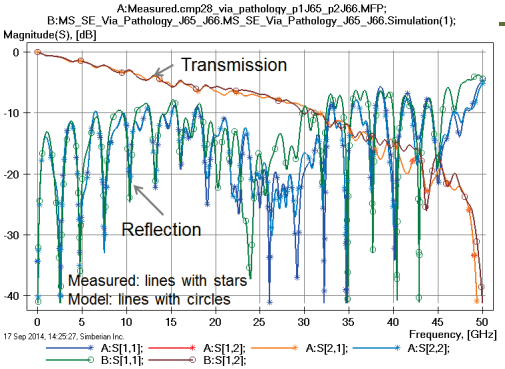
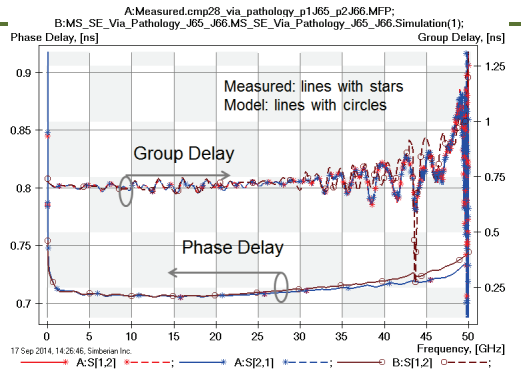
Simbeor is formally validated up to 50 GHz

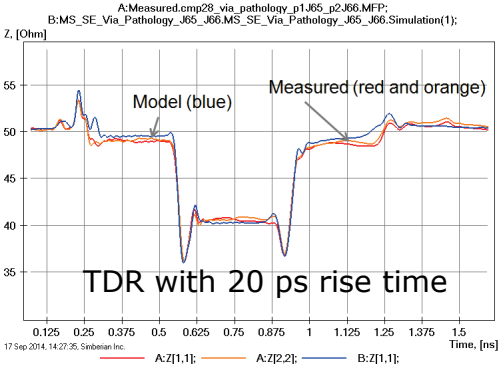
EXAMPLE

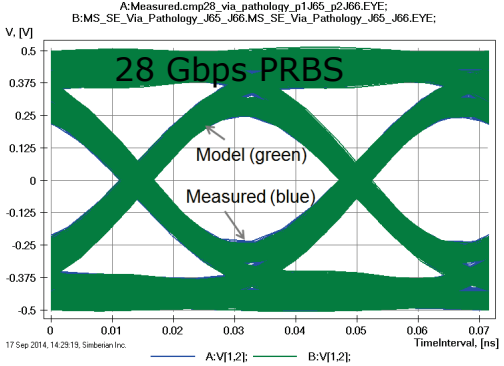


CMP-28 Channel Validation Platform from Wild River Technology LLC









See Webinar #4. Complete description of CMP-28/32 platforms with all results is available at **http://www.simberian.com/Presentations/CMP-28_Simbeor_Kit_Guide.pdf**

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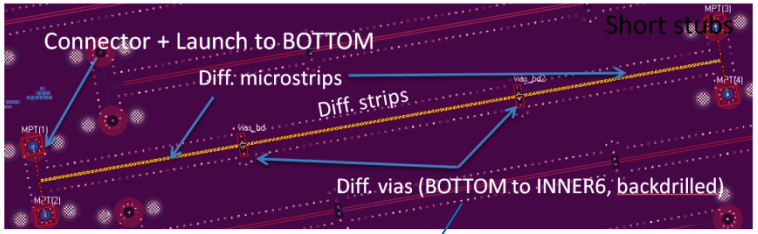
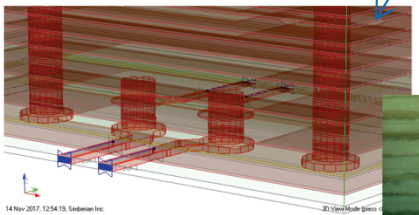
Example of systematic validation with EvR-1 test board from Infinera

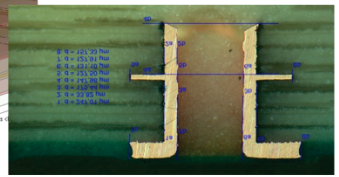
1.1 in microstrips – vias – 1.5 in strips – vias – 1.1 in microstrips

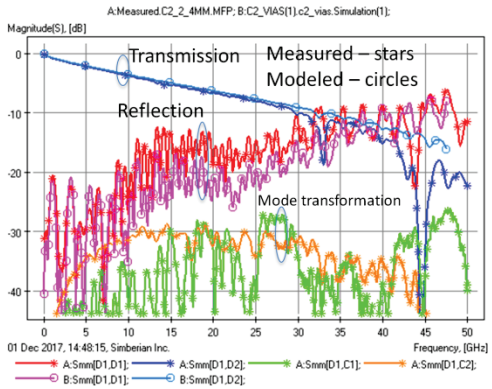


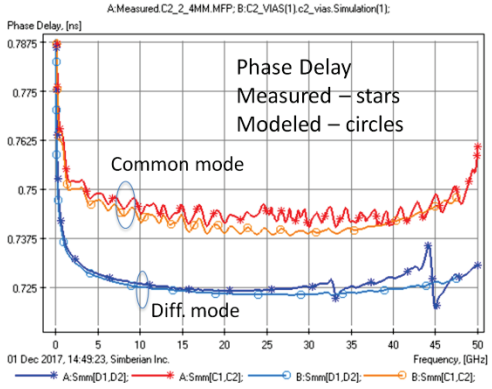
Backdrilled vias model

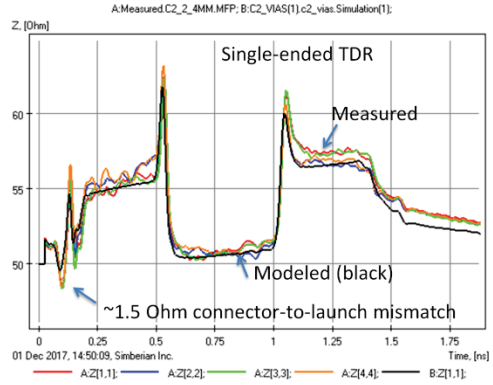


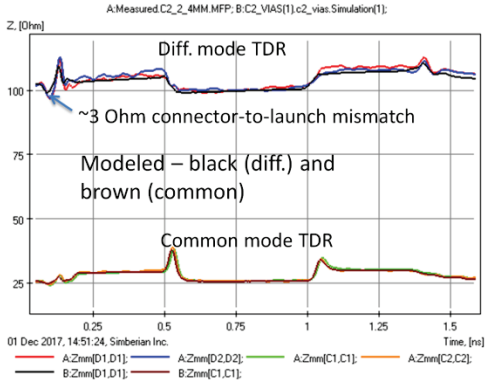
De-compositional EM analysis
Shape and size of all traces and backdrilling position are adjusted…











Complete report #2018_01 at
http://www.simberian.com/AppNotes.php

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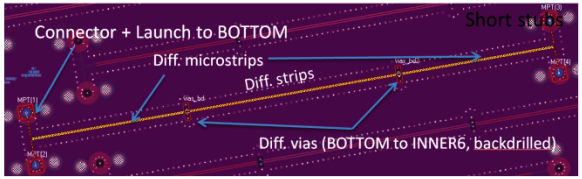
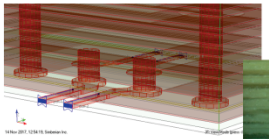
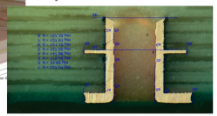
28 Gbps NRZ, PRBS-32, 15 ps rise time

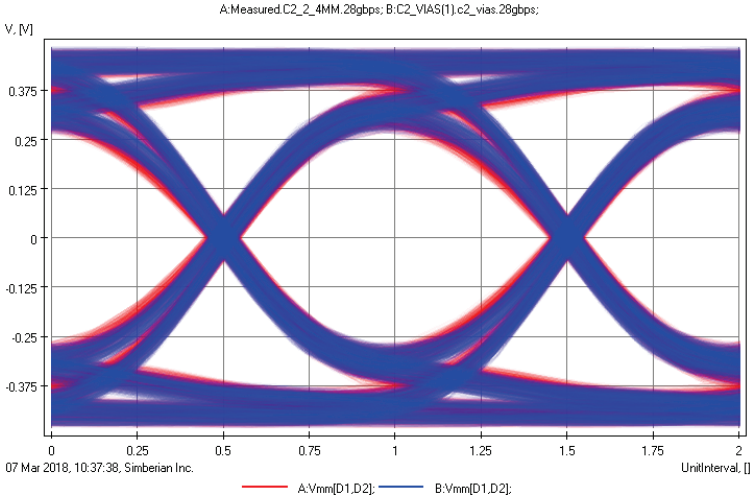


Backdrilled vias model



De-compositional EM analysis
Shape and size of all traces and backdrilling position are adjusted…





Eye Analyzer

Show Eye Metrics: Selected Auto-open

Parameter	Measured.C2_2_4M...	C2_VIAS(1).c2_vias....
Eye Level Zero (V)	-0.370953	-0.373448
Eye Level One (V)	0.371227	0.375322
Eye Level Mean (V)	-8.25219e-005	0.00123696
Eye Amplitude (V)	0.74218	0.74877
Eye Height (V)	0.504704	0.526895
Eye Width (UI)	0.883814	0.898891
Eye Opening Factor	0.680029	0.703681
Eye Signal to Noise	6.45773	6.10486
Eye Rise Time (20-80) (UI)	0.459316	0.42801
Eye Fall Time (80-20) (UI)	0.460037	0.427404
Eye Jitter (PP) (UI)	0.116186	0.101109
Eye Jitter (RMS) (UI)	0.0279181	0.0240858

28 Gbps NRZ: model – blue, measured – red; 5.5% difference in eye heights and 1.5% in heights

EvR-1 test board – see complete report at Complete report #2018_01 at http://www.simberian.com/AppNotes.php

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Why use Simbeor?

- Provides systematic “sink or swim” approach to design predictable interconnects
- Algorithms are systematically validated with measurements up to 50 GHz!
- Unique algorithms for material models identification – must be the basis of systematic approach to design predictable interconnects
- Advanced and verifiably accurate models of transmission lines
- Unique EM models for flexible interconnects and periodic structures
- Unique macro-modeling capabilities for consistent FD and TD analyses of networks with t-lines and S-parameter models (seamless FD<->TD analyses)
- Unique de-embedding capabilities (part of LNS)
- Advanced and verifiably accurate models of discontinuities (vias, pins,…)
- Unique de-compositional capabilities for chip-to-chip link analysis (no artifacts on the boundaries)

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Simberian
Electromagnetic Solutions

Simbeor THz

Electromagnetic Signal Integrity Software to Design Predictable PCB/Packaging Interconnects

To learn more, visit www.simberian.com

Be The SI Expert™