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DesignCon® 2020

WHERE THE CHIP MEETS THE BOARD

Conference
January 28 - 30, 2020

Expo
January 29 - 30, 2020

Santa Clara Convention Center

Design insights from electromagnetic analysis and measurements of PCB and Package interconnects operating at 6-112 Gbps and beyond

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DesignCon2020, Santa Clara Convention Center
January 28, 1:30pm - 4:30pm, Ballroom C

Outline

- Introduction
- Bandwidth for modeling and measurements
- Major signal degradation factors
- Analysis of interconnects
- Design of predictable interconnects
- Design insights from signal integrity practitioner
- Limits on PCB interconnects
- Conclusion

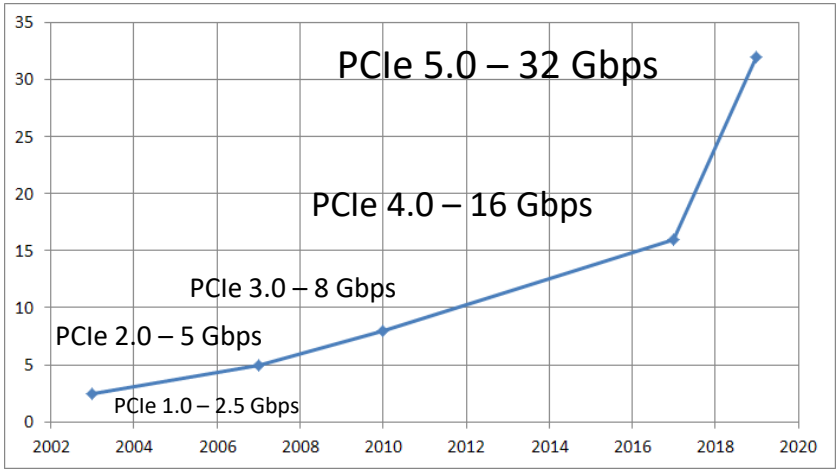
Introduction

- What does it take to design predictable PCB/packaging interconnects operating at 6-112 Gbps? – design interconnects that behave as expected?
- Can we use design processes and practices adopted at lower data rates? - use approach that worked at 1-3 Gbps to 10-30 Gpbs for instance?
- Can we achieve the first pass design success and what does it take to do it?
- What signal degradation factors have to be accurately predicted and at which data rate they become important?
- This presentation is just introduction into design of predictable interconnects for increasingly growing data rates…

Data rates in consumer/communication electronics are rapidly increasing!

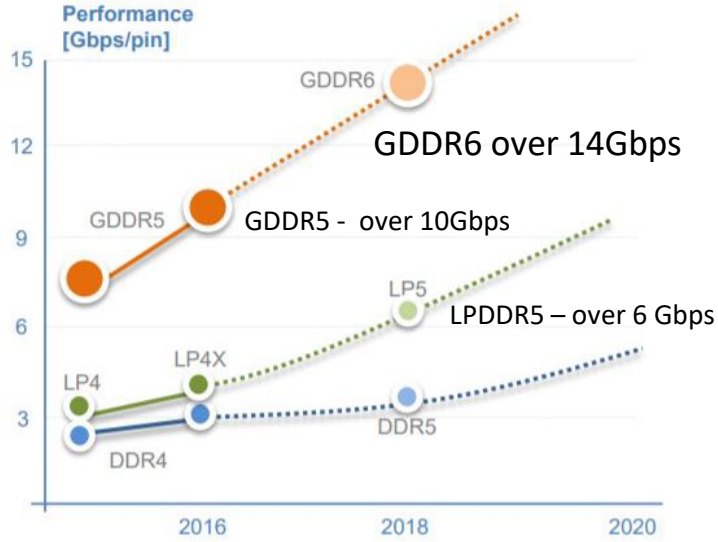
More data through Ethernet, USB, SAS, InfiniBand, CEI…
Ethernet IEEE 802.3ck group works on 112 Gbps over PCB&cable

Data rate per single link (Package/PCB)



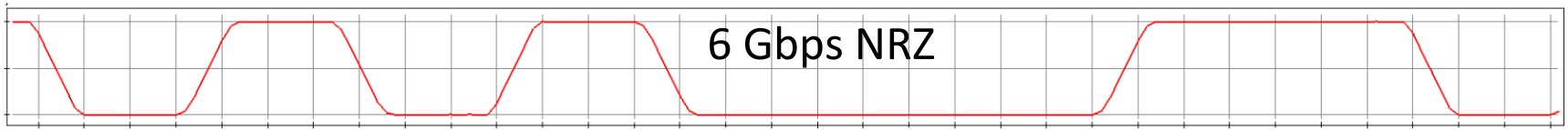
PCIe data rate double almost every 3 years
Around 1 billion devices will run on PCIe5 in 2-3 years
(M. Mazumder, Intel Corp. – DesignCon 2019)

Validated EM models required starting from 3-5 Gbps!



[source : B. Koo, DesignCon 2019, HOT Chips, SAMSUNG]

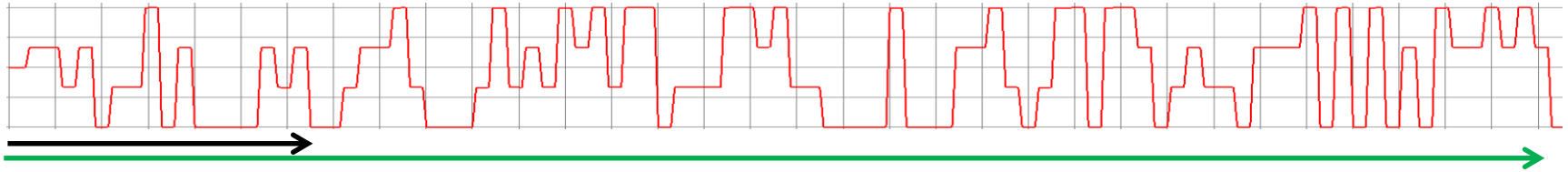
PCB and package scale in bits or symbols from 6 to 112



~2 symbols in packaging interconnects

~10 bits in PCB interconnects

112 Gbps PAM4



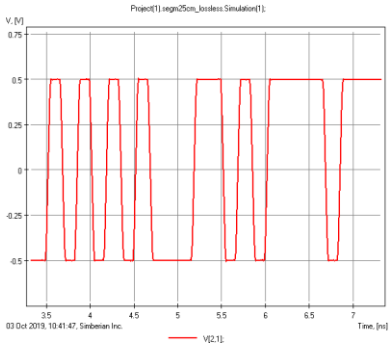
~20 symbols in packaging interconnects

~100 symbols in PCB interconnects

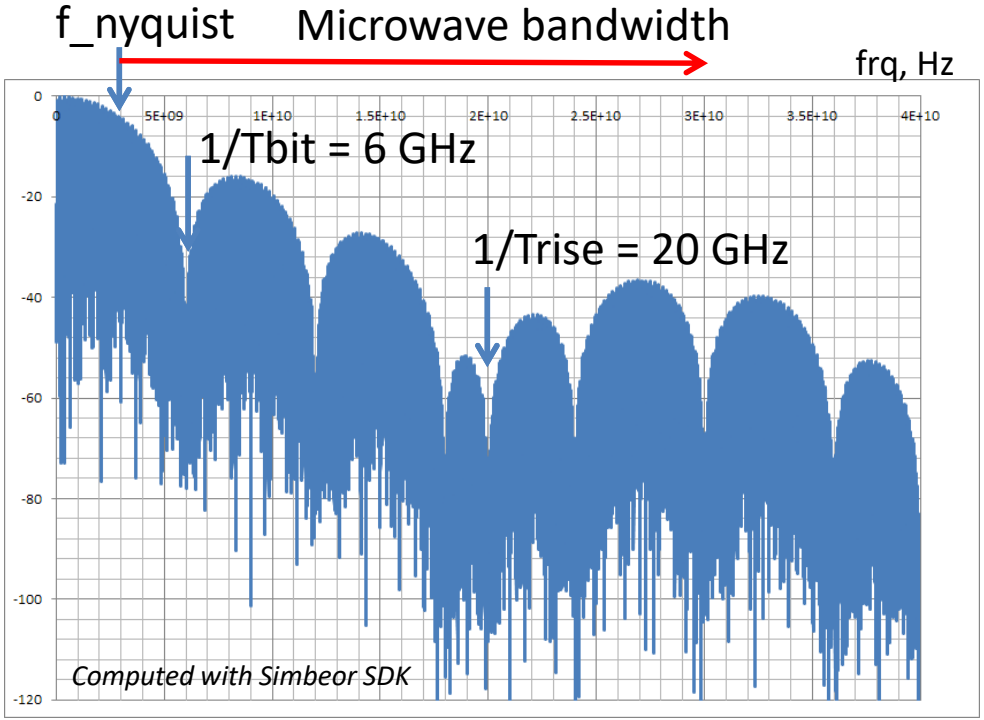
Time-domain signals are simulated in frequency domain…

6 Gbps NRZ signal spectrum

6 Gbps: Trise=50ps;
Tbit=166.6667ps;
f_nyquist = 3 GHz



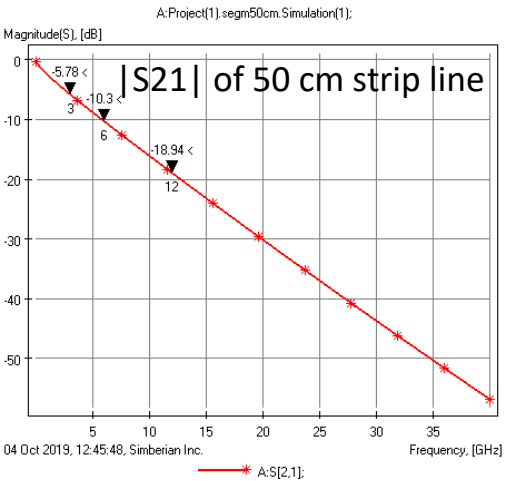
PSD of
PRBS7

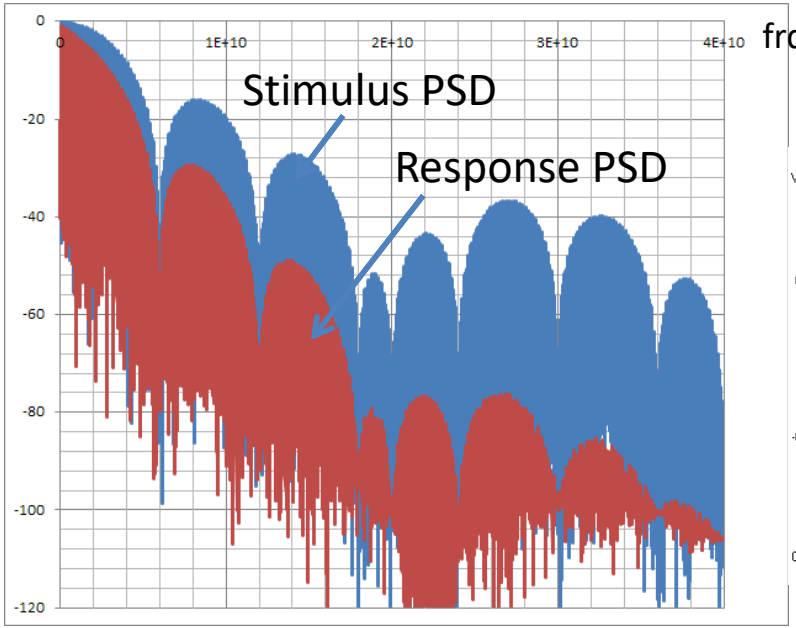


What is bandwidth?
0.5/Trise? 1/Trise?

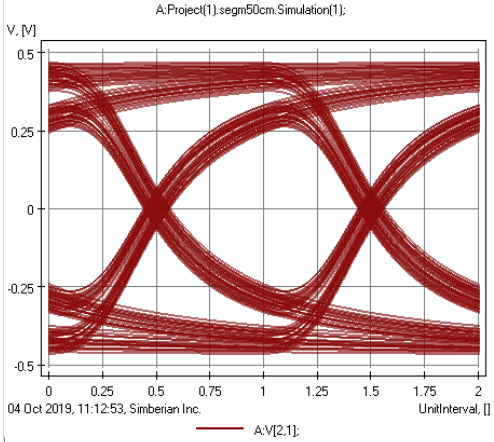
Getting through interconnects at 6 Gbps

FR408 – Wideband Debye: Dk=3.8, LT=0.0117 @ 1 GHz
Copper: RR=1.2, Causal Hammerstad Roughness Model: SR=0.4, RF=2





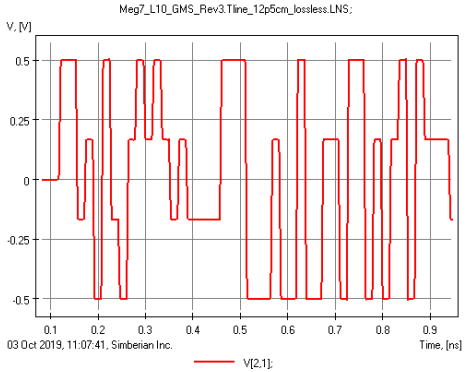
Distorted response



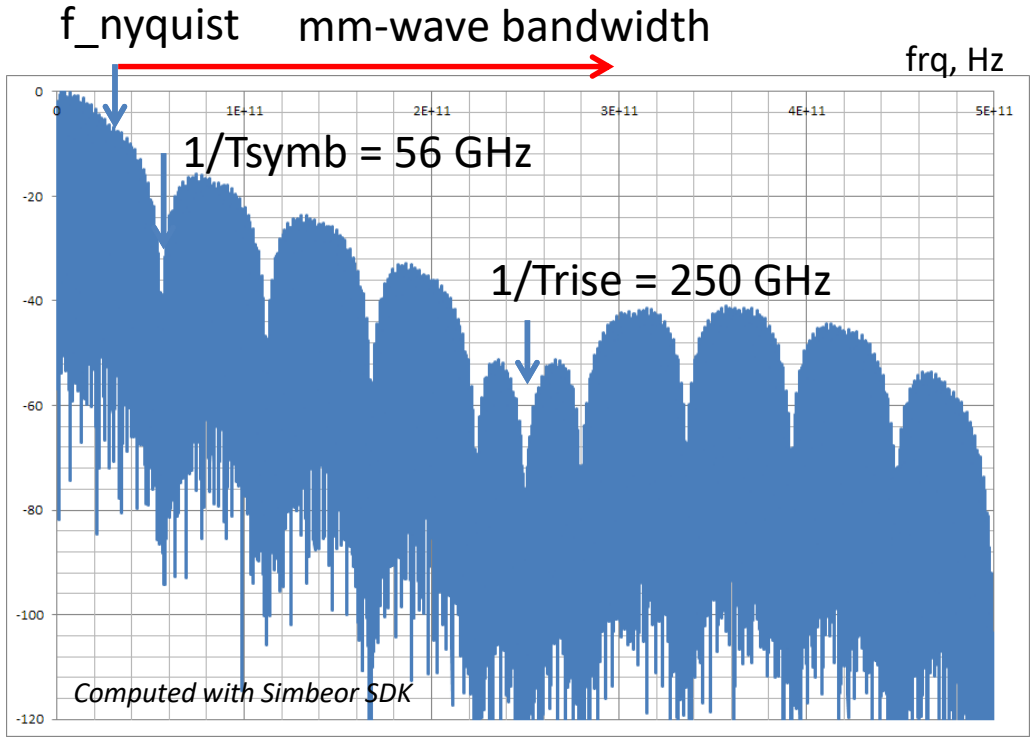
High-frequency harmonics are reduced – it reduces the bandwidth…

112 Gbps PAM4 signal spectrum

112 Gbps: Trise=4ps;
Tsymb=17.8571ps;
f_nyquist = 28 GHz



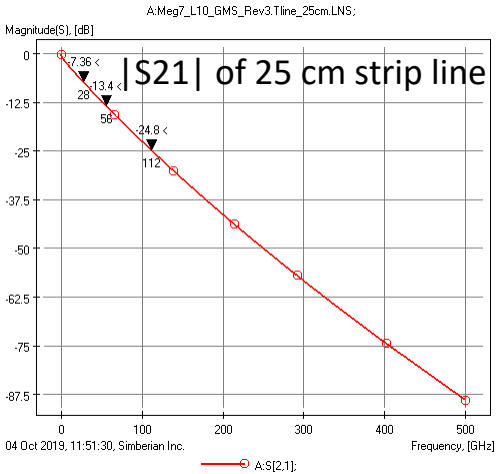
PSD of PRBS7

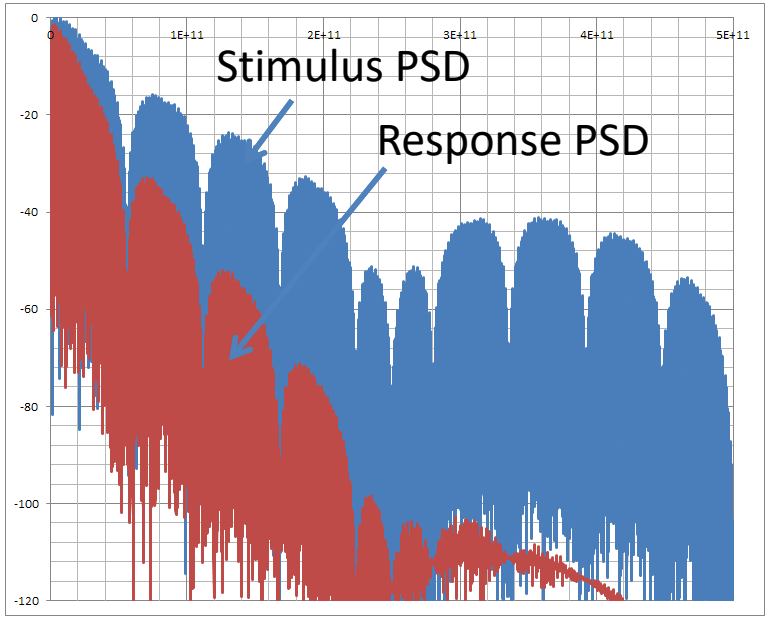


What is the bandwidth?
0.5/Trise looks unrealistic…

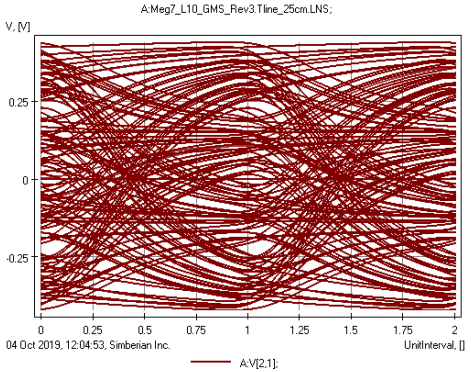
Getting through interconnects at 112 Gbps

Meg7 – Wideband Debye: Dk=3.17, LT=0.0011 @ 1 GHz
Copper: RR=1.4, Roughness – Huray-Bracken Model: SR=0.14 um, RF=8.7





Additional signal conditioning is required!

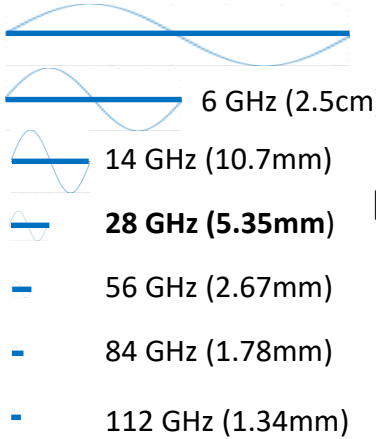


High-frequency harmonics are reduced – it reduces bandwidth and may kill the signal..

PCB and package scale in wavelengths

Package (~10 WL @28 GHz, ~40 WL @112 GHz)

PCB (~50*WL @ 28 GHz, ~200*WL @ 112 GHz)



3 GHz

6 GHz (2.5cm)

14 GHz (10.7mm)

28 GHz (5.35mm)

56 GHz (2.67mm)

84 GHz (1.78mm)

112 GHz (1.34mm)

Dk=4

Frequency [GHz]	WL Air [mm]	WL [mm]	WL/2 [mm]	WL/4 [mm]	WL/8 [mm]
3	**99.931**	**49.965**	**24.983**	**12.491**	**6.246**
6	49.965	24.983	12.491	6.246	3.123
14	21.414	10.707	5.353	2.677	1.338
28	**10.707**	**5.353**	**2.677**	**1.338**	**0.669**
56	5.353	2.677	1.338	0.669	0.335
84	3.569	1.784	0.892	0.446	0.223
112	2.677	1.338	0.669	0.335	0.167

1 mm = 39.37008 mil

1 mil = 0.0254 mm

WL is wavelength in dielectric $\lambda = \frac{c}{f \cdot \sqrt{\varepsilon_r}}$

Design Limits:

WL/2 - cutoff for SIW formed by via fences, resonances;

WL/4 - resonances, via localization (pass/fail);

WL/8 – via fence shielding;

We are deep into microwave and mm-wave territory

Waveguide Domain ruled by the Electromagnetic Analysis!

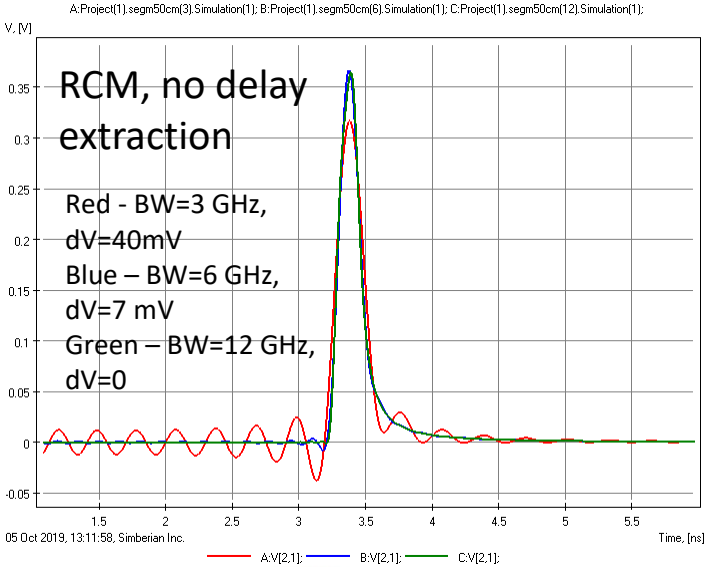
Bandwidth for simulation or measurement…

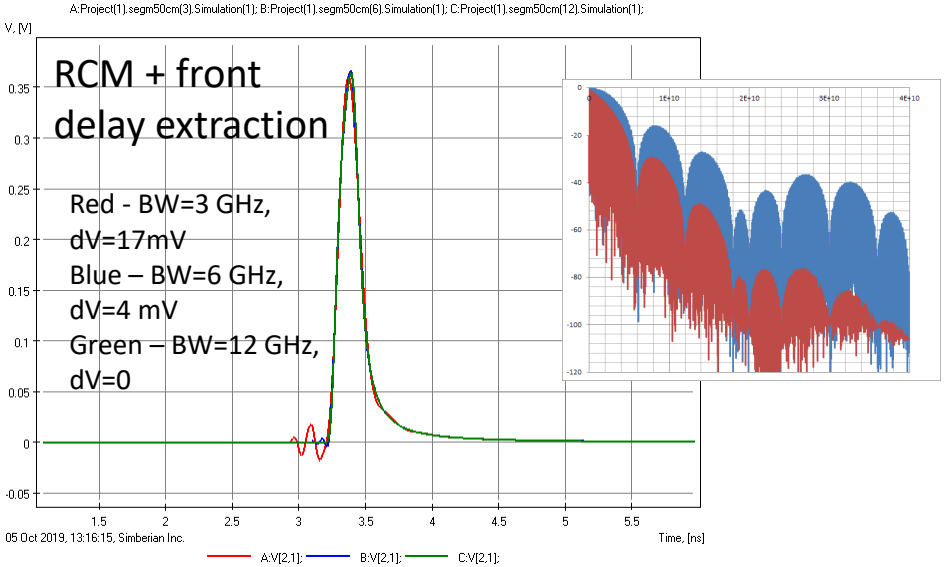
- Defined by signal source spectrum (may be measured)
- Reduced by expected channel insertion loss (it includes all kinds of losses - thermal, reflections, leaks)
- Must be adjusted to account for possible coupling spectrum (NEXT, multipath propagation,…)
- No universal formula - should be defined on case by case basis
- Possible way is a numerical experiment…

Use of single bit response for 6 Gbps NRZ bandwidth (BW) estimation

Test case: About 50 Ohm strip line – almost no reflections
FR408 – Wideband Debye: Dk=3.8, LT=0.0117 @ 1 GHz
Copper: RR=1.2, Causal Hammerstad Roughness Model: SR=0.4, RF=2

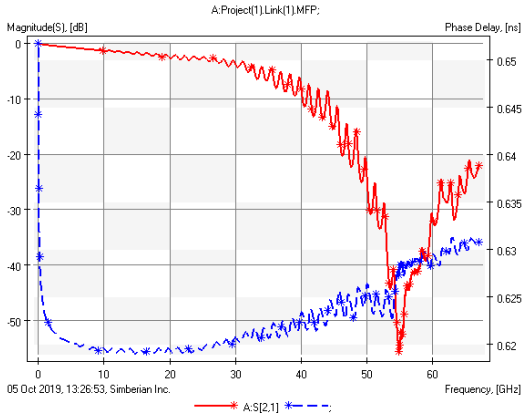
Will also depend on the EDA tool!!!

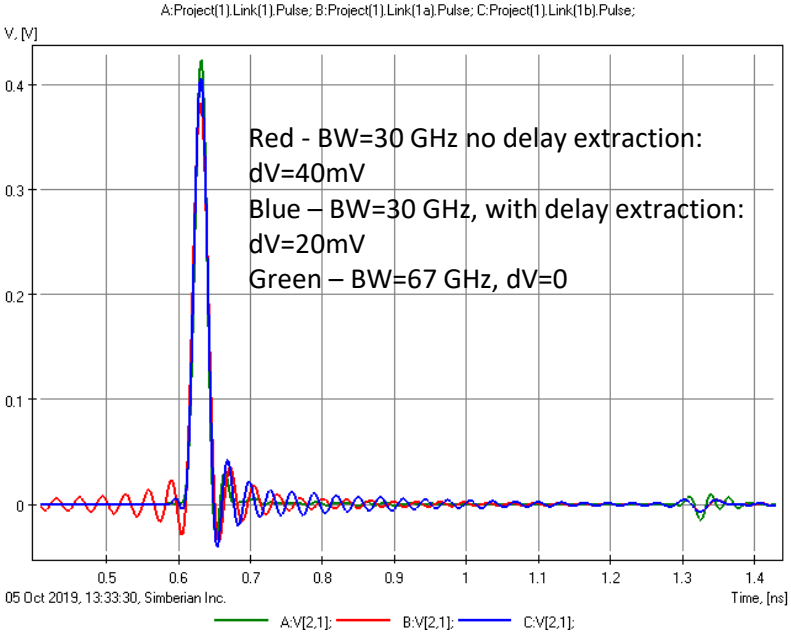


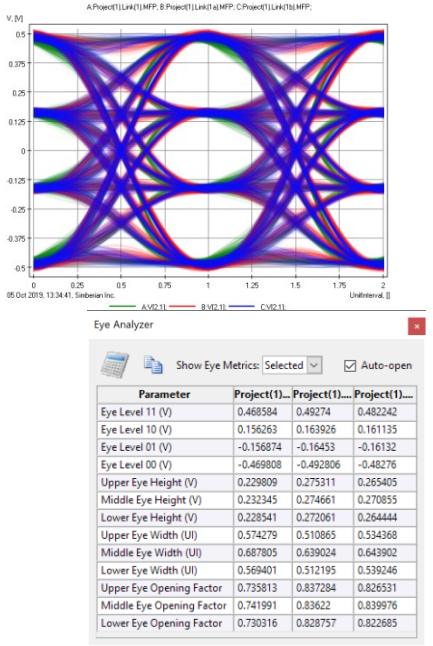


Use of single symbol response for 112 Gbps PAM4 bandwidth (BW) estimation

Test case: 5 cm of strip line on Meg7 with two vias with stubs
S-parameters measured up to 67 GHz







Parameter	Project(1)...	Project(1)....	Project(1)....
Eye Level 11 (V)	0.468584	0.49274	0.482242
Eye Level 10 (V)	0.156263	0.163926	0.161135
Eye Level 01 (V)	-0.156874	-0.16453	-0.16132
Eye Level 00 (V)	-0.469808	-0.492806	-0.48276
Upper Eye Height (V)	0.229809	0.275311	0.265405
Middle Eye Height (V)	0.232345	0.274661	0.270855
Lower Eye Height (V)	0.228541	0.272061	0.264444
Upper Eye Width (UI)	0.574279	0.510865	0.534368
Middle Eye Width (UI)	0.687805	0.639024	0.643902
Lower Eye Width (UI)	0.569401	0.512195	0.539246
Upper Eye Opening Factor	0.735813	0.837284	0.826531
Middle Eye Opening Factor	0.741991	0.83622	0.839976
Lower Eye Opening Factor	0.730316	0.828757	0.822685

Major Signal Degradation Factors

Thermal losses

Reflections

Couplings

Major signal degradation factors

- **Thermal losses**
  - Dielectric polarization loss and dispersion
  - Conductor resistivity and surface roughness loss and dispersion
- **Reflections**
  - Trace/transmission line impedance mismatch
  - Single discontinuities – vias, transitions, AC caps, gaps in reference plane…
  - Periodic discontinuities – cut outs, fiber-weave effect,…
- **Couplings**
  - Crosstalk – interference and leaks
  - Via localization breakout – leaks and interference
  - Couplings through discontinuities in reference planes
  - Modal transformations in diff. pairs (aka skew)
  - Multipath propagation, radiation, EMI, EMC,…

What effects are important at a particular data rate?

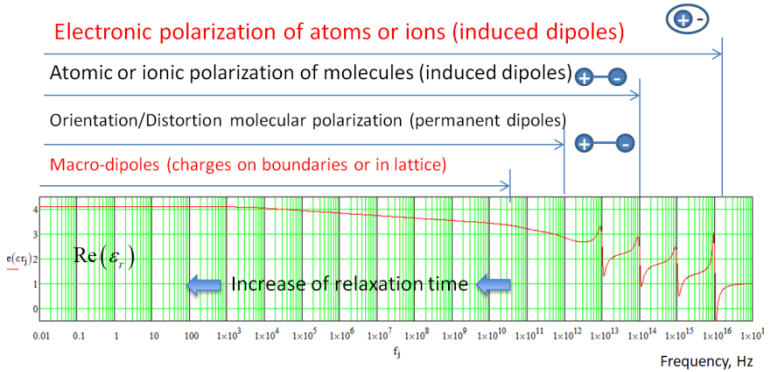
Are they accounted for by signal integrity software?

Are they all included into electromagnetic software?

If all effects are included, will model correlate with measurements?

Thermal losses – energy absorbed by materials

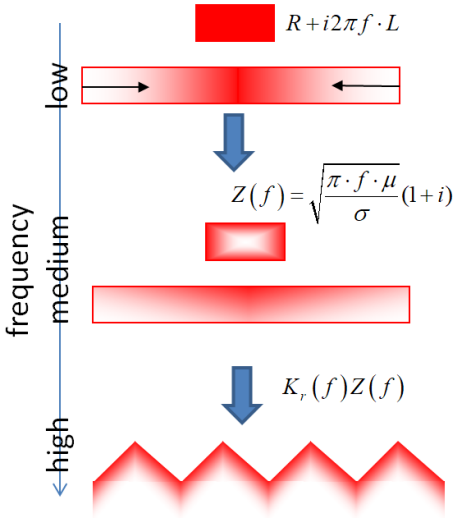
Dielectric polarization losses



All thermal losses are included into transmission S-parameter (S21, SDD21,… insertion loss)

See more in Material World… tutorial - #2016_01 at Technical presentations

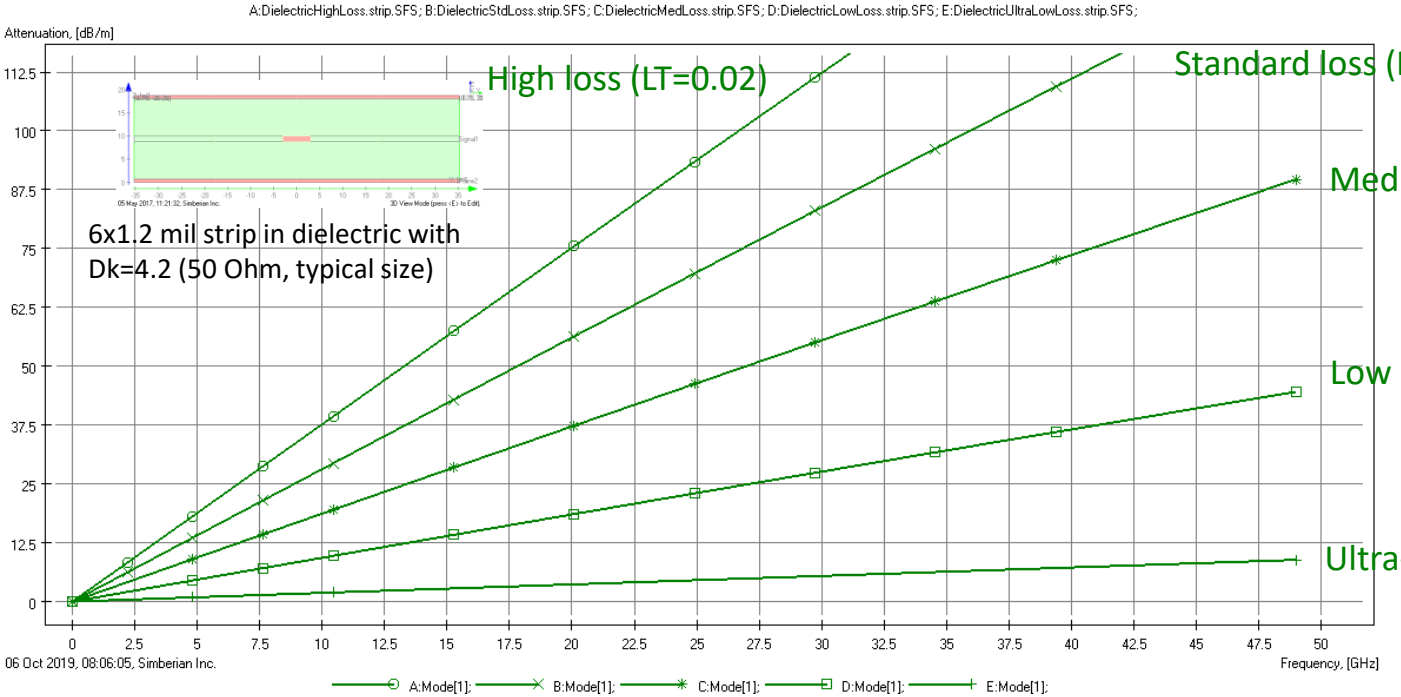
Conductor losses – resistivity and roughness



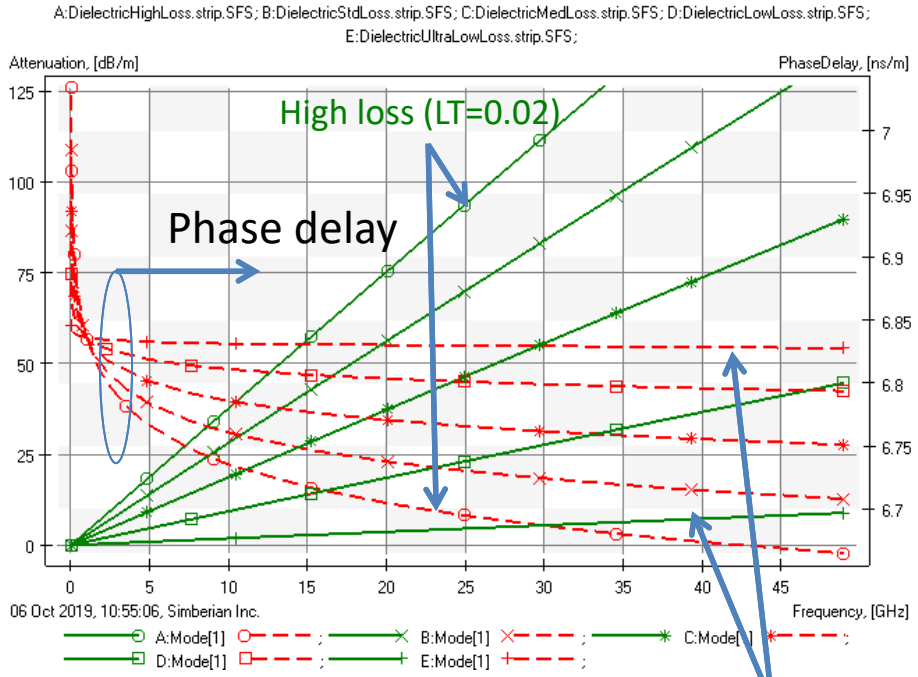
Resonant absorption in Nickel (about 2.7 GHz)

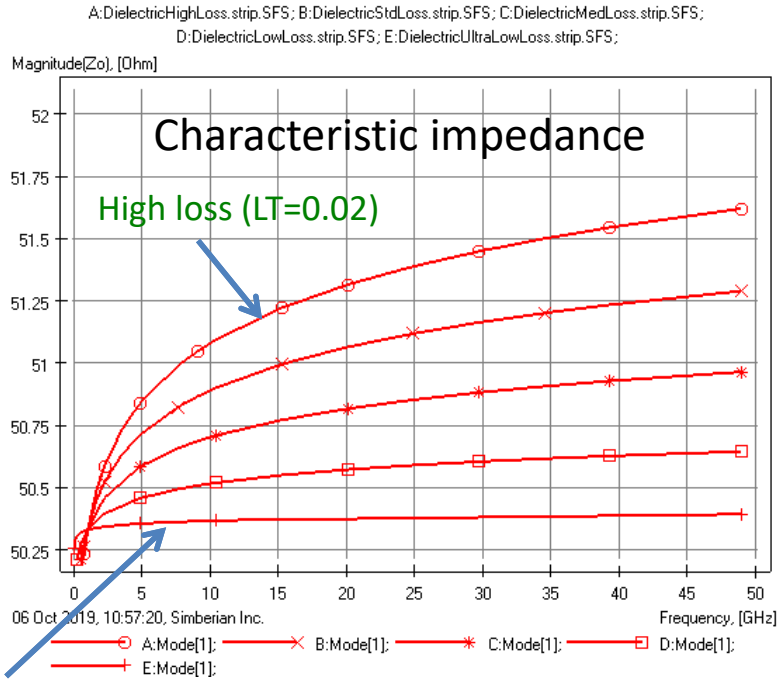
Dielectric polarization losses

Approximately linear growth with frequency



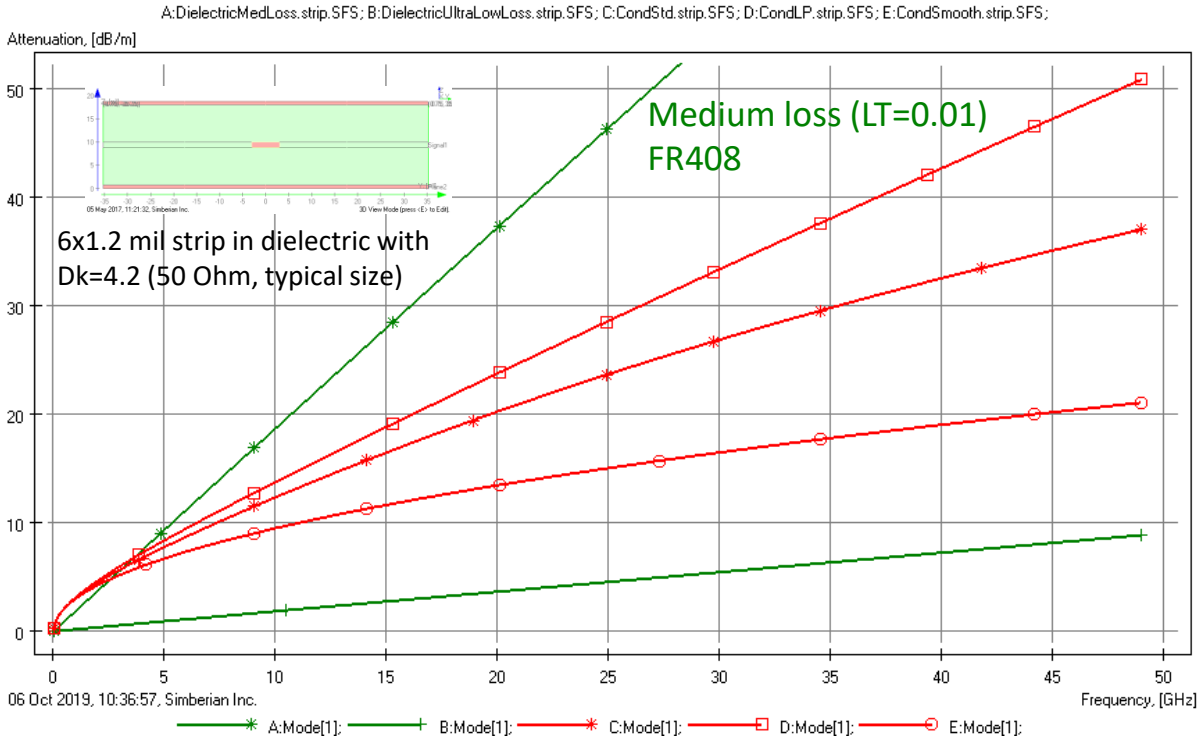
Lossy dielectrics change delay and impedance (causality)





Ultra-Low loss (LT=0.001)

Conductor losses



Copper with HVLP surface,
SR=0.14um, RF=8.7

Copper with STD/RTF surface,
SR=0.4um, RF=2

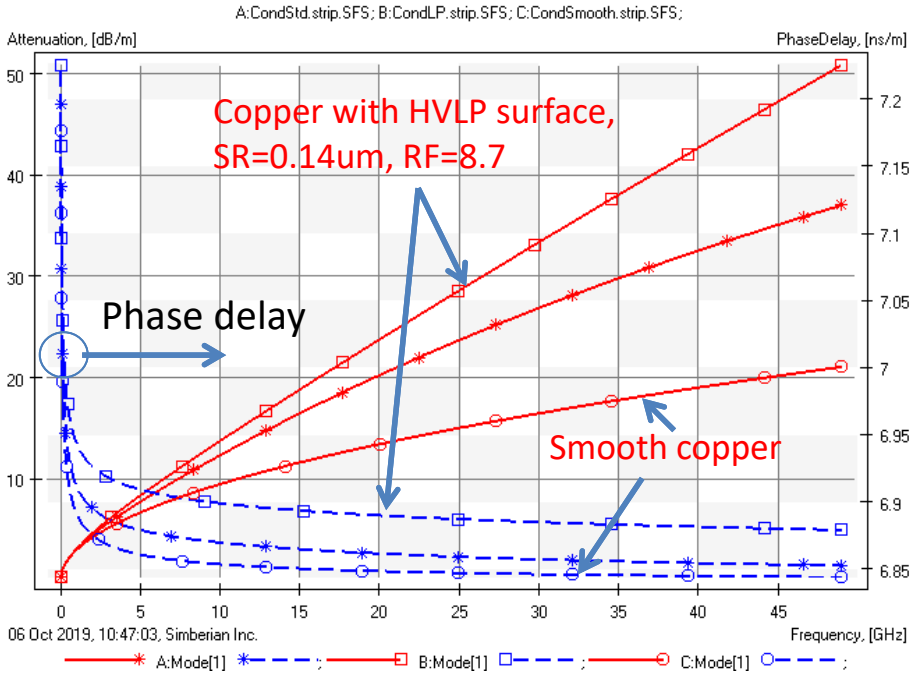
Smooth copper

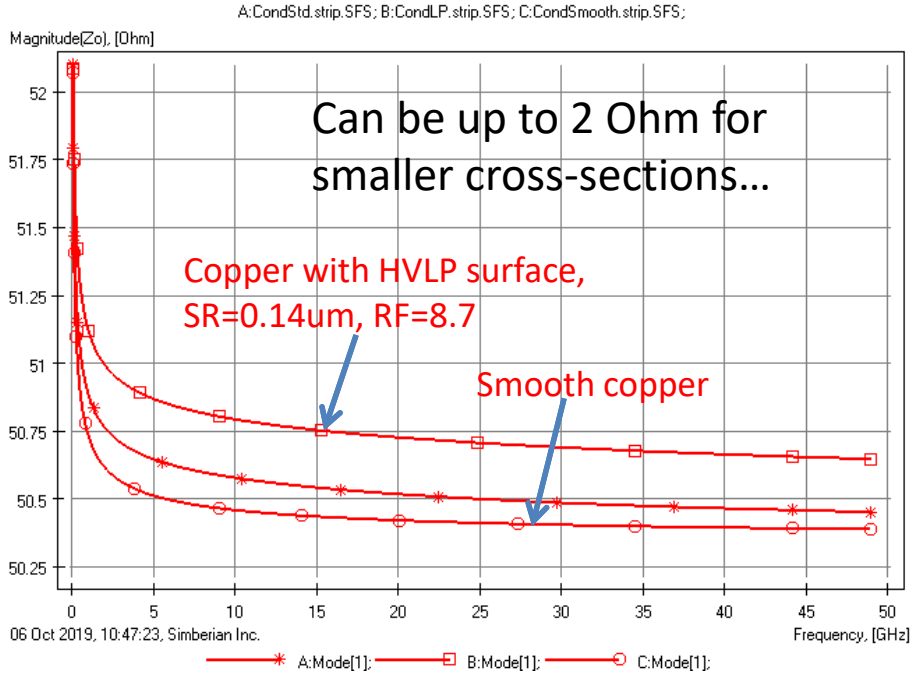
Ultra-Low loss (LT=0.001)
Meg7

Minimal possible losses on PCB are limited mostly by copper and copper roughness!

Larger smooth strips in dielectric with lower Dk and ultra-lower losses -> closer to cables;

Lossy rough conductors change delay and impedance (causality)





Copper roughness models are identified with GMS-parameters from measurements

See explanation at demo-video #2017_09: **How Interconnects Work™**: Rough conductor currents and internal inductance

Predictability of thermal losses and dispersion

- Depends on availability of frequency-continuous ultra-broadband models for dielectric and conductor roughness
- Dielectric data from laminates manufacturers can be used to construct such models with sufficient accuracy for preliminary analysis
- Dielectric models for higher data rates and for better accuracy must be identified
- Parameters for conductor roughness models are usually not available and must be identified
- Possible identification techniques with separation of dielectric and conductor loss and dispersion
  - Identification with GMS-parameters (Shlepnev, EPEPS 2015) – 2 t-line segments
  - Identification with SPP Light (Shlepnev, Choi, Cheng, Damgaci, EPEPS 2016) – 2 t-line segments
  - Gamma-T - combined identification with Gamma extraction and T-resonator (Choi, Cheng, Damgaci, Godishala, Shlepnev, DesignCon 2017)

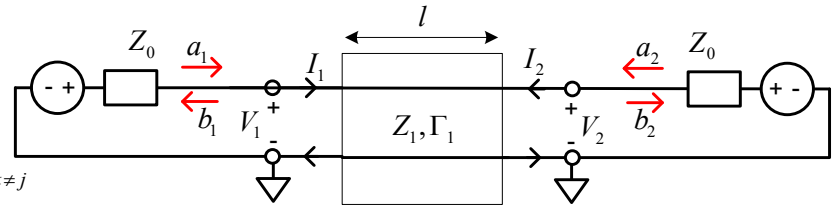
See webinars #2, #5, #6, #8 at www.simberian.com

Reflections – losses and ISI

- Reflection sources
  - Trace/transmission line and terminations impedance mismatch
  - Single discontinuities – vias, transitions, AC caps, gaps in reference plane…
  - Periodic discontinuities – cut outs, fiber-weave effect,…
- All reflections are included into transmission S-parameter (insertion loss)
- Useful as compliance metric for channel quality control
- Effective Return Loss – metric in time domain

Idealized channel S-parameters

$$S_{i,j} = \left.\frac{b_i}{a_j}\right|_{a_k=0\ k\neq j}$$



Zo – termination impedance;
Z1 complex transmission line impedance;
Gamma – complex propagation constant:

$$\Gamma_1 = \alpha + i\frac{2\pi}{\Lambda}$$

Scattering parameters:

S11 or reflection

$$S(\omega,l) = \begin{bmatrix} \left(Z_1^2 - Z_0^2\right)/D & 2\cdot Z_1\cdot Z_0\cdot csh\left(\Gamma_1\cdot l\right)/D \\ 2\cdot Z_1\cdot Z_0\cdot csh\left(\Gamma_1\cdot l\right)/D & \left(Z_1^2 - Z_0^2\right)/D \end{bmatrix} \qquad D = Z_1^2 + Z_0^2 + 2\cdot Z_1\cdot Z_0\cdot cth\left(\Gamma_1\cdot l\right)$$

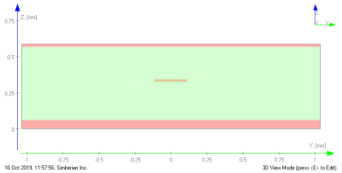
If normalization impedance is equal to the characteristic impedance of the mode, we get generalized modal S-matrix:

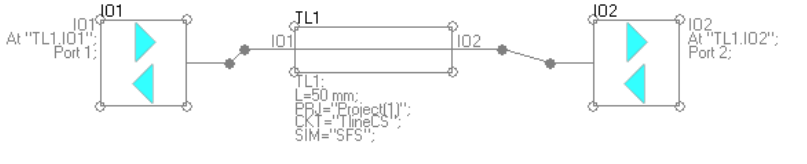
$$Z_0 = Z_1 \quad \Rightarrow \quad S(\omega,l) = \begin{bmatrix} 0 & \exp\left(-\Gamma_1\cdot l\right) \\ \exp\left(-\Gamma_1\cdot l\right) & 0 \end{bmatrix}$$

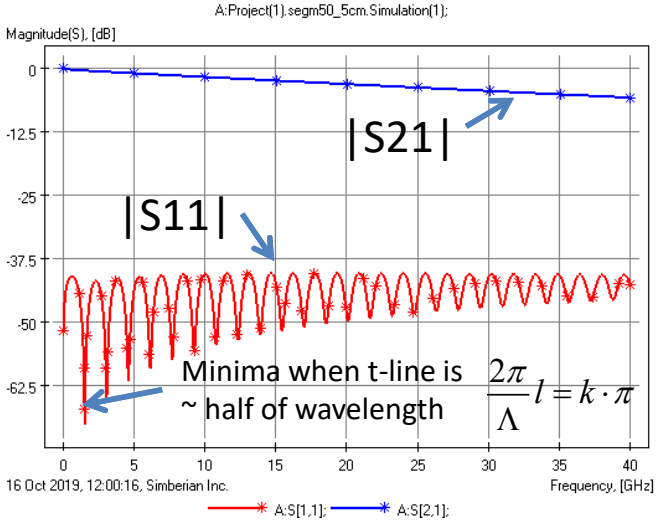
(no reflections - we can only wish that our channels are like that)

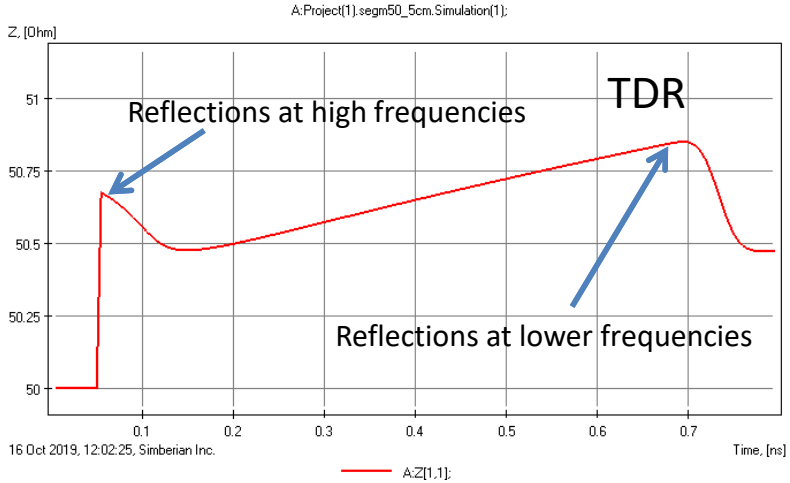
Reflections from more realistic links

5 cm about 50.5 Ohm strip line segment;
FR408 – Wideband Debye: Dk=3.8, LT=0.0117 @ 1 GHz;
Copper: RR=1.2, Causal Hammerstad Roughness Model: SR=0.4, RF=2





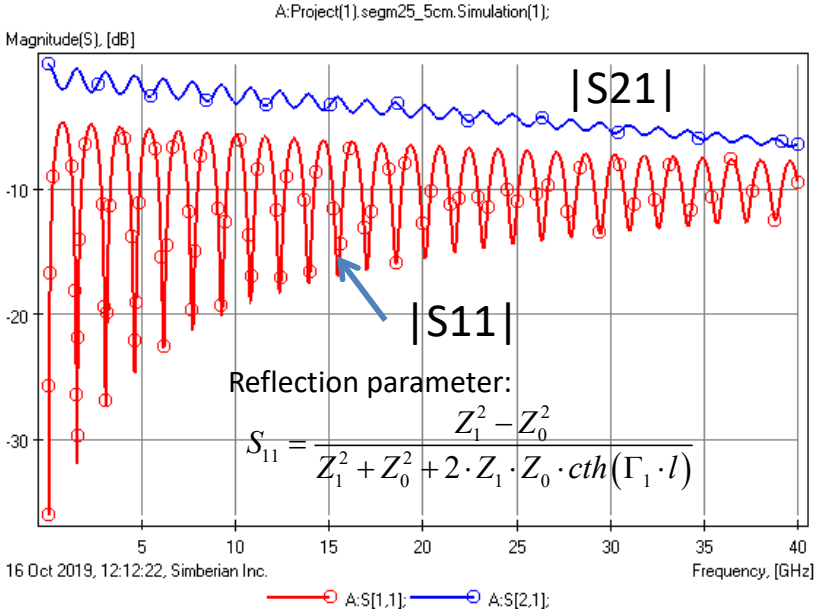




More in app note #2009_04

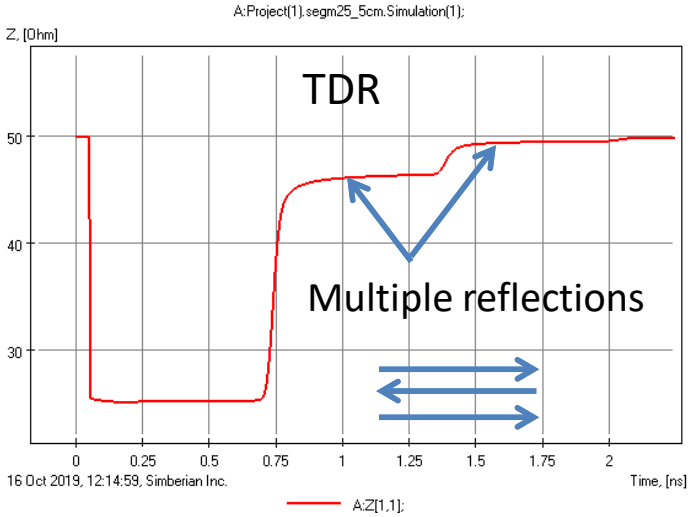
Reflections causes by impedance mismatch

5 cm about 25 Ohm strip line segment;
FR408 – Wideband Debye: Dk=3.8, LT=0.0117 @ 1 GHz;
Copper: RR=1.2, Causal Hammerstad Roughness Model: SR=0.4, RF=2



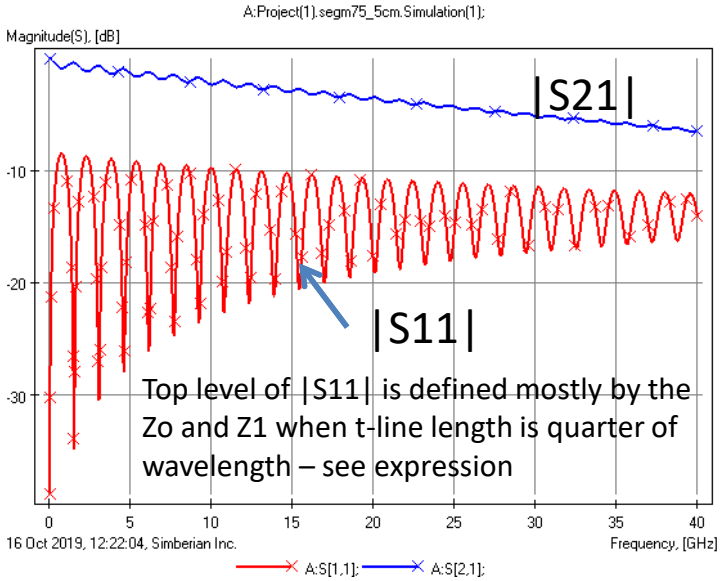
Reflection parameter:

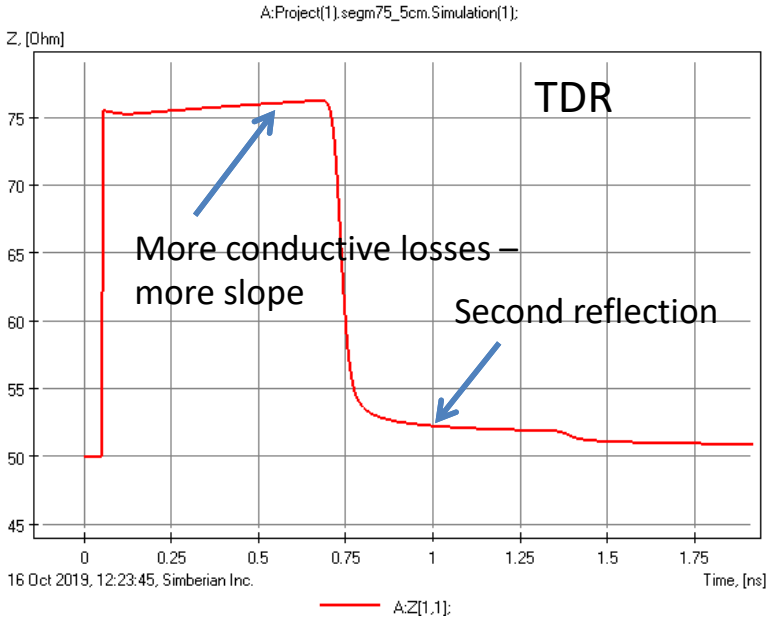
$$S_{11} = \frac{Z_1^2 - Z_0^2}{Z_1^2 + Z_0^2 + 2 \cdot Z_1 \cdot Z_0 \cdot cth(\Gamma_1 \cdot l)}$$



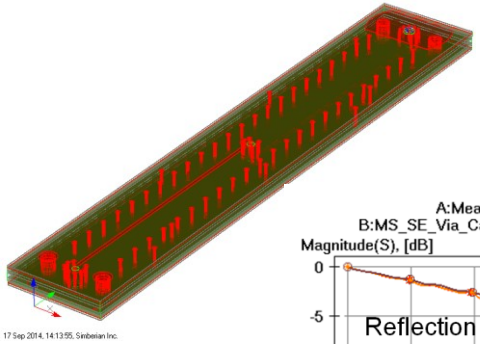
Reflections causes by impedance mismatch

5 cm about 75 Ohm strip line segment;
FR408 – Wideband Debye: Dk=3.8, LT=0.0117 @ 1 GHz;
Copper: RR=1.2, Causal Hammerstad Roughness Model: SR=0.4, RF=2

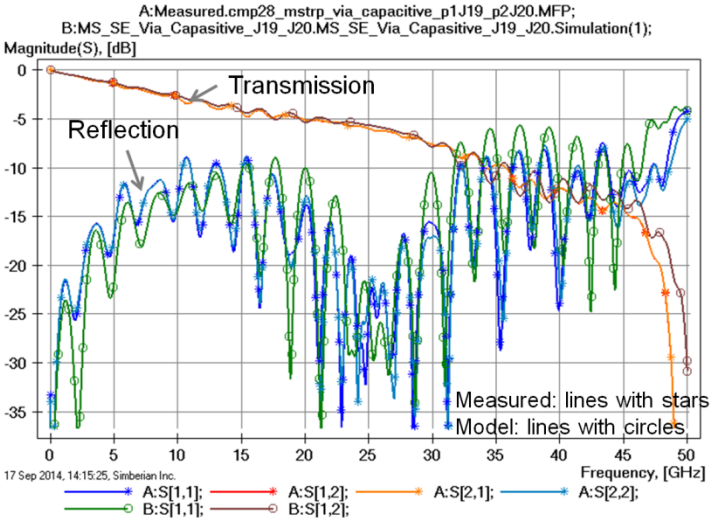


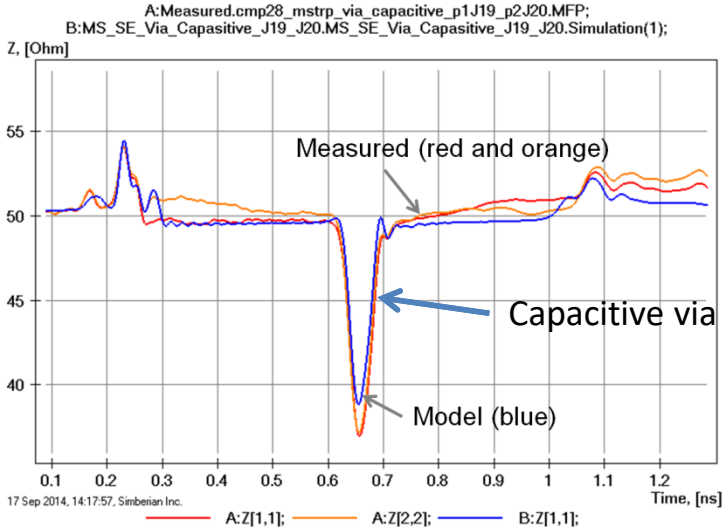


Major discontinuities - VIAS



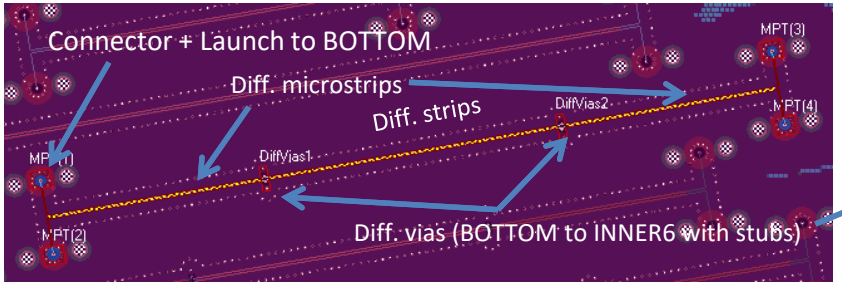
Capacitive PCB SE via example from CMP-28 channel modeling platform from Wild River Technology – complete kit is available on request



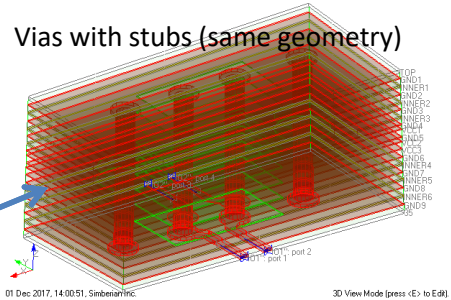


Vias must be optimized!!!

EvR1-C1: Diff. link with 2 vias with stubs from BOTTOM to INNTER6



Vias with stubs (same geometry)

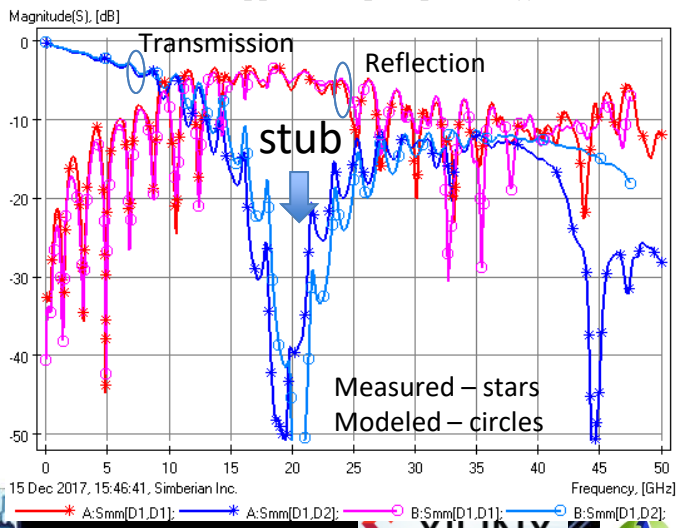


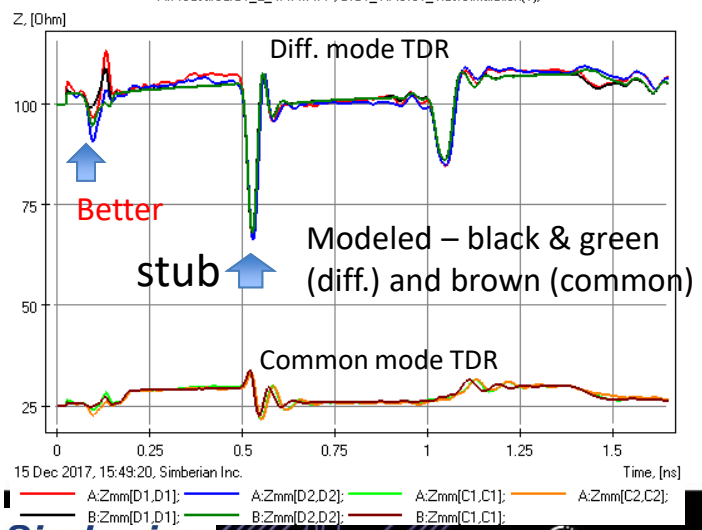
De-compositional EM analysis
Shape and size of all traces and backdrilling position are adjusted…

Vias simulated with "thick" metal option

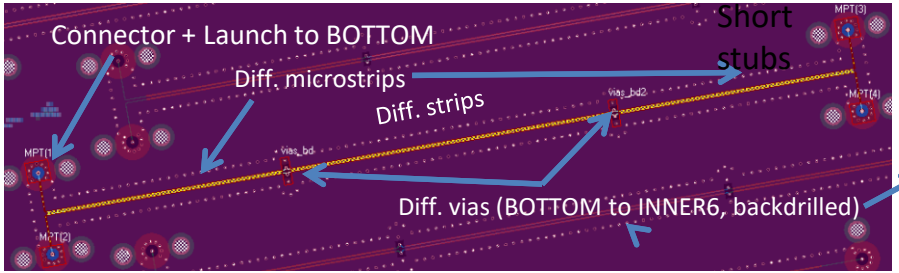
Mixed-mode S-parameters & TDR

Analysis to measurement correlation example from EvR-1 project – see more at app notes #2018_01, 2018_07 and webinar #8 at www.simberian.com

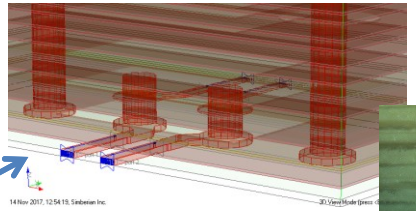




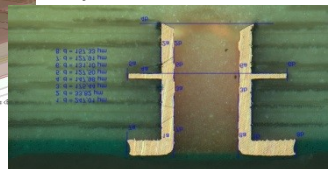
EvR1-C2: Diff. link with 2 optimized vias from BOTTOM to INNTER6



Backdrilled vias model



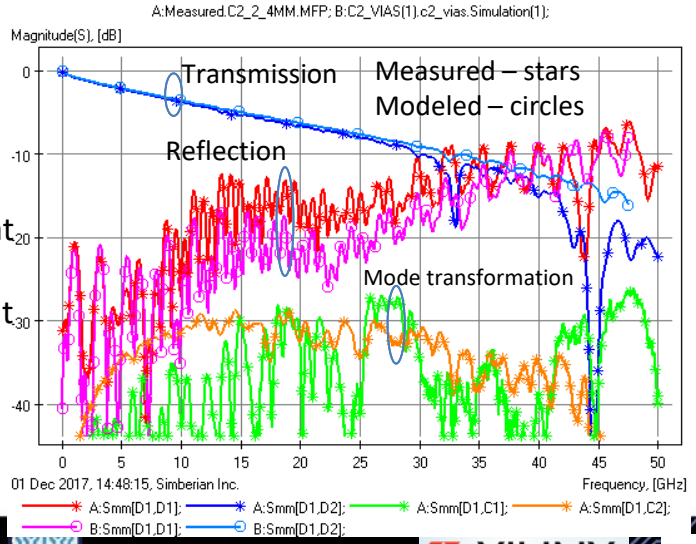
De-compositional EM analysis
Shape and size of all traces and backdrilling position are adjusted…

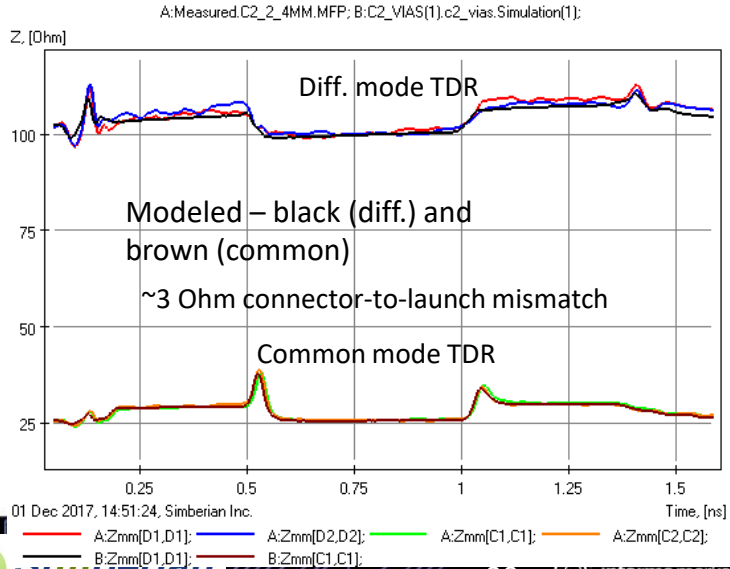


Mixed-mode S-parameters

Analysis to measurement correlation example from EvR-1 project – see more at app notes #2018_01, 2018_07 and webinar #8 at www.simberian.com

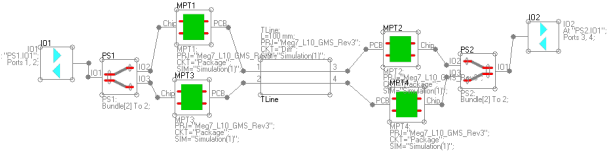
Acceptable correspondence up to 30 GHz

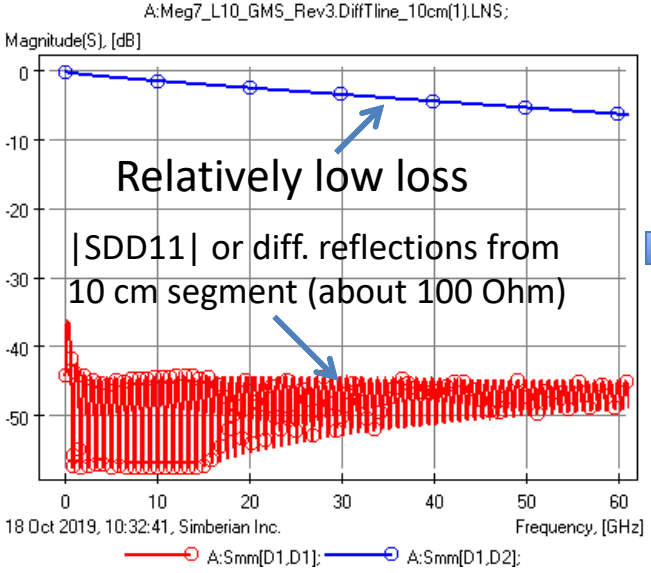




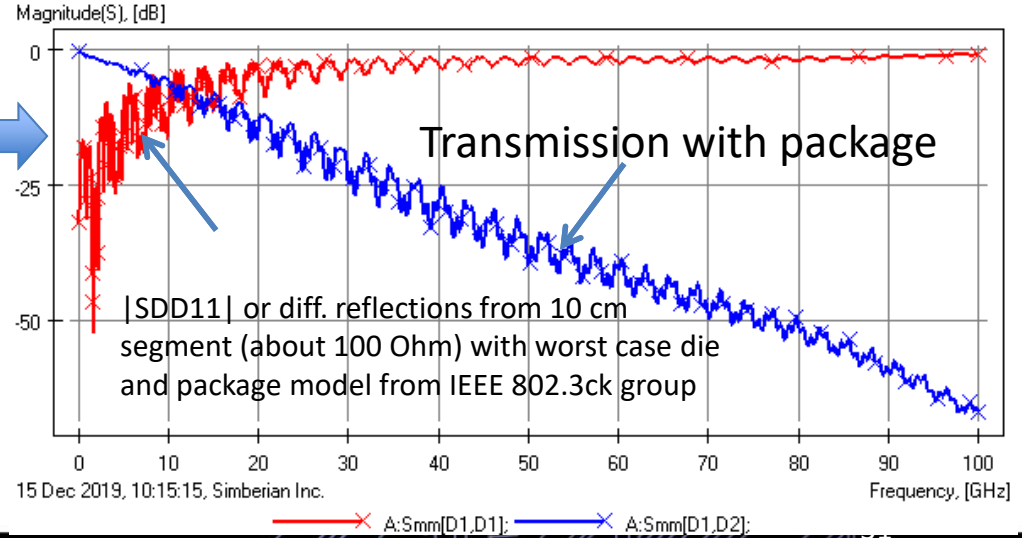
Reflections from discontinuities – With Die & PKG model from IEEE 802.3ck

Meg7 – Wideband Debye: Dk=3.17, LT=0.0011 @ 1 GHz
Copper: RR=1.4, Roughness – Huray- Bracken Model:
SR=0.14 um, RF=8.7

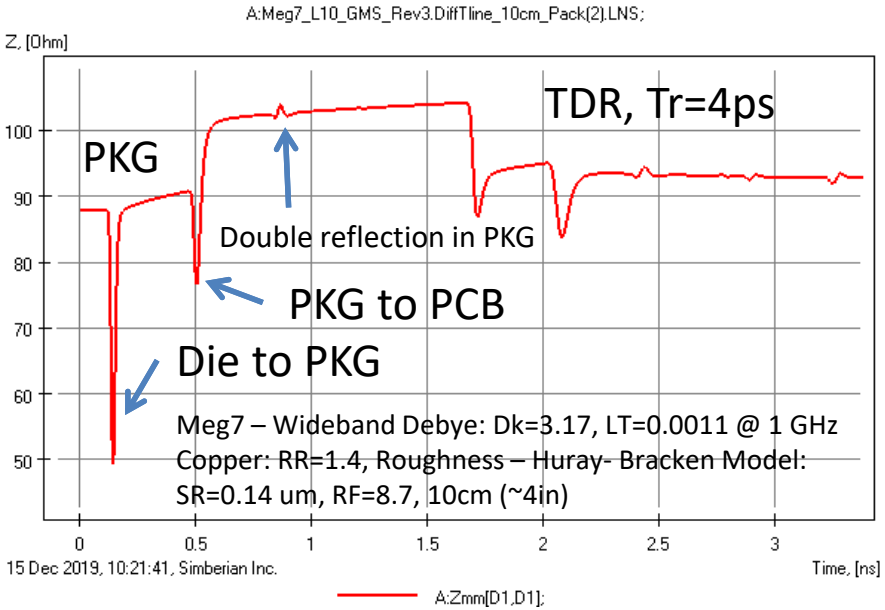


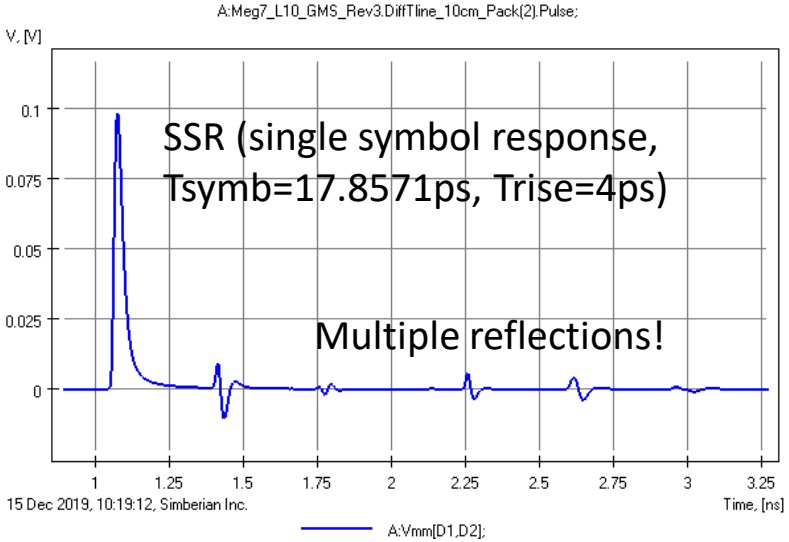


Cd=120fF, Ls=120 pH Cb=30fF, Cp=90fF, Lp=30mm



Reflections from discontinuities – With die & PKG model from IEEE 802.3ck

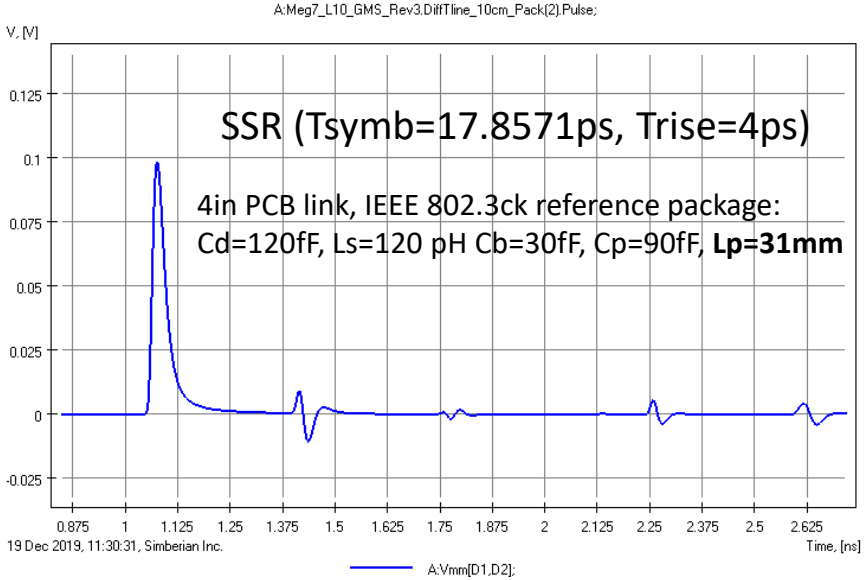




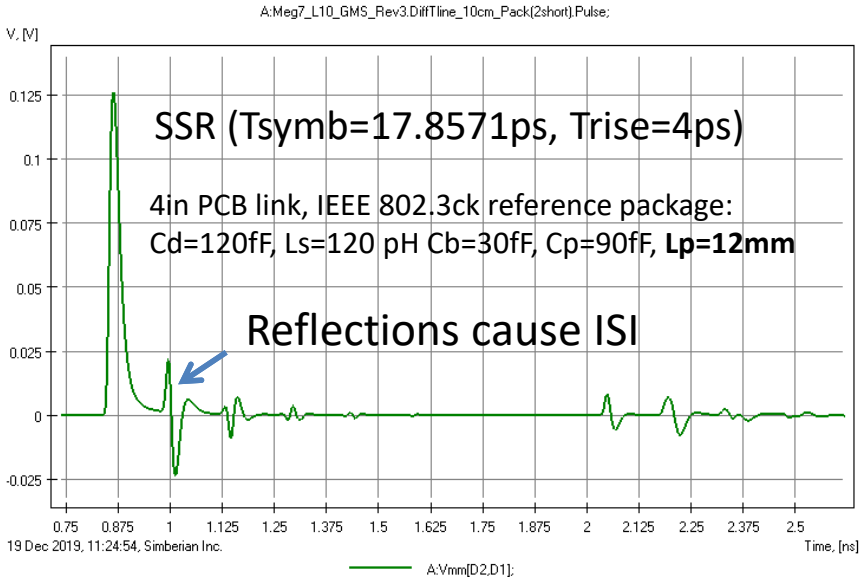
Worst case reference package model from IEEE 802.3ck group for COM metric computation: Cd=120fF, Ls=120 pH Cb=30fF, Cp=90fF, Lp=30mm

Shorter package -> more distortions

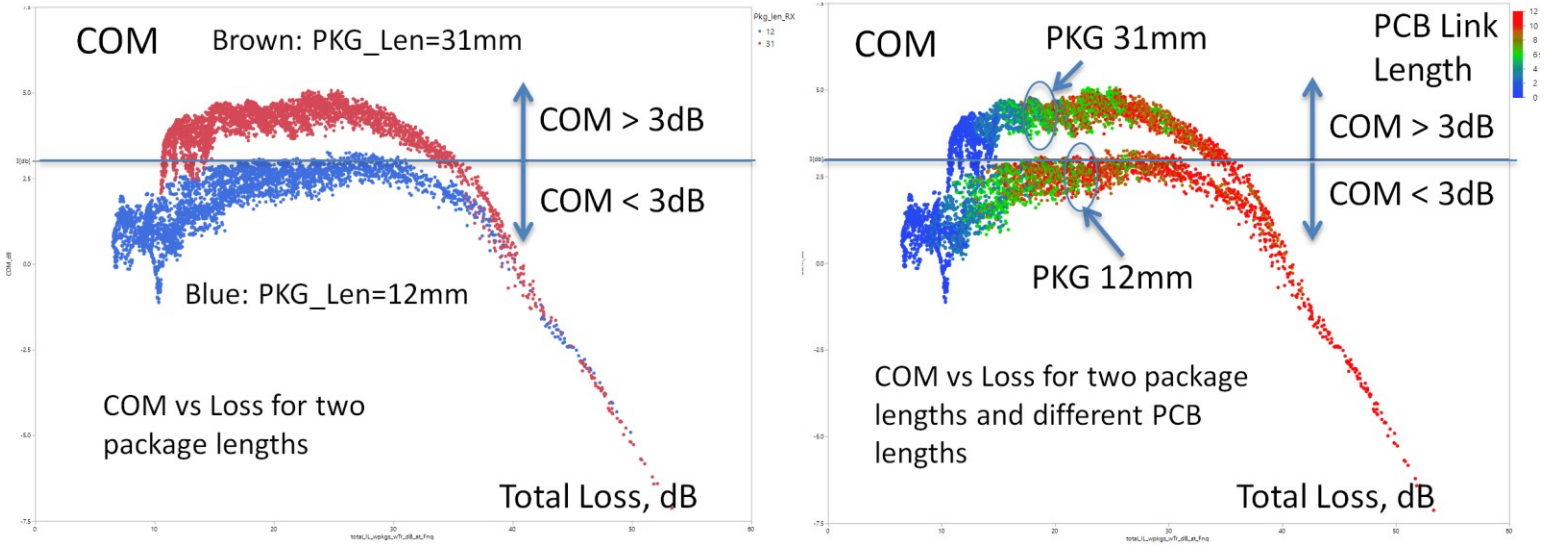
Longer package (30mm)



Shorter package (5mm)



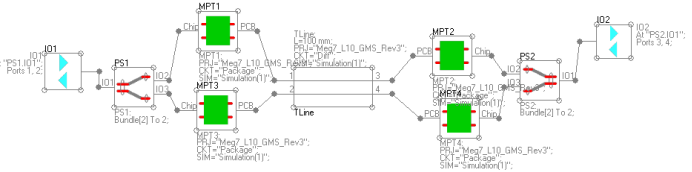
Package discontinuity importance



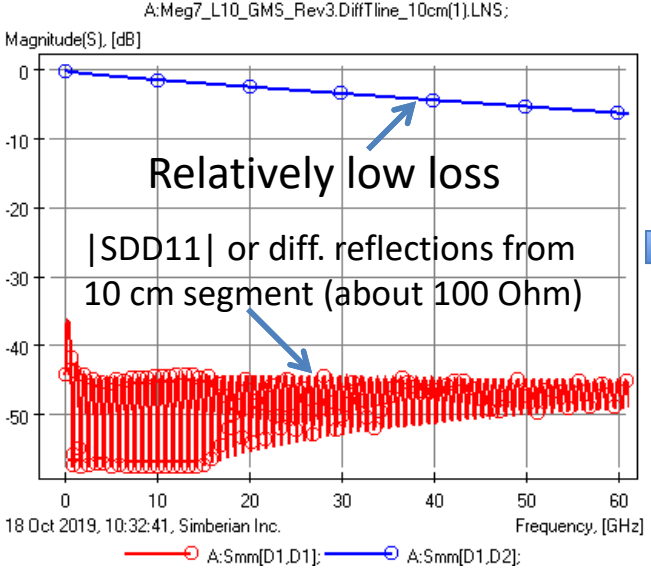
More at A. Manukovsky, Y. Shlepnev, Z. Khasidashvili, E. Zalianski, *Machine Learning Applications for COM Based Simulation of 112Gb Systems*, DesignCon2020, Wednesday, January 29, 12:00pm - 12:45pm, Ballroom F.

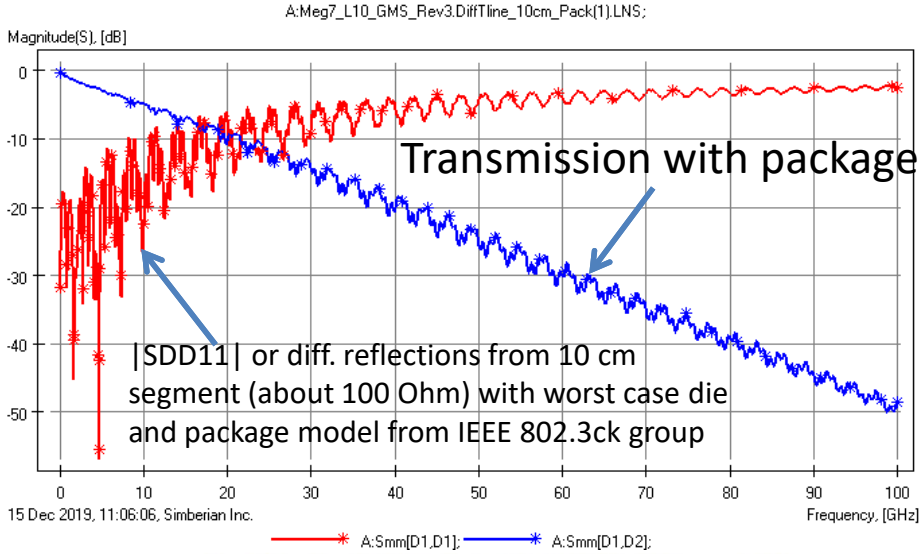
Reflections from discontinuities: Half of worst case IEEE 802.3ck

Meg7 – Wideband Debye: Dk=3.17, LT=0.0011 @ 1 GHz
Copper: RR=1.4, Roughness – Huray- Bracken Model:
SR=0.14 um, RF=8.7



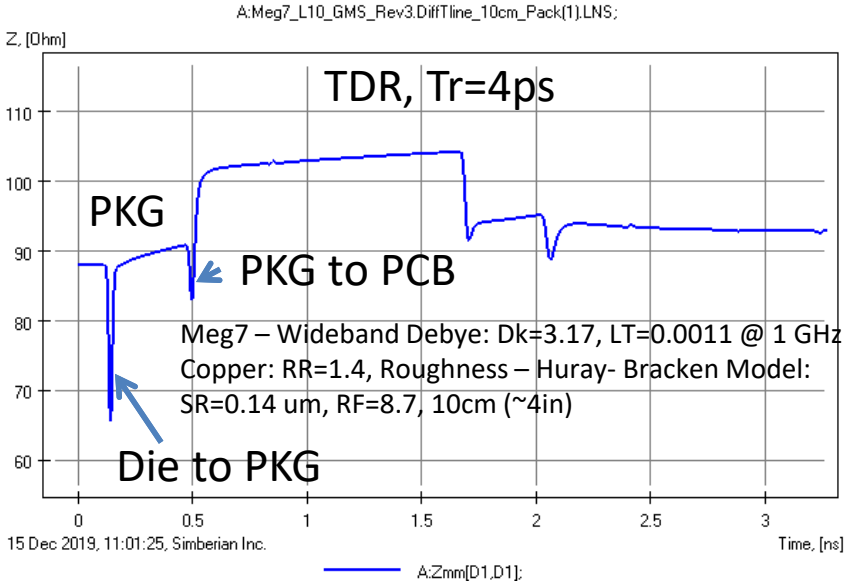
Cd=60fF, Ls=120 pH, Cb=15fF, Cp=45fF, Lp=30mm

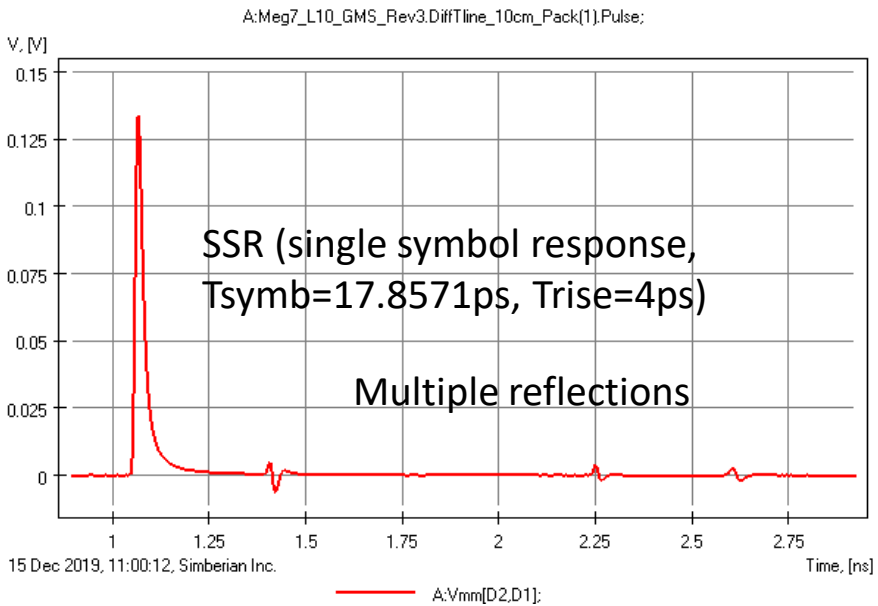




Reflections from discontinuities

It looks bad even with the half of worst case – package is a weak link

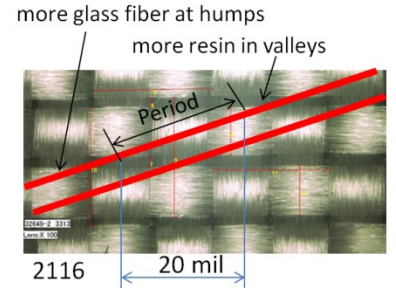


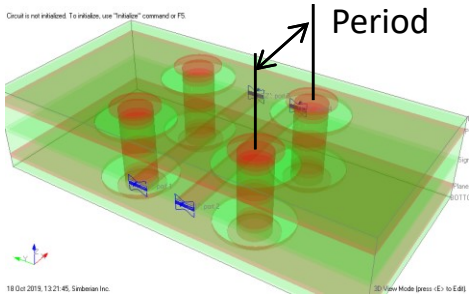


Half of worst case reference package model from IEEE 802.3ck group for COM metric computation: Cd=60fF, Ls=120 pH Cb=15fF, Cp=45fF, Lp=30mm

Reflections from periodic discontinuities

- Fiber-Weave Effect – periodic discontinuities in dielectric
- Periodic cut-outs in ground planes - traces in BGA breakout
- Via fences too close to traces
- Periodic discontinuities can be used to equalize even and odd mode velocities in tabbed microstrips and flex interconnects





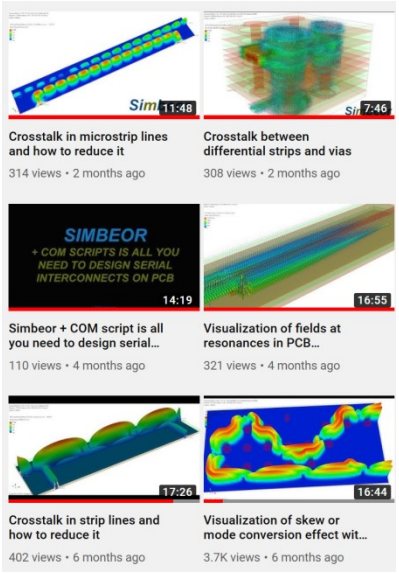
Resonance at Wavelength = 2*Period

See demo-video #2019_06: **How Interconnects Work™**: Visualization of fields at resonances in PCB interconnects

More on discontinuities and periodic structures

- #2017_07: **How Interconnects Work™**: Microstrip crossing slot in the reference plane - long slots and close solid plane cases
- #2017_06: **How Interconnects Work™**: Microstrip crossing slot in the reference plane
- #2017_05: **How Interconnects Work™**: Microstrip over circular cut-outs in reference plane (with analysis to measurement validation)
- #2017_03: **How Interconnects Work™**: Differential microstrip over meshed reference plane in flex interconnects
- #2017_02: **How Interconnects Work™**: Microstrip over meshed reference plane in flex interconnects

See it on YouTube Simbeor channel….



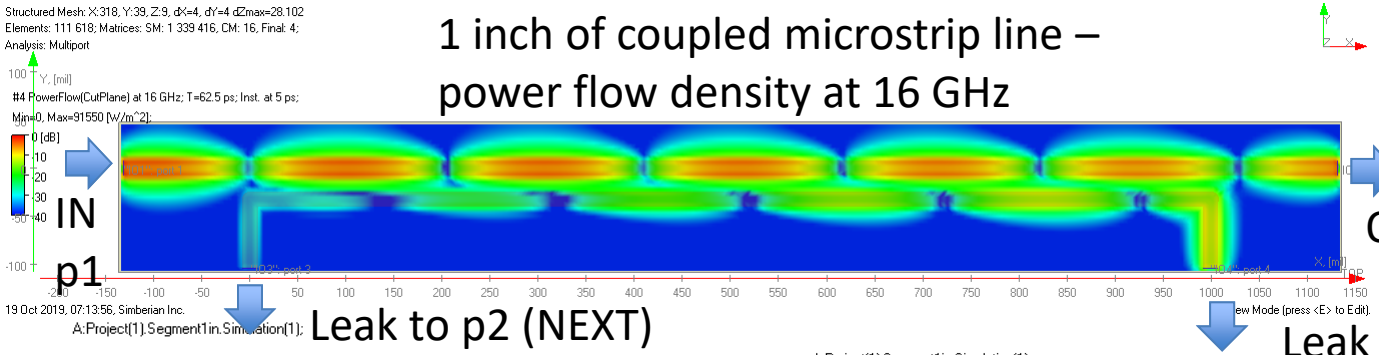
Couplings: Leaks and Interference

- Crosstalk – leaks and interference in traces
- Via localization breakout – leaks and interference and through parallel planes and between vias
- Couplings through slots and cutouts in reference planes
- Modal transformations in diff. pairs (aka skew) – bends, asymmetry in routing, FWE
- Multipath propagation, radiation, EMI, EMC,…

Leaks and multipath propagation are all included in transmission S-parameter (S21 or SDD21, insertion loss)

Couplings and interference from aggressors are always additional parameters (NEXT, FEXT, common to differential,…)

Crosstalk - Leaks



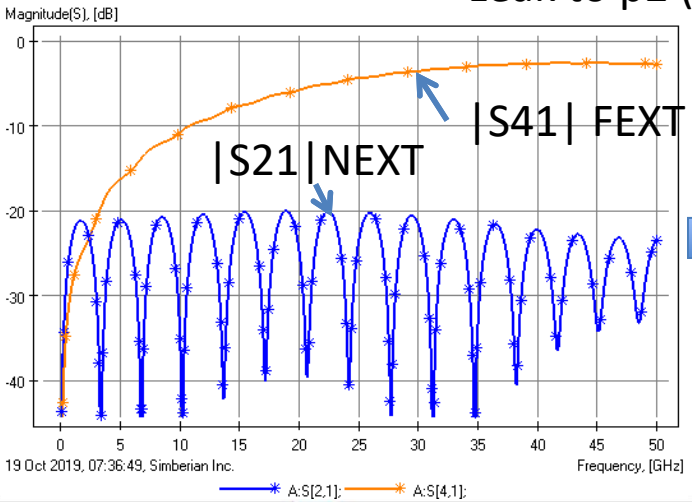
1 inch of coupled microstrip line – power flow density at 16 GHz

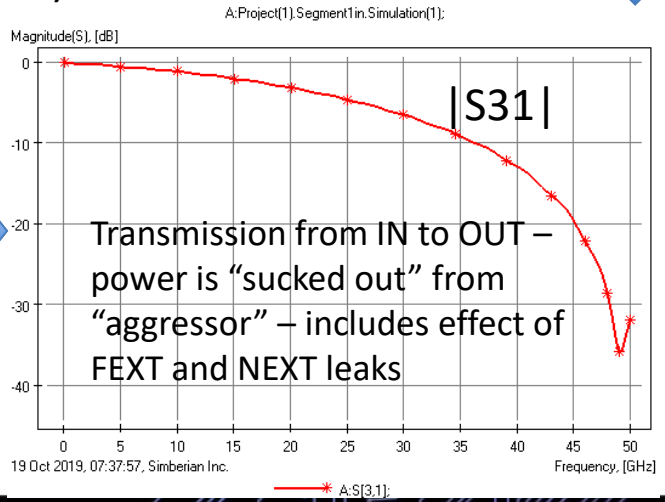
IN p1

OUT p3

Leak to p2 (NEXT)

Leak to p4 (FEXT)

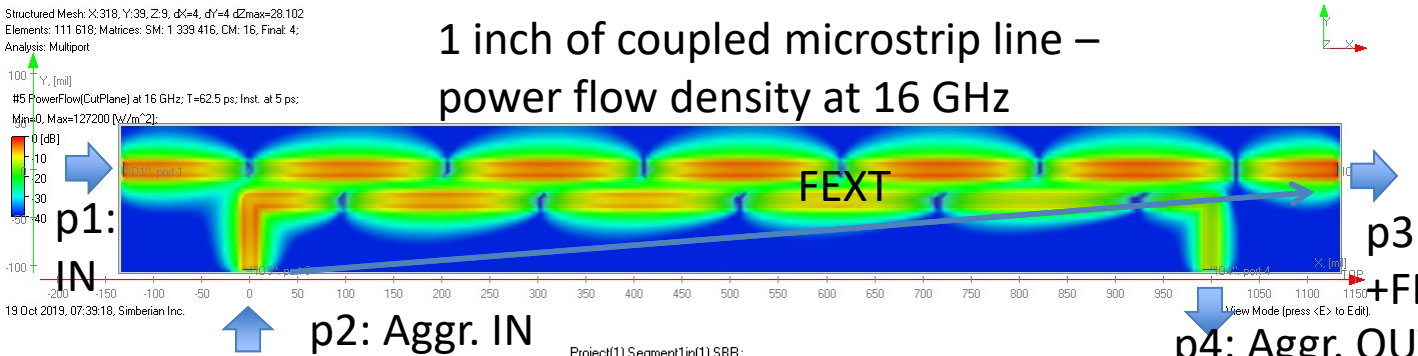


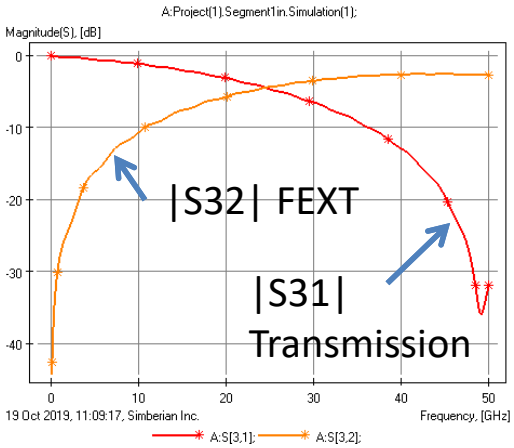


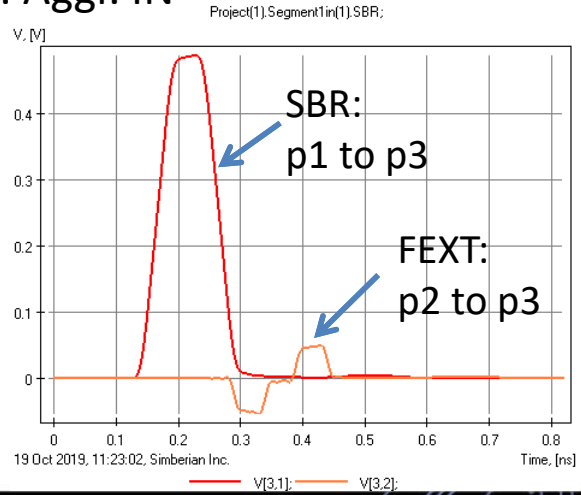
Behavior can be explained by superposition of odd and even modes in coupled segment

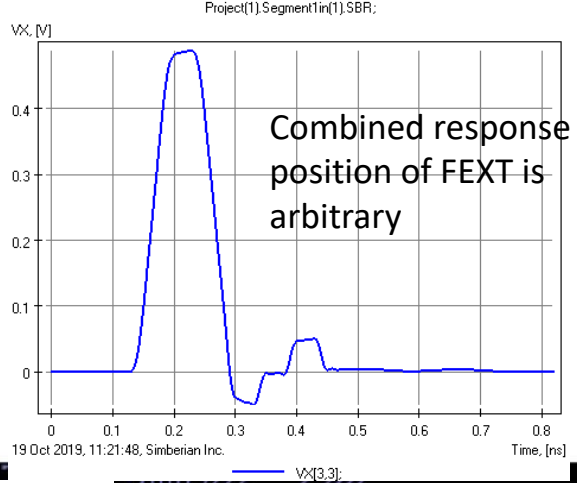
Crosstalk - Interference

1 inch of coupled microstrip line – power flow density at 16 GHz



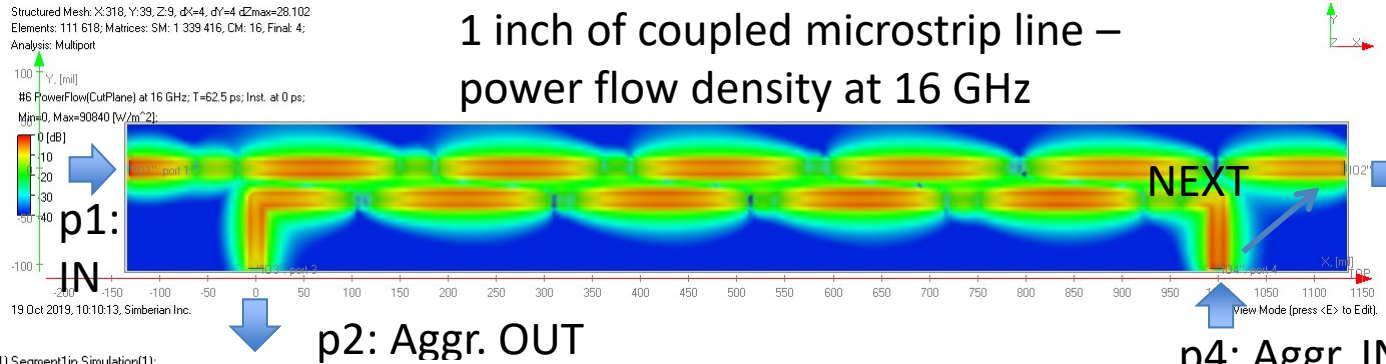


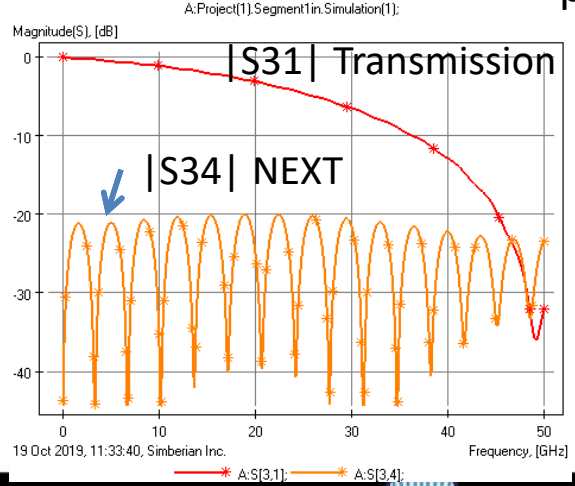


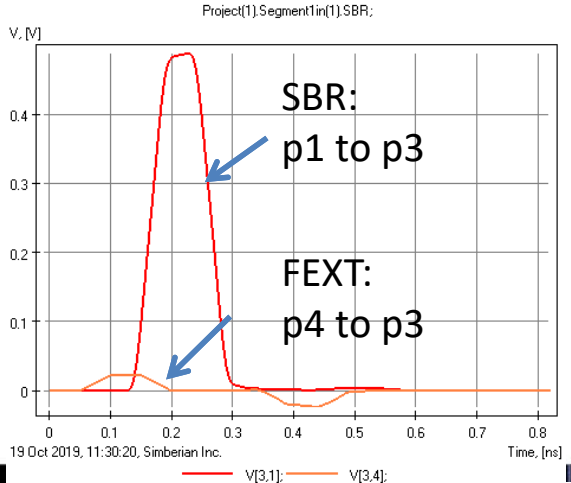


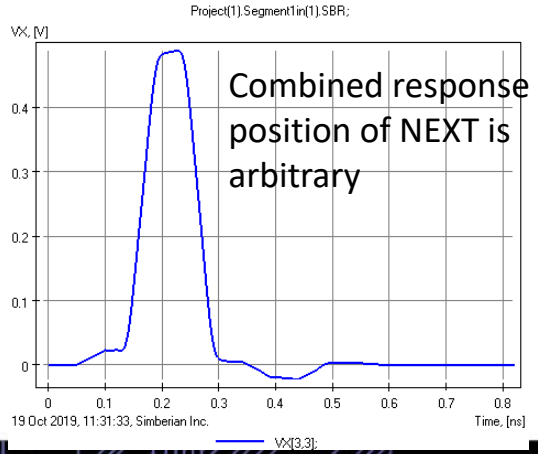
Crosstalk - Interference

1 inch of coupled microstrip line – power flow density at 16 GHz



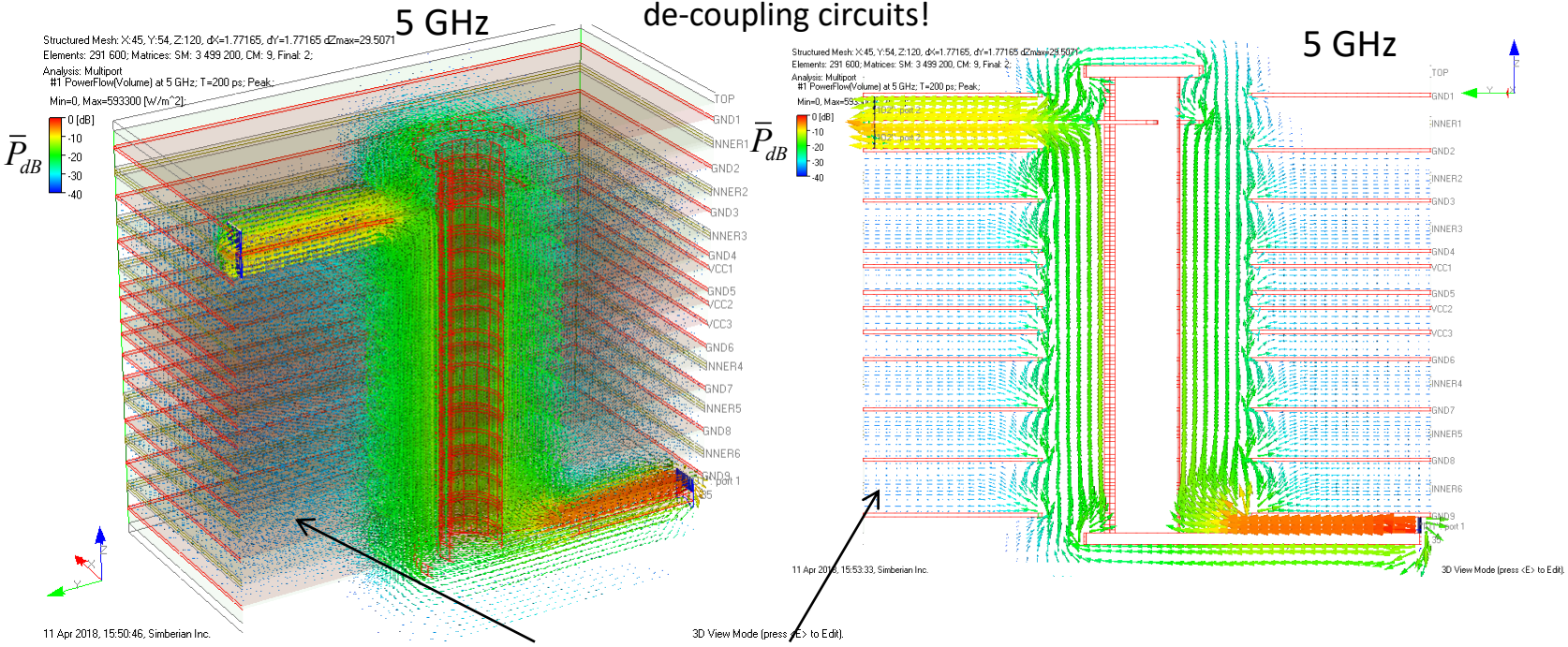






Power leaks from single via (no stitching)

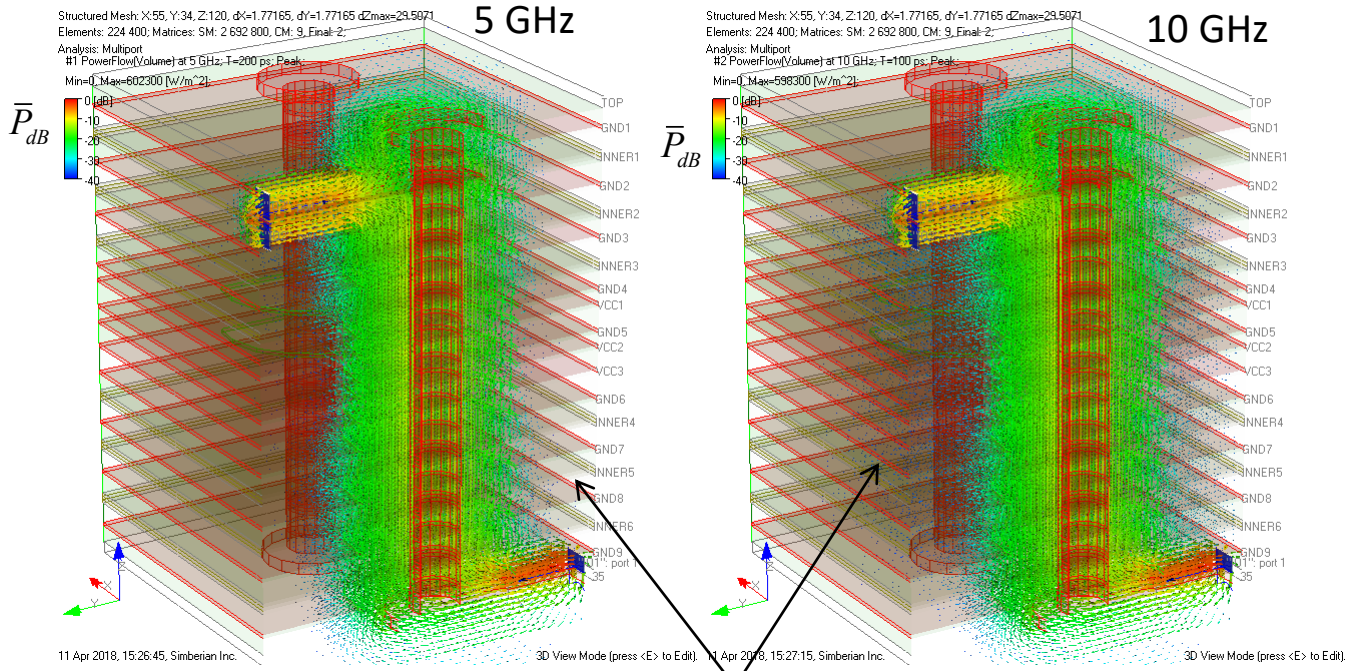
Behavior of such via will depend on the board geometry and de-coupling circuits!



Power leaks into inter-plane areas

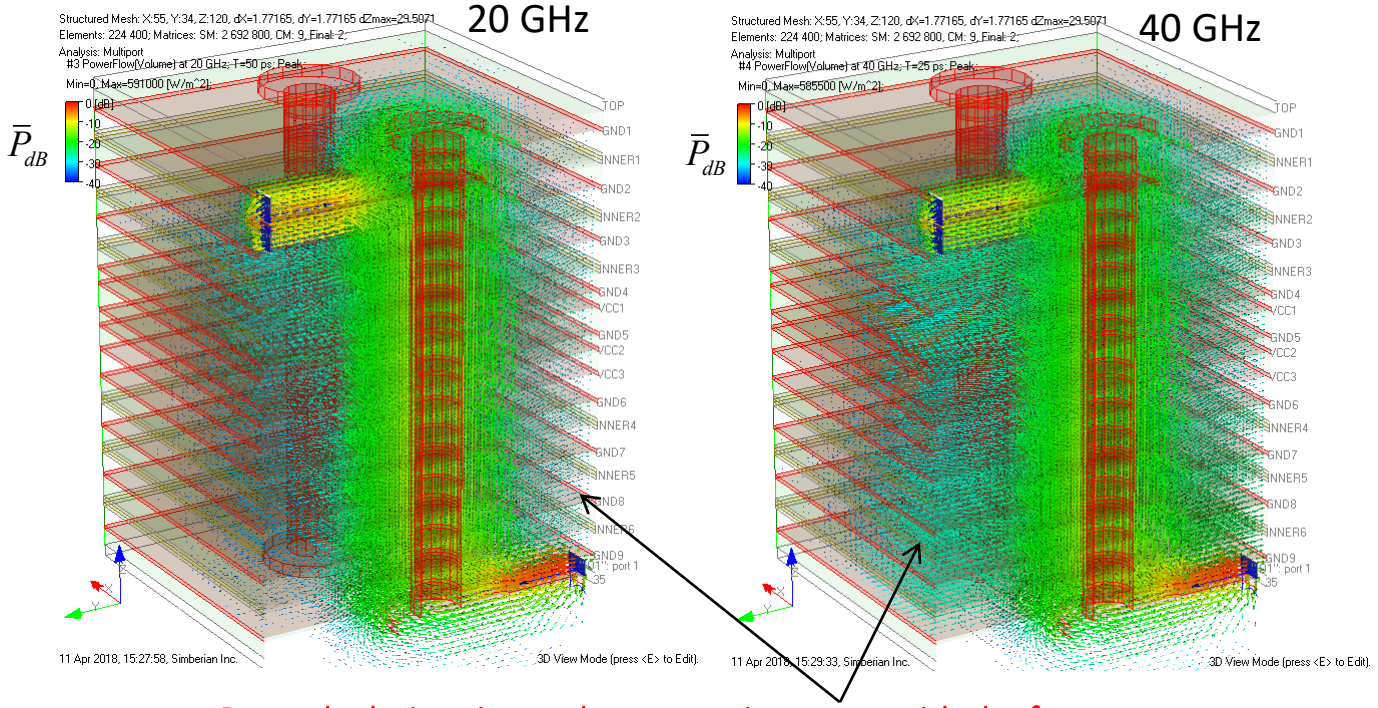
Demo-video #2019_08: **How Interconnects Work™**: Signal leakage from single-ended PCB vias - visualize and fix it!

Power flow through via with 2 stitching vias – conditionally localized structure



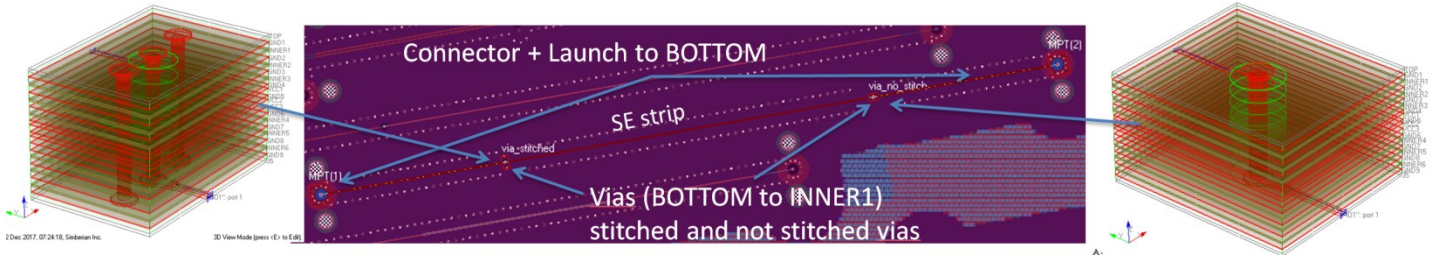
Small power leaks into inter-plane areas at lower frequencies

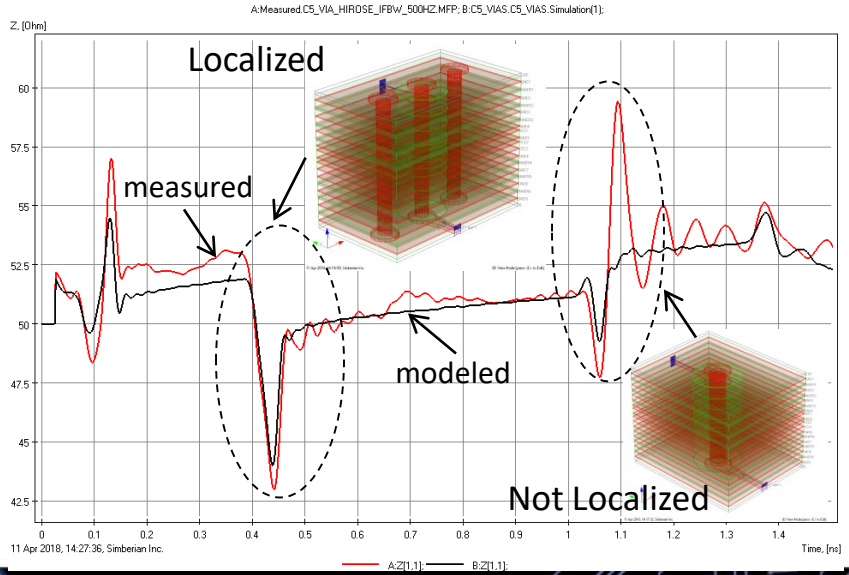
Power flow through via with 2 stitching vias – breakout of localization



Power leaks into inter-plane areas increases with the frequency

Via predictability from EvR-1 board





Via with just 2 stitching vias at 30 mil distance is localized only up to 10-15 GHz

Behavior of the single via is unpredictable!

From M. Marin, Y. Shlepnev, 40 GHz PCB Interconnect Validation: Expectation vs. Reality, DesignCon2018, January 31, 2018, Santa Clara, CA.

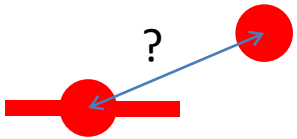
PREDICTABILITY OF COUPLINGS –
design only with localized predictable structures!

Not localized == not predictable!

Stripline

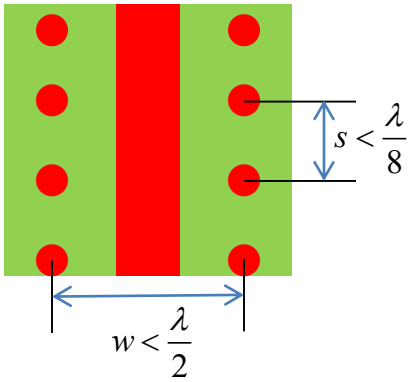
Microstrip

Via + stitching via(s) somewhere

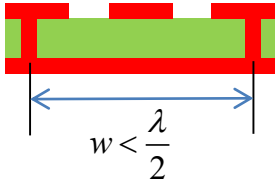


Predictable, conditionally localized, single-mode!

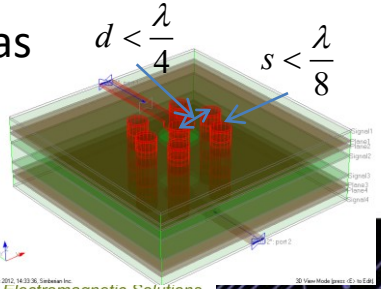
"Fenced" Stripline



CBCPW



Localized Vias

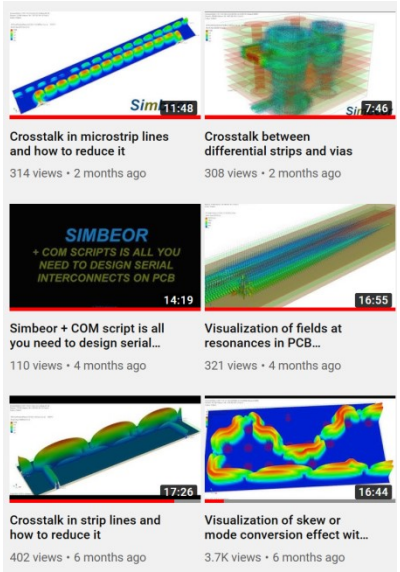


If not possible - use of bandgap structures for localization

More on coupling…

- #2019_11: **How Interconnects Work™**: Crosstalk in microstrip lines and how to reduce it (use of tabbed lines)
- #2019_10: **How Interconnects Work™**: Where crosstalk may come from - case of coupling between differential striplines and vias
- #2019_09: **How Interconnects Work™**: Where crosstalk may come from - case of stripline coupling through antipads in BGA breakout areas
- #2019_05: **How Interconnects Work™**: Crosstalk in adjacent striplines and how to reduce it - visualization with power flow density
- #2019_03: **How Interconnects Work™**: Crosstalk in striplines and how to reduce it - visualization of coupling with power flow density, electric and magnetic fields and current density
- #2019_02: **How Interconnects Work™**: Visualization of mode conversion or skew in differential traces with power flow density
- #2017_08: **How Interconnects Work™**: Crosstalk in microstrip traces crossing split planes
- #2016_13: **How Interconnects Work™**: Crosstalk power flow in differential vias
- #2016_12: **How Interconnects Work™**: Crosstalk power flow in single-ended vias
- #2016_11: **How Interconnects Work™**: Crosstalk power flow in microstrip lines

See it on YouTube Simbeor channel….



Analysis of PCB/Packaging Interconnects

Equations and solutions

Accuracy

Predictability

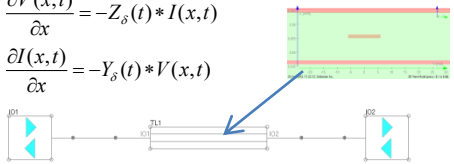
Analysis of Interconnects: Problem dimension and formulation

1D models or transmission line models – Telegrapher's equations

Modal or per unit length parameters for the Telegrapher's equations (Z, Y) are computed with static or quasi-static field solver (2D problems for Laplace's equations) or an electromagnetic fields solver (3D problems for Maxwell's equations)

Lines with coupling, multimodal waveguides, periodic structures can be accurately modeled

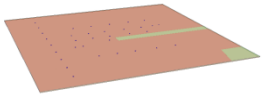
$$\frac{\partial V(x,t)}{\partial x} = -Z_\delta(t) * I(x,t)$$
$$\frac{\partial I(x,t)}{\partial x} = -Y_\delta(t) * V(x,t)$$



2D models or transmission plane models - 2D Telegrapher's equations (Maxwell's equations for 2D TE problems)

Component to model power delivery processes in parallel plane PDNs

See more at Y. Shlepnev, ACES 2006, EPEPS 2012



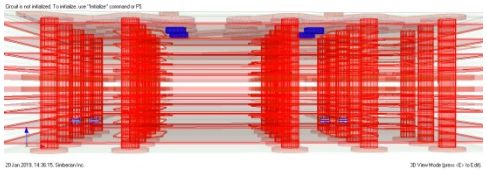
$$\frac{\partial J_{sx}(t)}{\partial x} + \frac{\partial J_{sy}(t)}{\partial y} = -Y_{\square}(t) * V(t) + J_z(t)$$
$$\frac{\partial V(t)}{\partial x} = -Z_{\square}(t) * J_{sx}(t)$$
$$\frac{\partial V(t)}{\partial y} = -Z_{\square}(t) * J_{sy}(t)$$

3D models or 3D full-wave models - everything described and solved with Maxwell's equations without any simplifications for 3D geometries or field components

Analysis of discontinuities such as via-holes, connectors or any type of transitions between uniform traces

Analysis of SI, PI or SI+PI with 3D models is possible with some tools, but may be not practical due to enormous complexity and accuracy issues

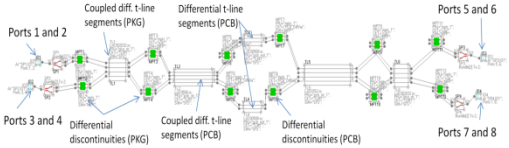
$$\nabla \times \vec{H}(\vec{r},t) = y_\delta(\vec{r},t) * E(\vec{r},t) + J$$



Analysis of Interconnects: Hybrid models

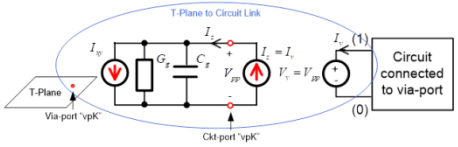
1D+3D: Hybrid de-compositional analysis with transmission line models for traces (1D) and 3D models for discontinuities or transitions

The best technique for the serial interconnects under the localization condition (Y. Shlepnev, EMC 2013)
This approach usually works for PCB and packaging problems with relatively long traces, but may fail if trace segments are too short - complete 3D analysis is required in this case



1D+2D: Hybrid analysis with transmission line models (1D) and the transmission plane models (2D) coupled at the via-holes (more at Y. Shlepnev, ACES 2006)

Such models are usually used to simulate SI + PI - even the whole board simulation is possible in many tools based on this technique, popular for solving un-localized problems
Though, the accuracy is severely limited due to via-hole models simplifications

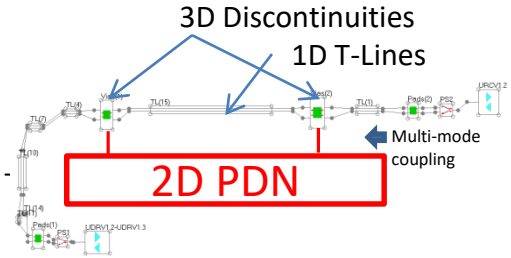


1D+2D+3D: Hybrid analysis with transmission line models (1D), transmission plane models (2D) with the coupling between two modeled simulated with 3D analysis

Advantage - fast algorithms of 1D+2D and accuracy of 3D at the discontinuities

Needed only in case if there is substantial coupling between 3D (via for instance) and 2D (PDN) models - **case of non-localized vias**, when energy from SI go to PI and the other way around

If you forced to use this approach, the alternative is to fix design – enforce the localization and simplify the problem back to 1D+3D

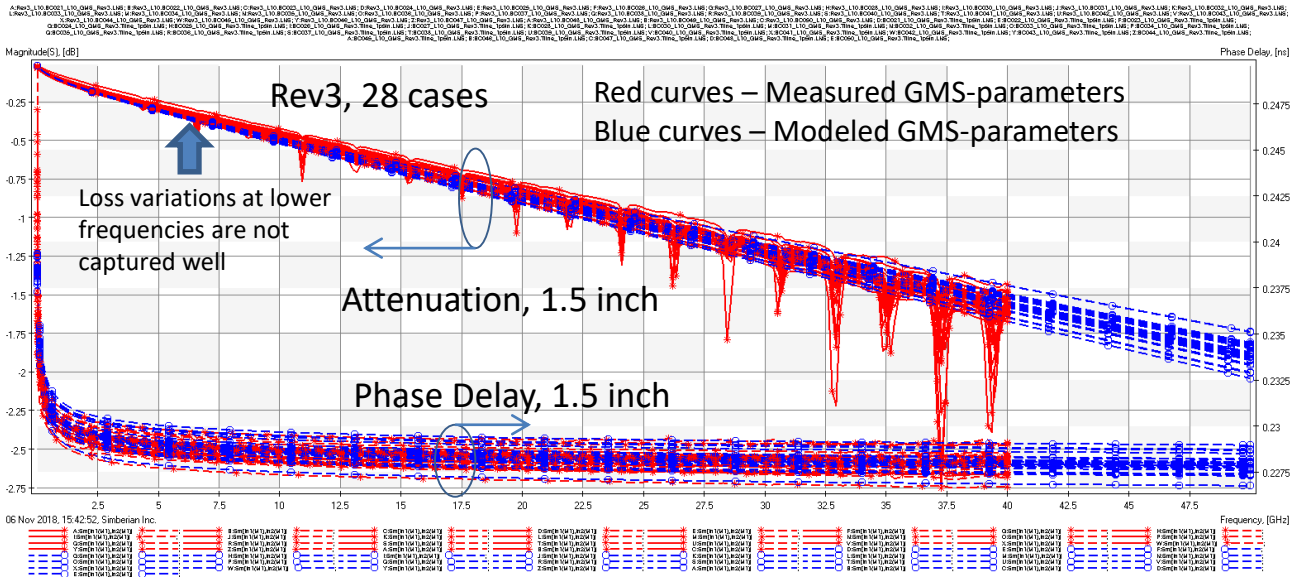


Accuracy of 1D+3D de-compositional analysis

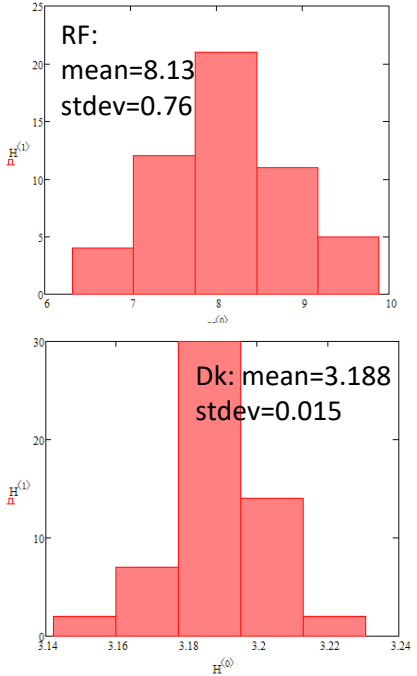
- Accuracy depends on proper **localization of every single element in the link**
  - Easy for 6 Gbps and very difficult on PCB for bandwidth of 112 Gbps signal
- **Broadband dielectric and conductor roughness models** are identified (with GMS-parameters or SPP Light)
  - Very important for PCB – models must be statistical for 56-112 Gbps (see more A. Manukovsky, Y. Shlepnev, DesignCon 2019, EPEPS 2019), about time to start doing it for packages
- **Manufactured geometry adjustments** are identified
  - May be less important for packages, very important for PCB – models must be statistical for 56-112 Gbps
- **Electromagnetic solvers are formally validated with measurements** using systematic approach ("sink or swim" for instance)
  - This is not just getting the analysis matching the measurements by any means – see more at M. Marin, Y. Shlepnev, DesignCon 2018, EMC 2018, Webinar #8
  - There are no data on solvers that are formally validated for 112 Gbps signal bandwidth (so far variations in geometry and materials technically prohibit this)
- Other considerations: Ports consistency and de-embedding, boundary conditions,…

Limitations on predictability of PCB interconnects

LT=0.001 @ 1 GHz, RR=1.5, SR=0.15 um, Dk, and RF are adjusted



Models extracted with Simbeor SDK



#2019_01: A. Manukovsky, Y. Shlepnev, Effect of PCB Fabrication Variations on Interconnect Loss, Delay, Impedance & Identified Material Models for 56-Gbps Interconnect Designs, DesignCon 2019
#2019_04: A. Manukovsky, Y. Shlepnev, Measurement-assisted extraction of PCB interconnect model parameters with fabrication variations, EPEPS 2019

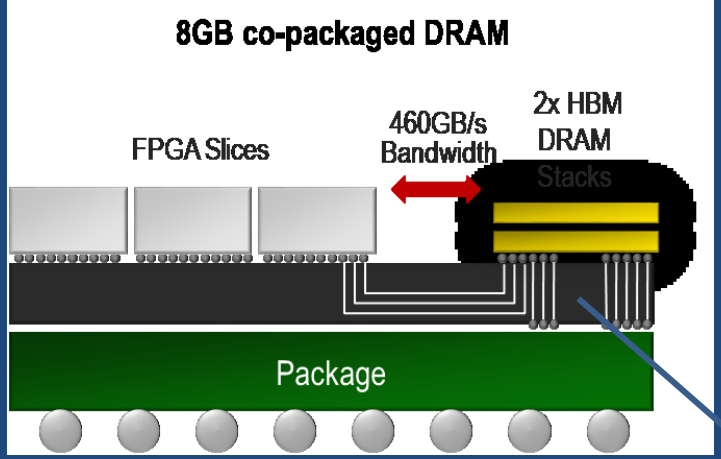
causes 1 Ohm variation in Zo

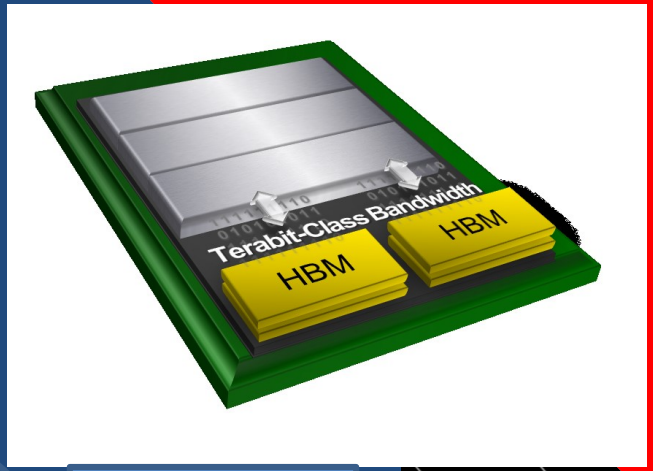
Design insights from signal integrity practitioner – examples of interconnect design

Vadim Heyfitch, Xilinx

Analysis of interconnects

- HBM2 on Organic Interposer as an Example of Chiplets' Interface
- 112G PAM4 Single-Ended Channel in 7-2-7 Package Substrate:
  Via Design & Channel Analysis
- Validation of Characteristic Impedance on Package Substrate with Micro-probing and Measurements
- GL102 Material Property Identification with a Test Vehicle
- Crosstalk in BGA Breakout on PCB:
  When is necessary to back drill?
  How much does it help?
- Guard Rail between Differential Pairs:
  Does it help? How much space does it save?
- RCM use for Multi-scale time-domain PDN simulation





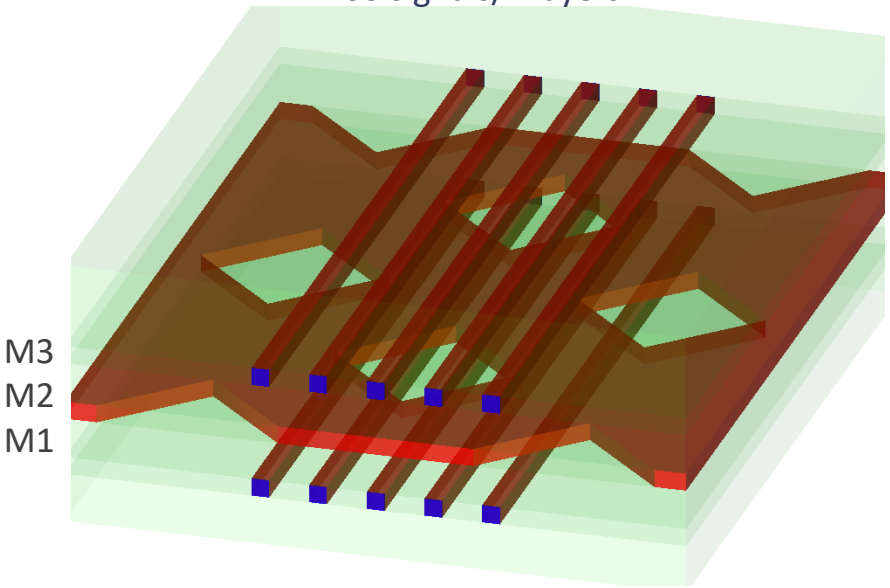
Does not have to be Silicon…

HBM2 on Organic Interposer as an Example of Chiplets' Interface

The two routing options on 3 layers

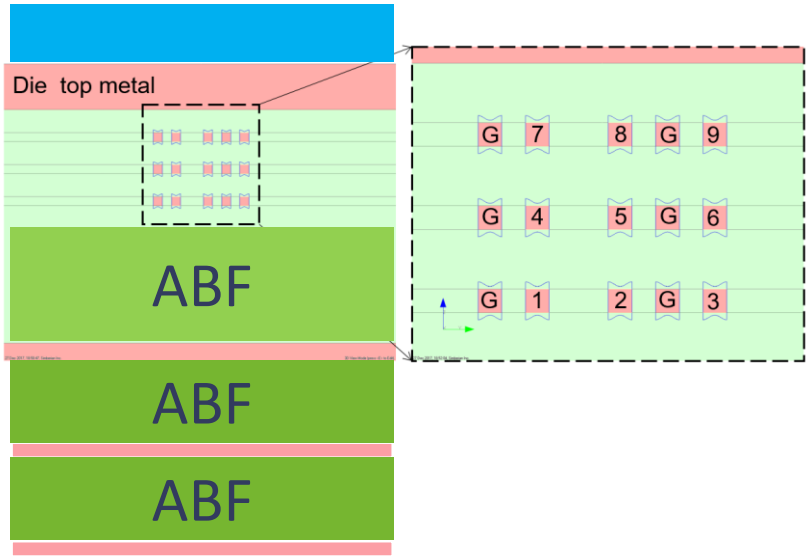
SGS (Signal-Ground-Signal) stackup

1700 signals/2 layers

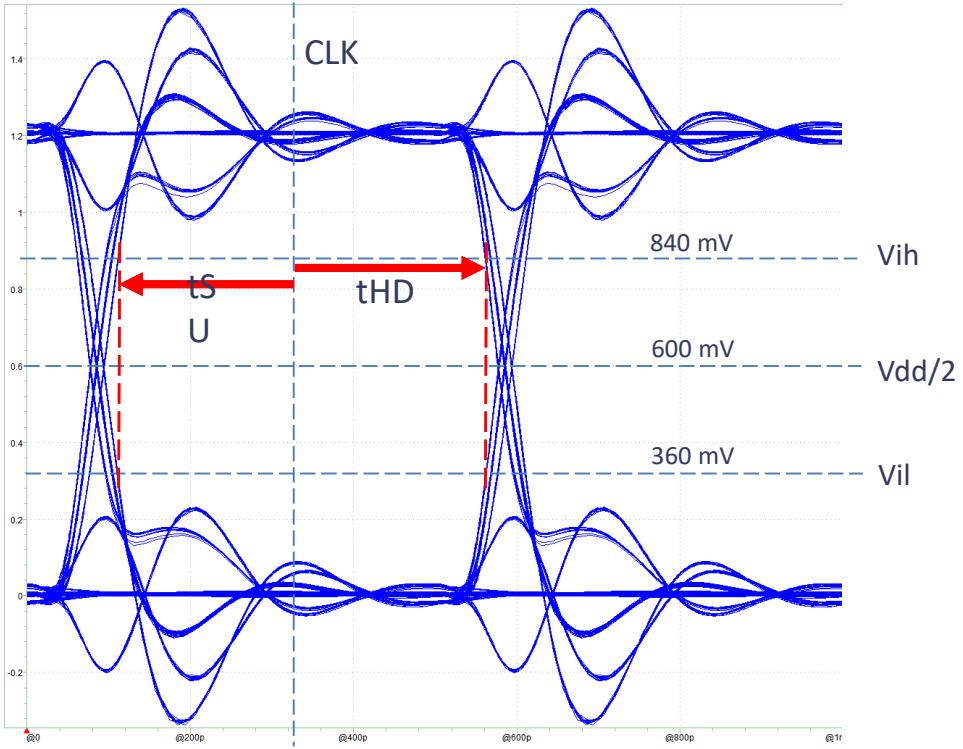


CPG (Co-Planar Ground)

1700 signals /3 layers… + GNDs

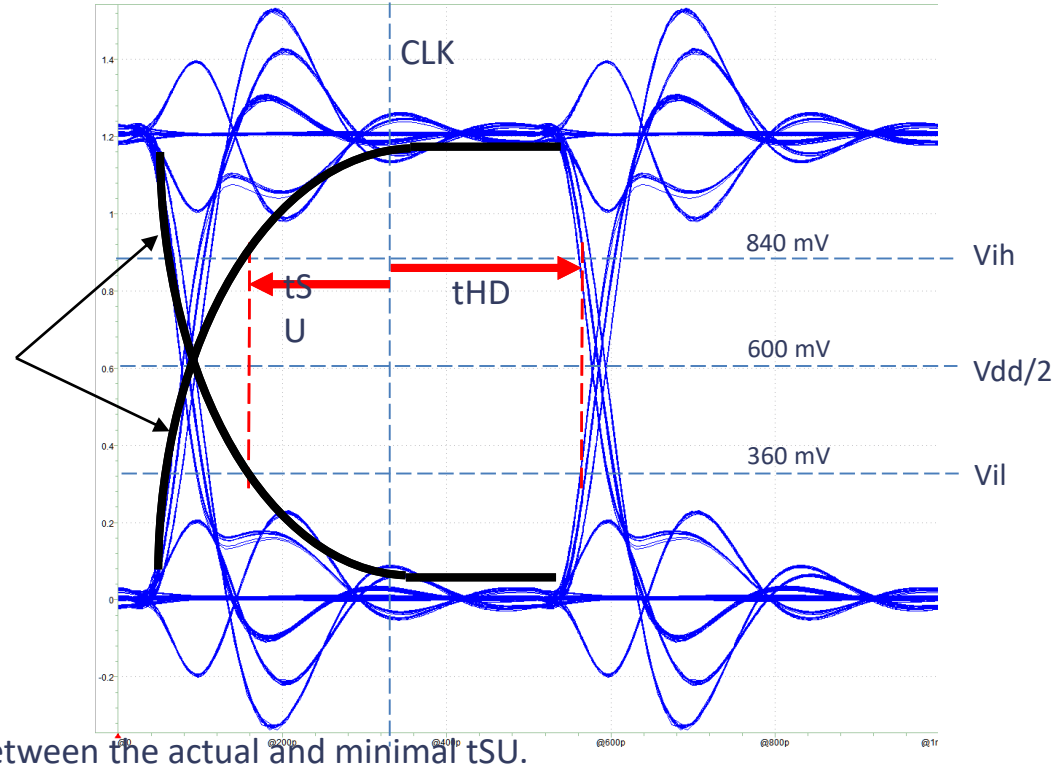


Eye Quality Metrics: tSU/tHD ⇔ Noise



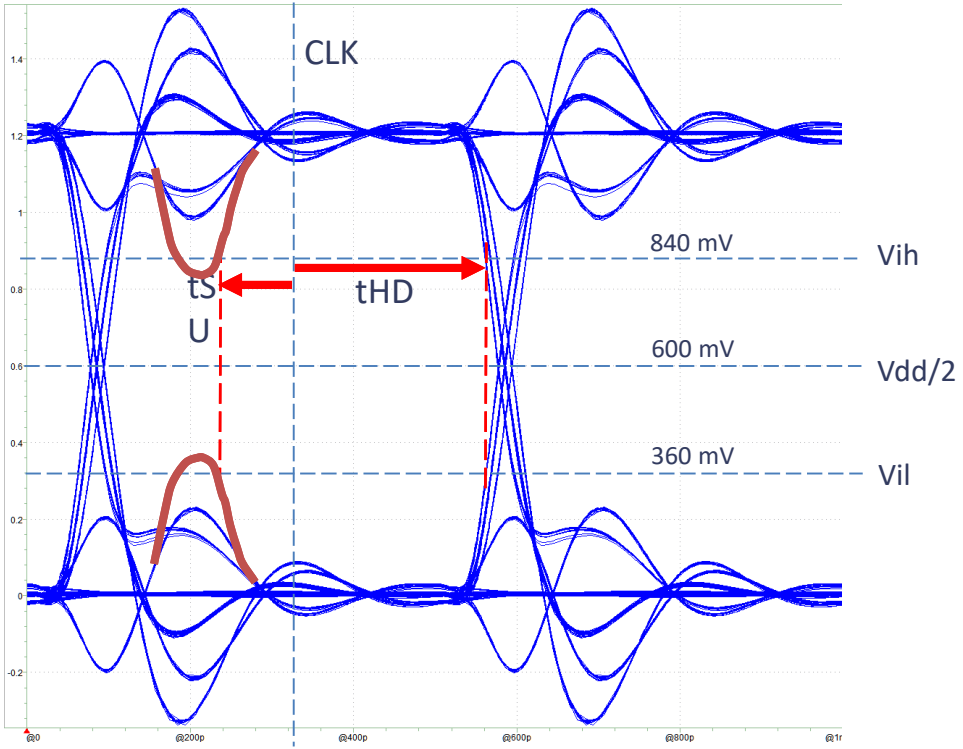
Silicon RC edge eats into tSU margin *)

RC-edge
on Silicon



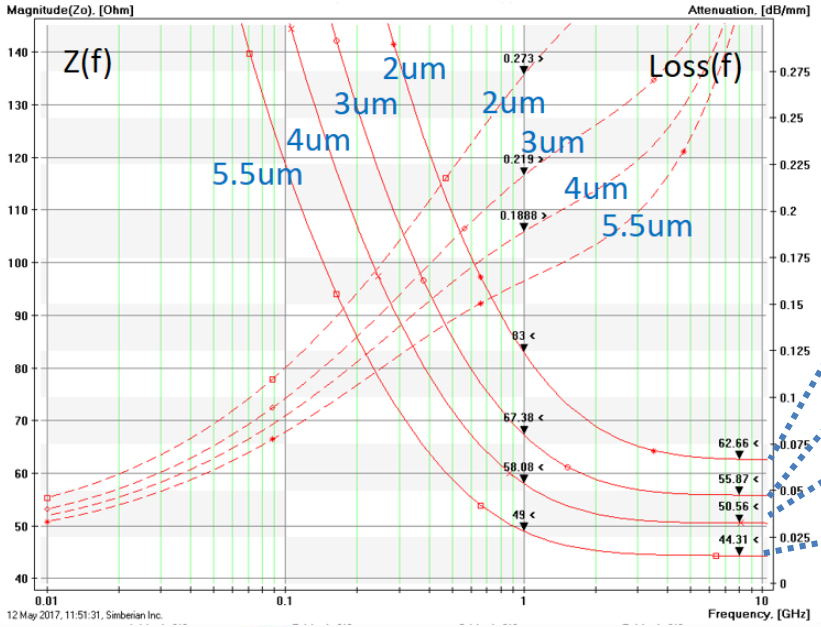
*) Margin is the delta between the actual and minimal tSU.

Want less loss? Be careful what you wish

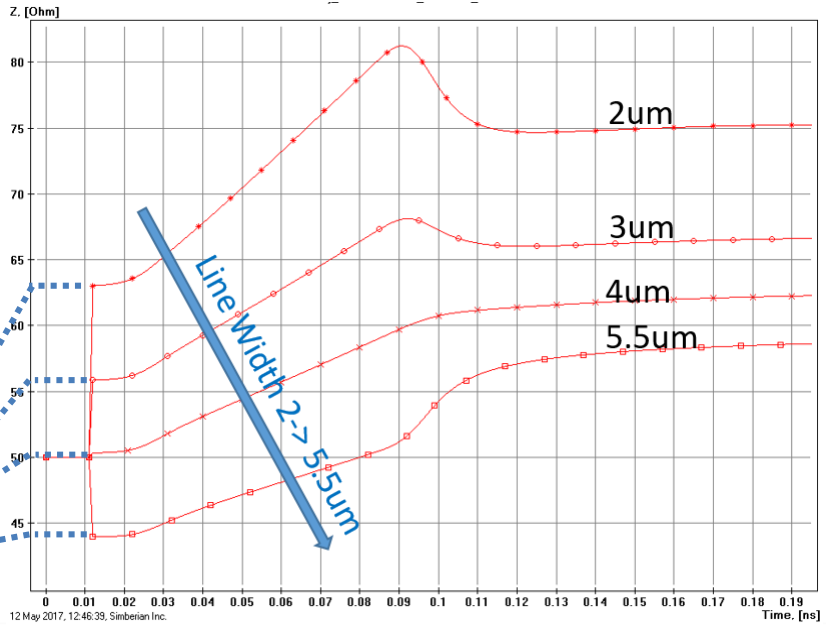


Line parameters

Z(f) & Loss(f) vs. trace width

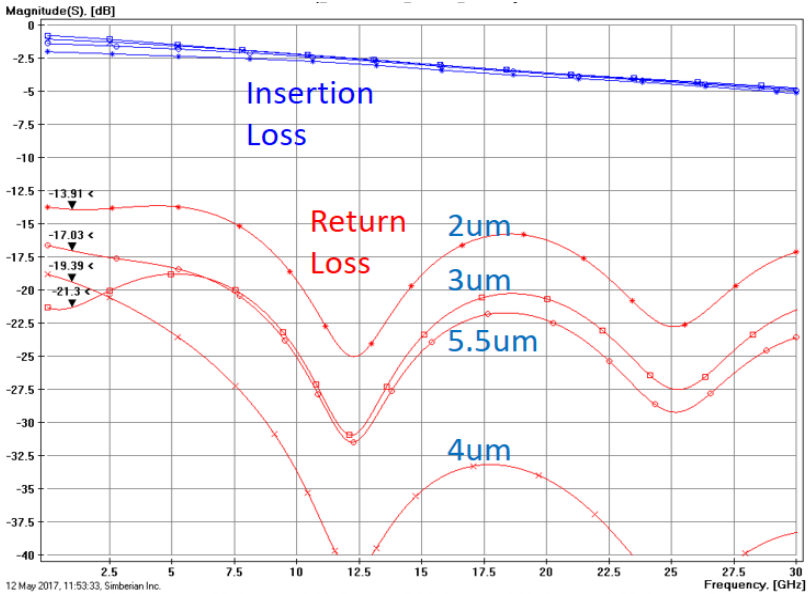


TDR (*effective* Z) vs. trace width

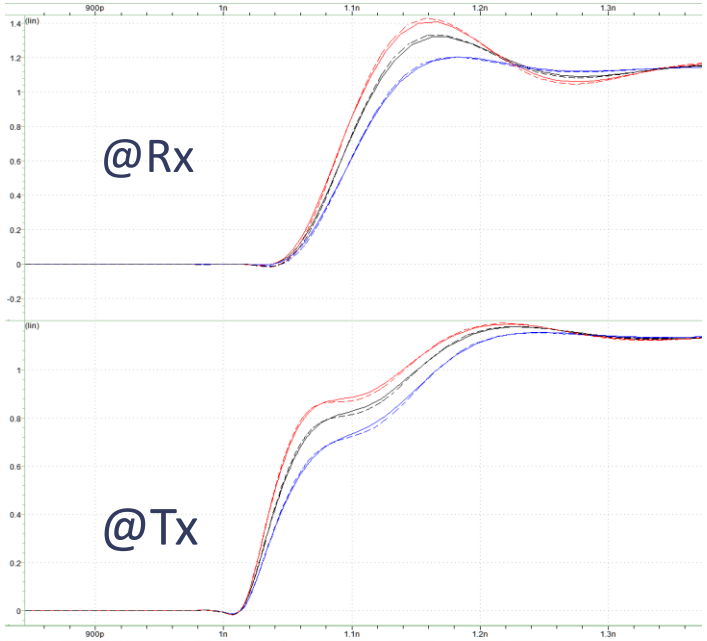


Minimal model frequency bandwidth?

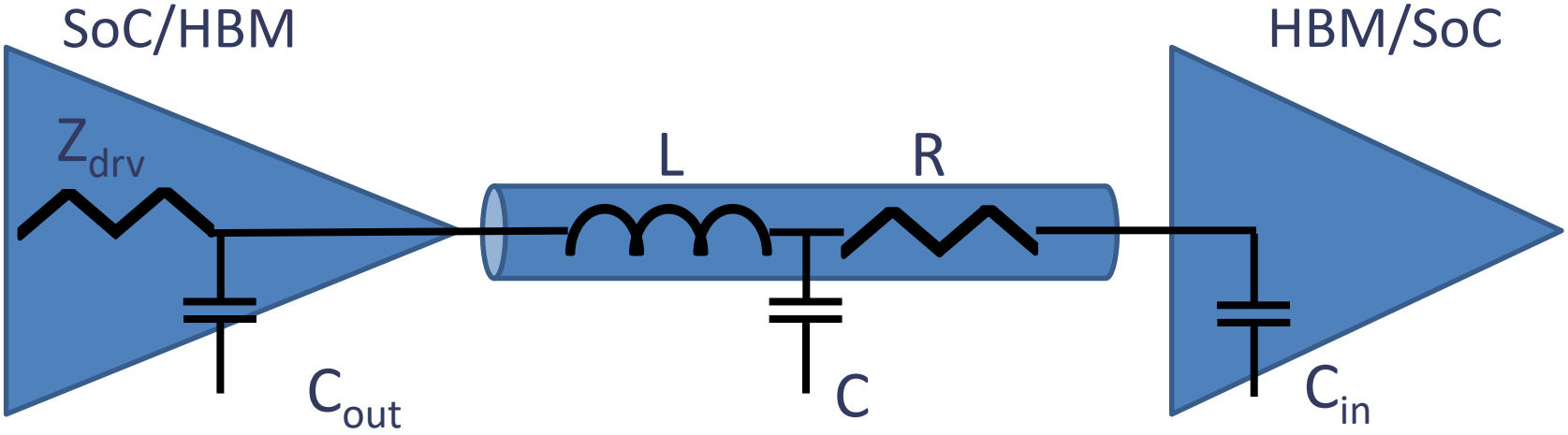
Insertion and Return Loss

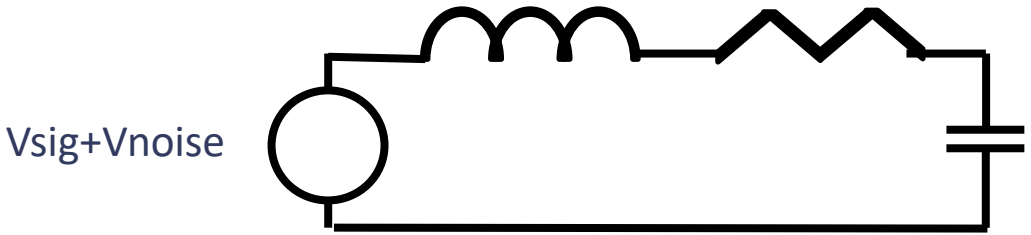


6GHz (solid) vs. 20GHz (dashed) for 3 Tx strength values.



Why does it ring? It's an oscillator!





$$\omega_0^2 = 1/LC$$

$$\omega^2 = \omega_0^2 - \gamma^2$$

No ringing without C_{out} & C_{in} – only Jitter!!

Parameters

edge

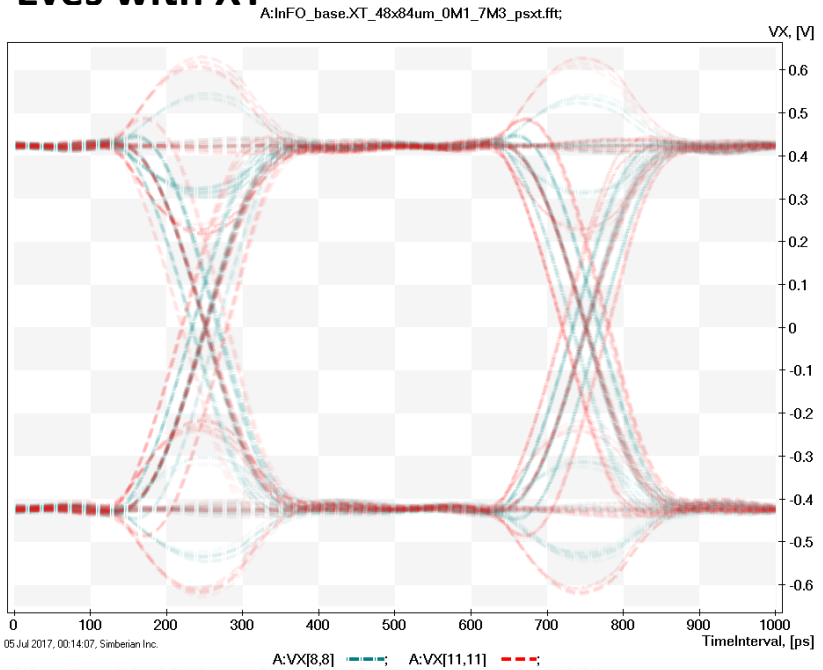
center

Eye Analyzer

Show Eye Metrics: Selected Auto-open

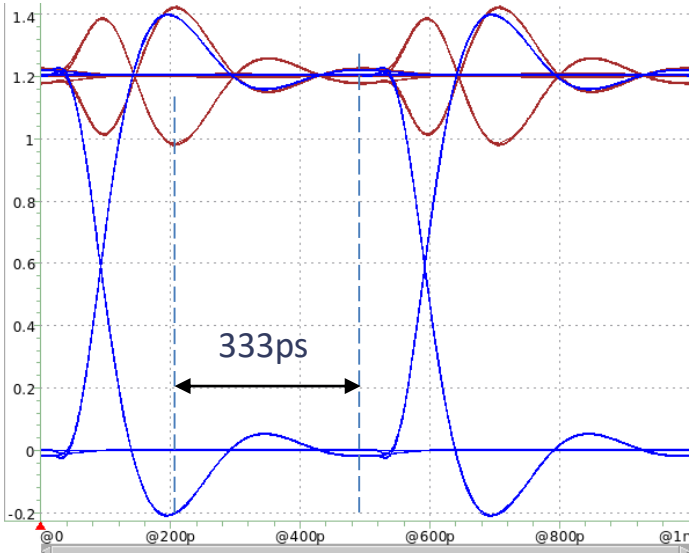
Parameter	InFO_base.XT_48x84um_0M1_7M3_psxt.fft: T_xt[8,8]	InFO_base.XT_48x84um_0M1_7M3_psxt.fft: T_xt[11,11]
Eye Level Zero (V)	-0.422958	-0.422877
Eye Level One (V)	0.4226	0.422664
Eye Level Mean (V)	-0.000394269	0.00134397
Eye Amplitude (V)	0.845558	0.845541
Eye Height (V)	0.813286	0.808479
Eye Width (UI)	0.922395	0.872284
Eye Opening Factor	0.961833	0.956168
Eye Signal to Noise	76.2806	81.1965
Eye Rise Time (20-80) (UI)	0.173381	0.17073
Eye Fall Time (80-20) (UI)	0.172278	0.170846
Eye Jitter (PP) (UI)	0.0776053	0.127716
Eye Jitter (RMS) (UI)	0.0258998	0.045982

Eves with XT



Free oscillations with 3GHz natural frequency

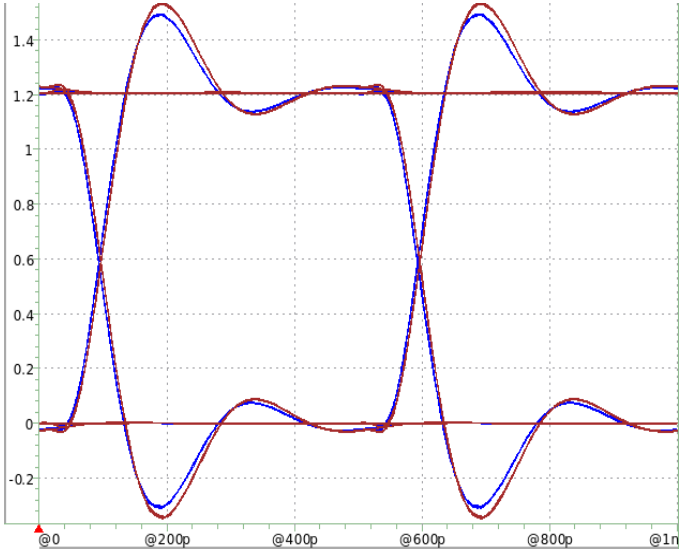
Victim is quiet-high



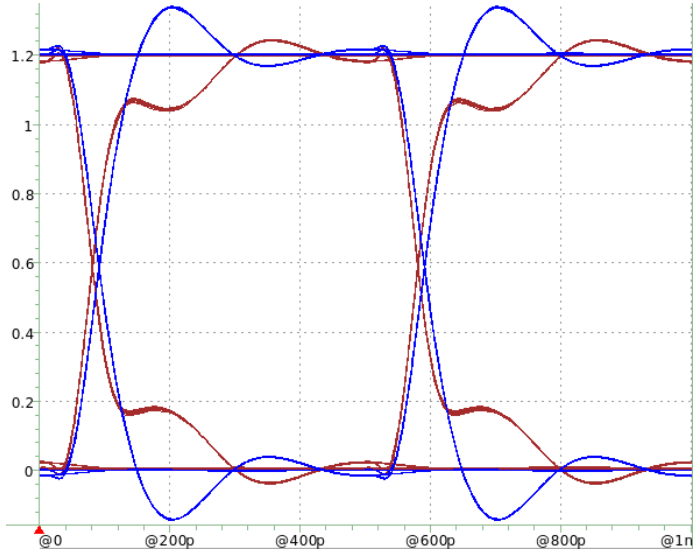
- 3GHz natural oscillation frequency
- Under-dampened
- Rings out within 1UI (almost)

Two more types of crosstalk

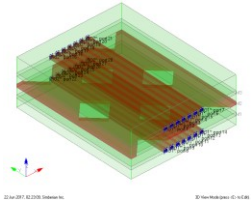
Victim/aggressor in phase



Victim/aggressor out of phase

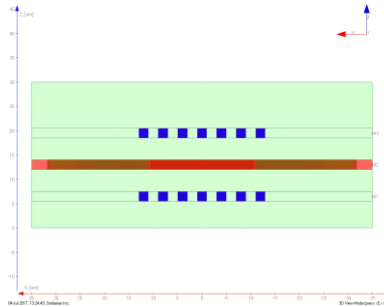


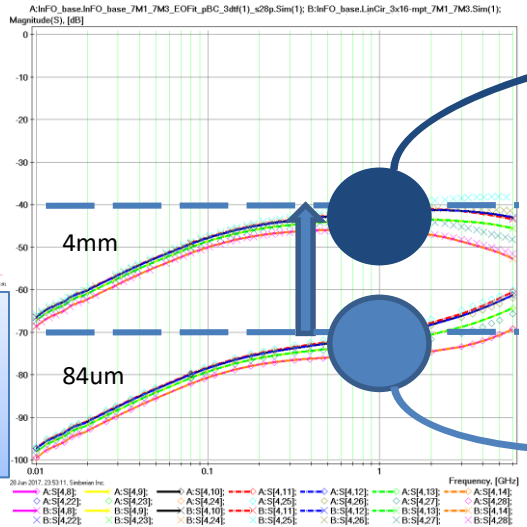
Crosstalk Coupling across M1/M3 layers (through M2 GND Mesh) vs. Coupling Within M3 layer

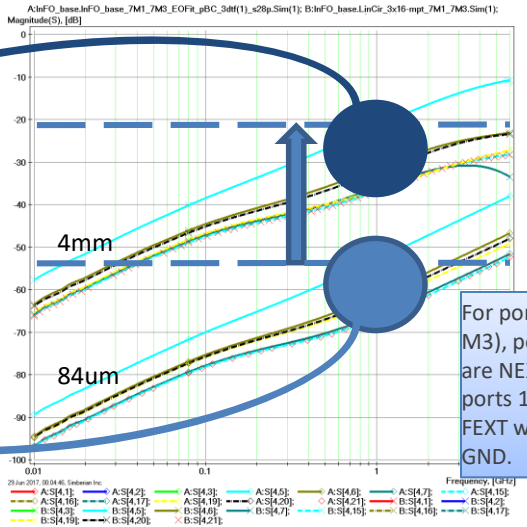


Across M3/M1 **is < -40dB @1GHz**

Within M3 **is < -21dB @1GHz**







4mm

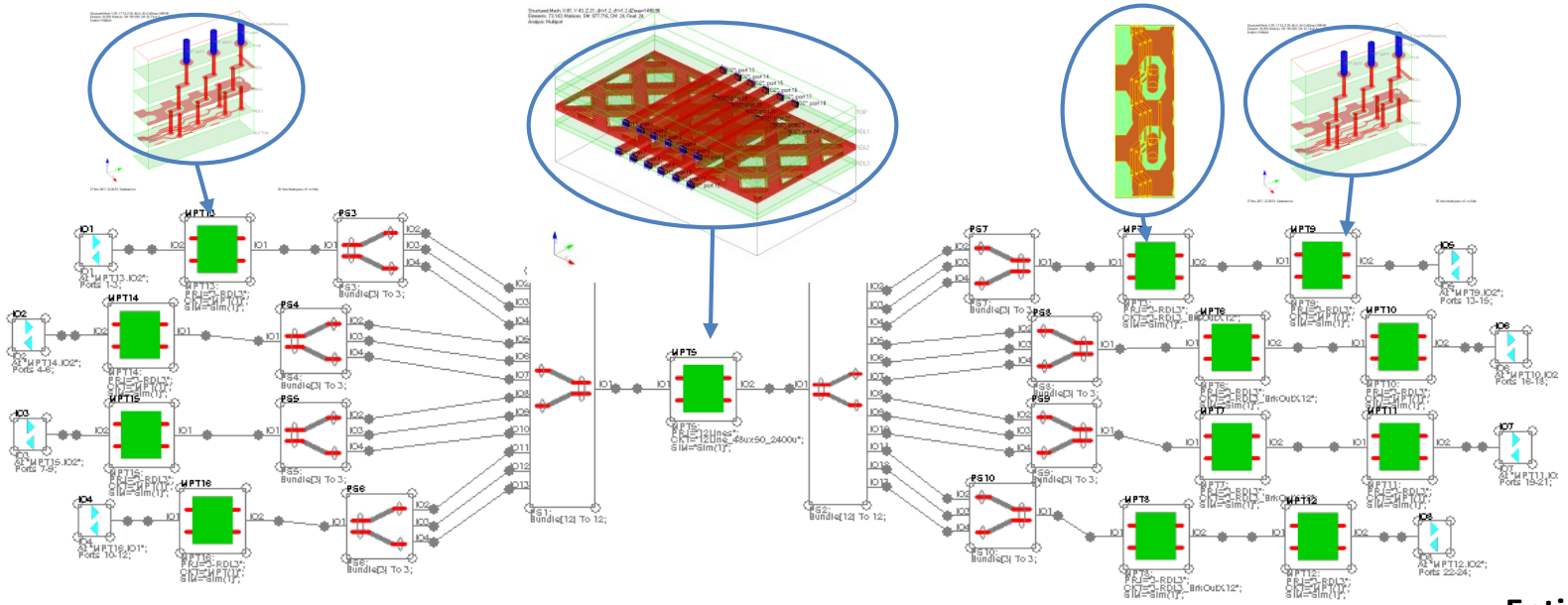
84um

For port4 (in M3), ports 8-14 are NEXT and ports 22-28 are FEXT across M2 GND.

For port4 (in M3), ports 1-7 are NEXT and ports 15-21 are FEXT within M2 GND.

Equivalent Circuit Schematic

HBM



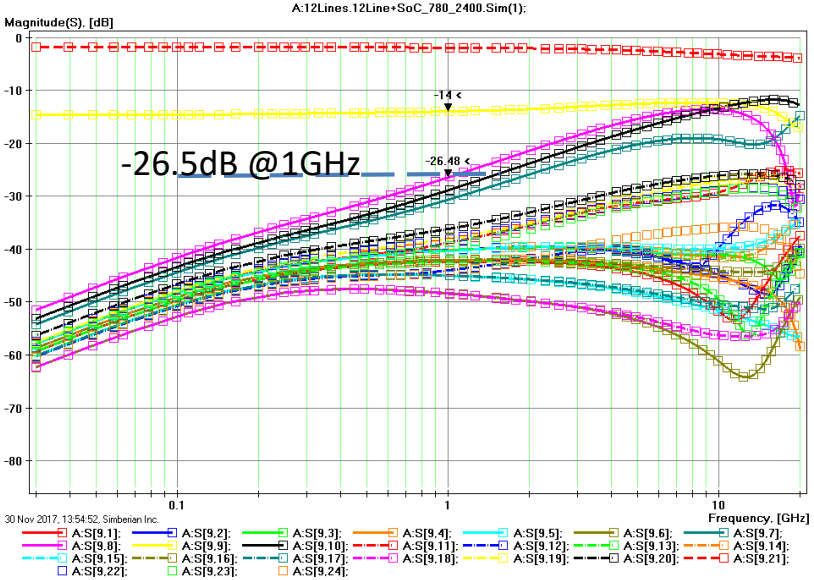
SoC

Max Xtalk @1GHz [dB]	**-54**	**-28.3**	**-32**	**-54**	**-26.5**
Max Return Loss @1GHz [dB]	**-37**	**-17**	**-22**	**-37**	**-14**

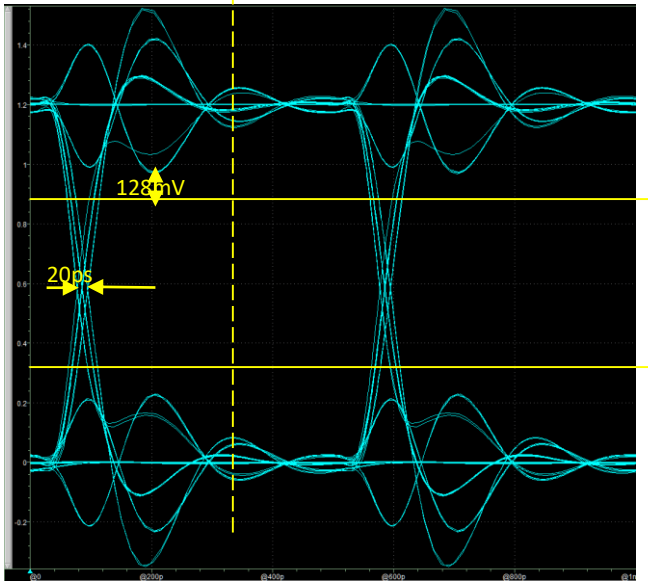
Entire Bus

Crosstalk in 12-Line s24p Mode

S[9,j] of the entire ckt



Eye diagram (15mA, FFFF,1.2V,110C IO ckt & 90C Interconnect)

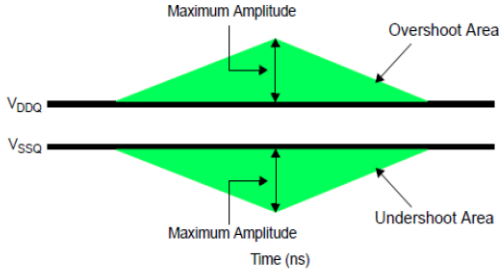


HBM2 JEDEC specification JESD235B

8.8 Overshoot/Undershoot

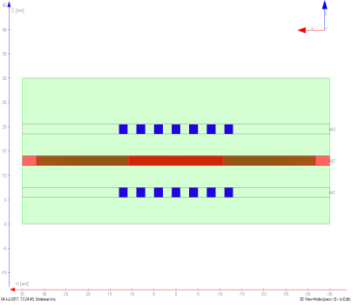
Table 56 — Overshoot/Undershoot Specification for R[5:0], C[7:0], DQ[127:0], DM[15:0], DBI[15:0]

Parameter	1.0 Gbps (BOL)	2.0 Gbps (EOL)	Unit	Notes
Maximum peak amplitude allowed for overshoot area	0.35	0.35	V	
Maximum peak amplitude allowed for undershoot area	0.35	0.35	V	
Maximum overshoot area above V_{DDQ}	0.18	0.09	V-ns	
Maximum undershoot area below V_{SS}	0.18	0.09	V-ns	

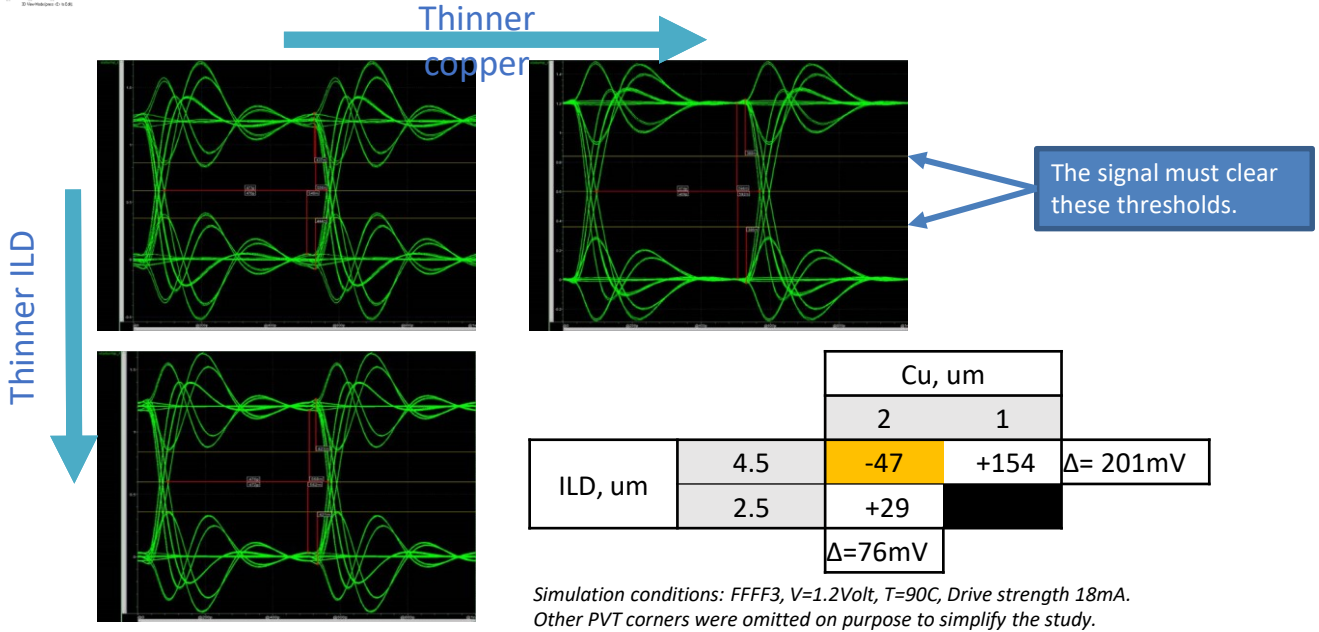


PASS !!!

Figure 88 — Overshoot, Undershoot Definition



Noise Margin vs. Dielectric & Cu thickness

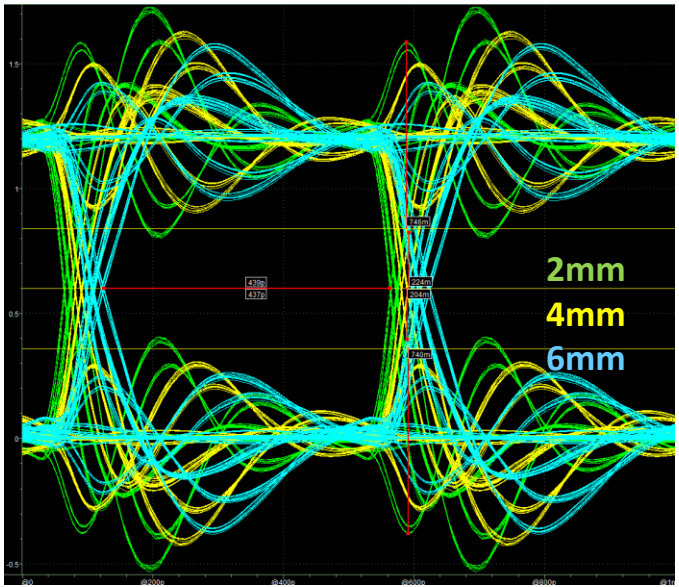


ILD, um	Cu, um: 2	Cu, um: 1	
4.5	-47	+154	Δ= 201mV
2.5	+29		
	Δ=76mV		

Simulation conditions: FFFF3, V=1.2Volt, T=90C, Drive strength 18mA.
Other PVT corners were omitted on purpose to simplify the study.

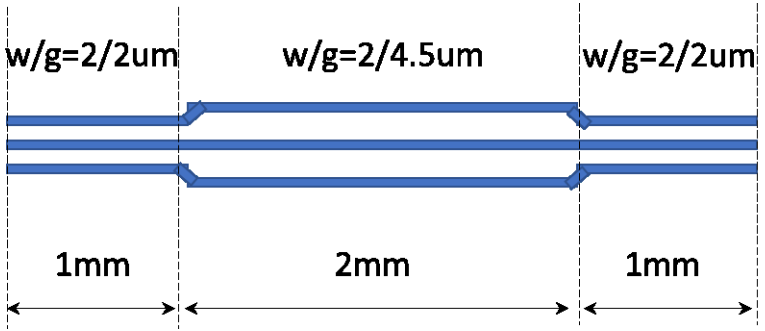
Noise Margin figure vs. Bus Length

Eyes (Middle section: 2 / 4 / 6 mm)



Noise Margin

	Length of the Middle section, mm		
	2	4	6
Noise Margin, mV	-47	+53	+96

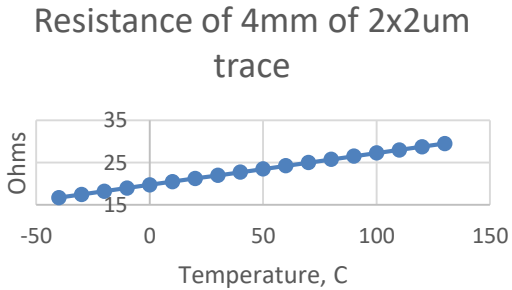


What is important in your model?

- Model accuracy is very important because this is the model of under-dampened oscillator coupled to other such oscillators.
  - Amplitude is very sensitive to model parameters.
  - Example: use of static field solver is incorrect as it assumed well developed skin effect, which is not the case here. Use full-wave solver with correct DC asymptotic behavior. If HFSS, make sure to mesh inside traces (no SIBC !!).

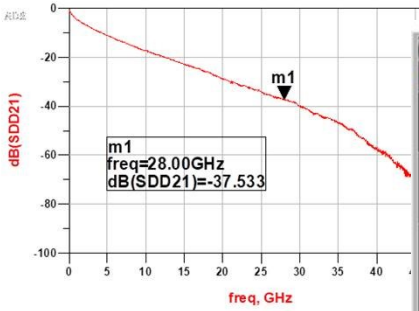
What is important in your design?

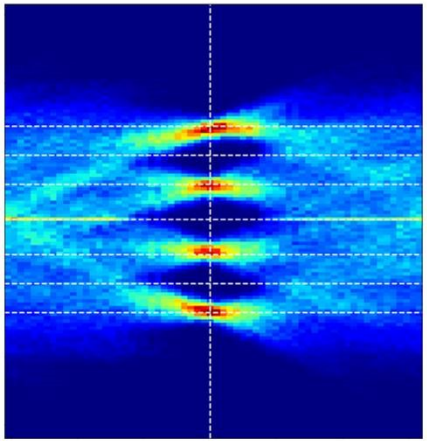
- Conclusions of this work apply to other very short reach *wide* interfaces on organic non-silicon substrate, whenever loss is insufficient to dampen LC-talk oscillations.
- More loss helps:
  - Higher nominal metal sheet resistance.
    - Thinner metal.
    - Higher temperature.
    - CuX alloy with higher resistance?
- Less crosstalk helps:
  - Thinner dielectric reduces crosstalk within layer (the dominant type) but increases crosstalk across GND plane.
  - Smaller perforation holes reduces crosstalk across GND plane.

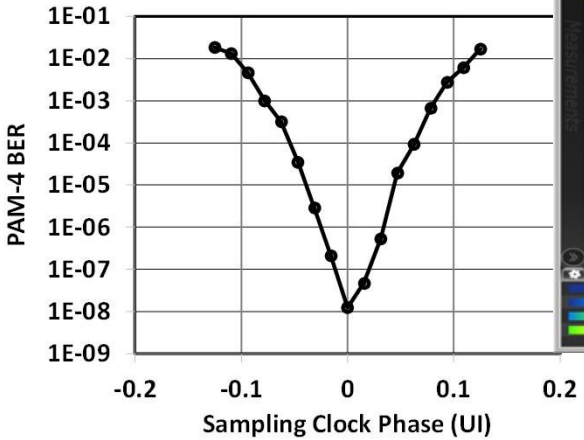


112G PAM4 Single-Ended Channel in 7-2-7 Package Substrate: Via Design & Channel Analysis

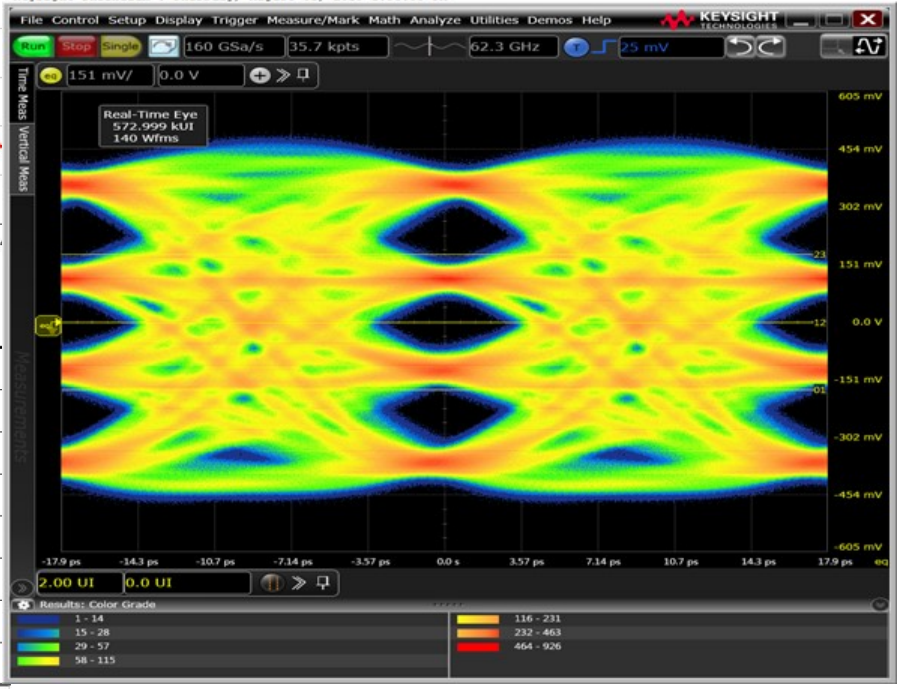
112Gbps 7nm – 37dB Die-to-die Loss





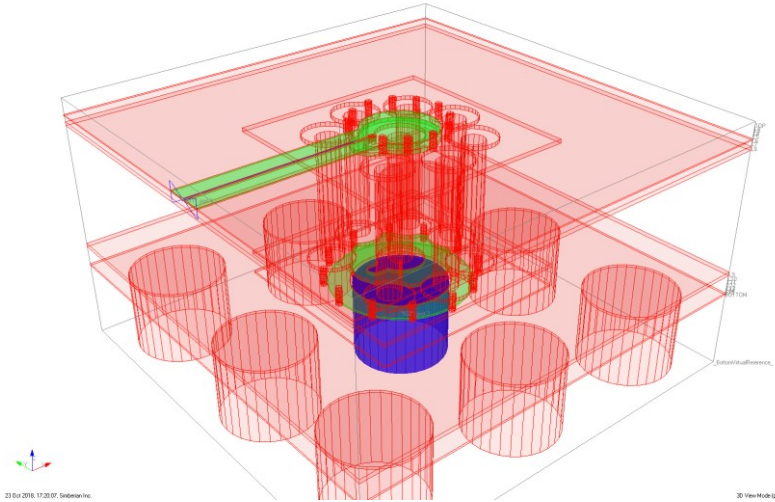


112Gbps Near-end TX eye with Scope FFE

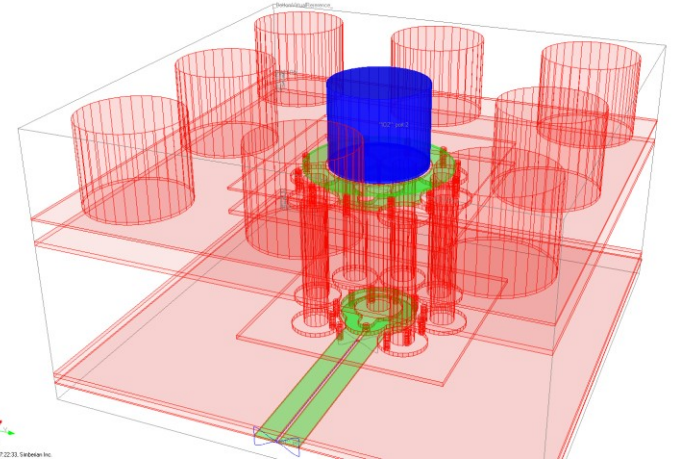


3D geometry of the via

Top view

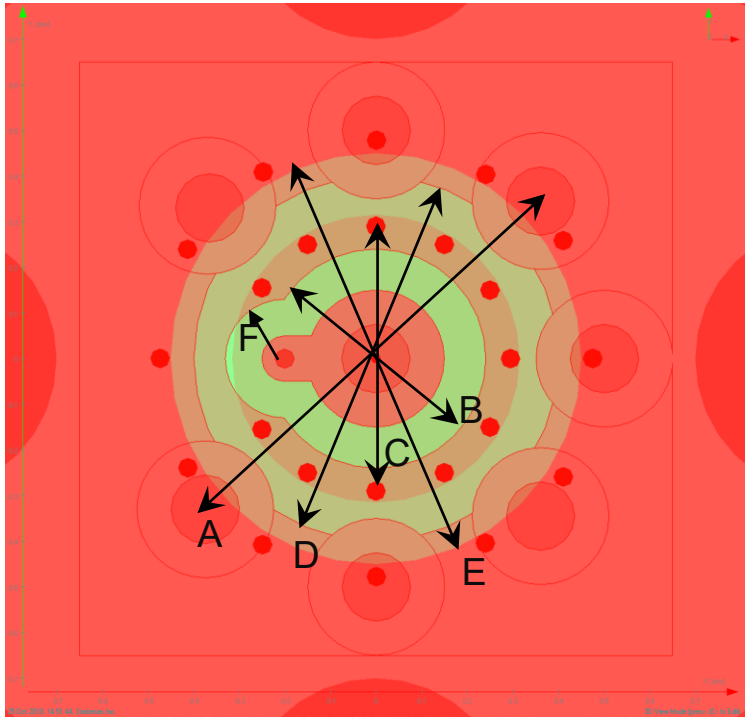


Bottom view

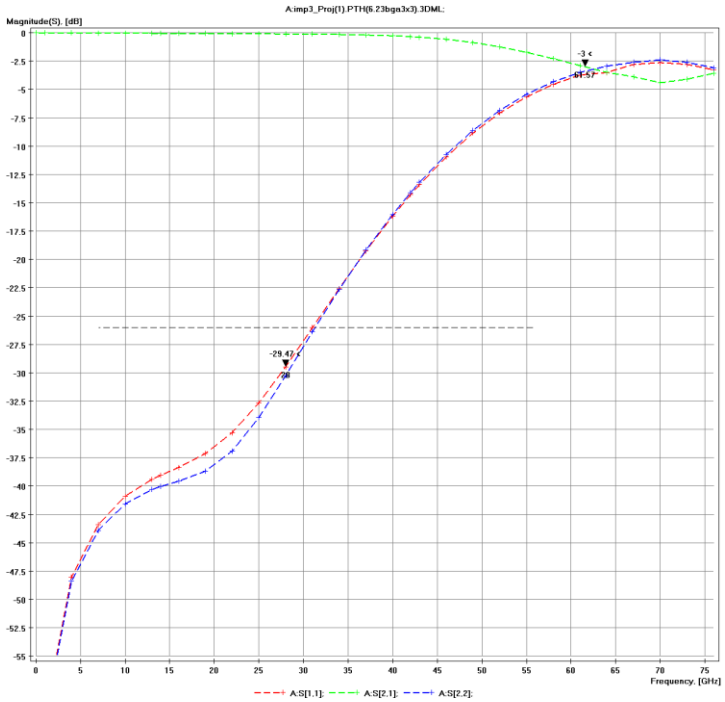


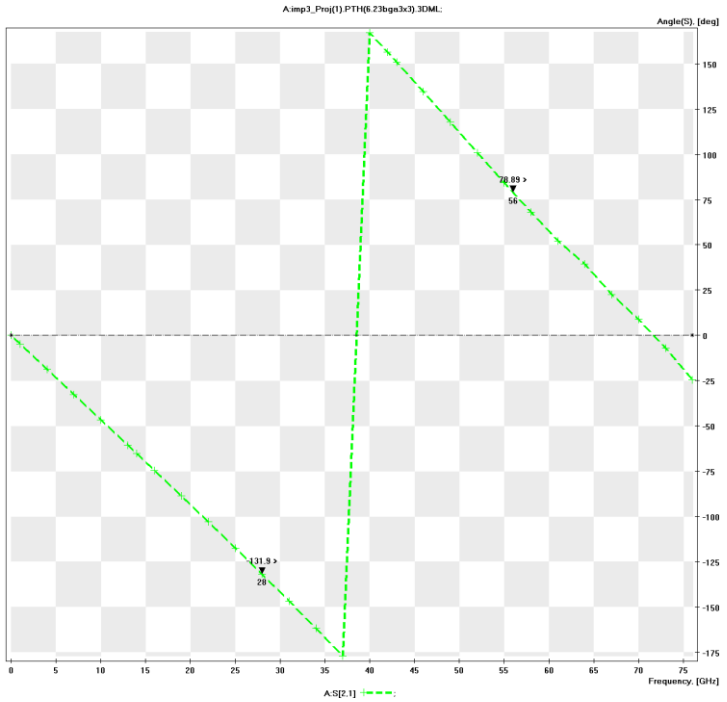
The best via (BW=61.7GHz)

Dimension	Final	Layers
A (dist)	1000	L8,9
B (void)	480	L2-L8
C (dist)	580	L2-L8
D (void)	800	L9
E (void)	900	L10-L16
F (void)	130	L2-L16



RL(@28GHz) -29dB, Bandwidth 61.5GHz

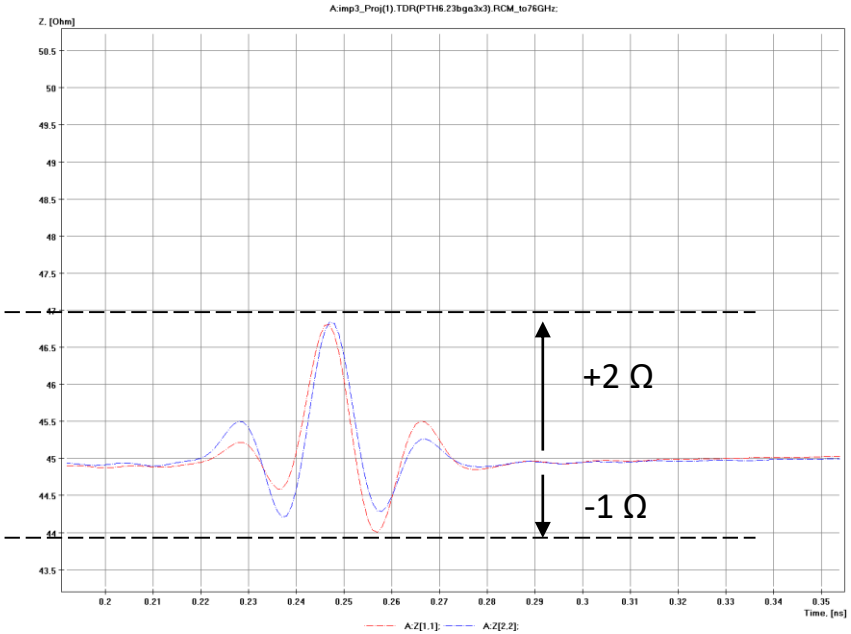




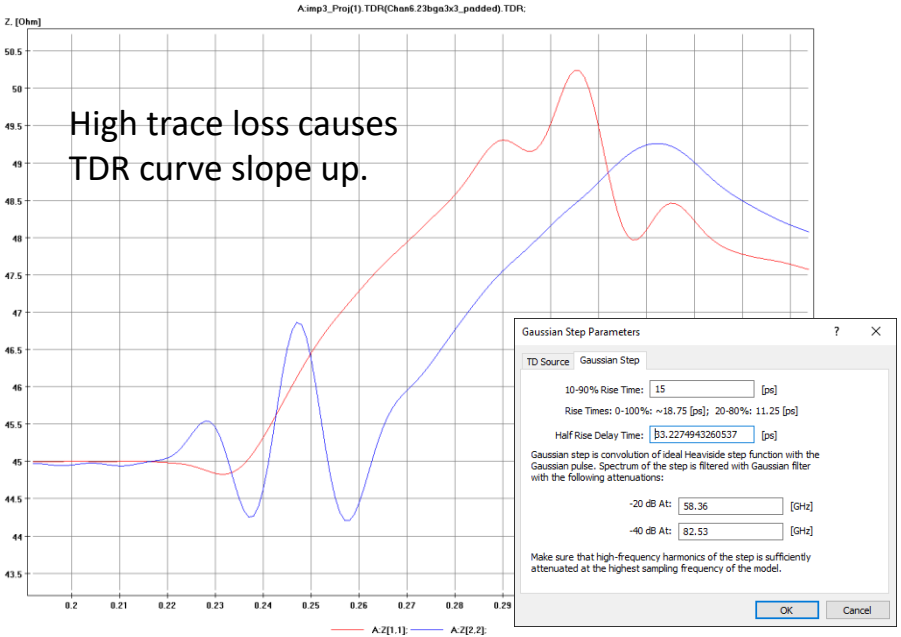
The via is 132° , i.e. almost 1/3d wavelength at Nyquist frequency

Via + Channel: comparison of TDR

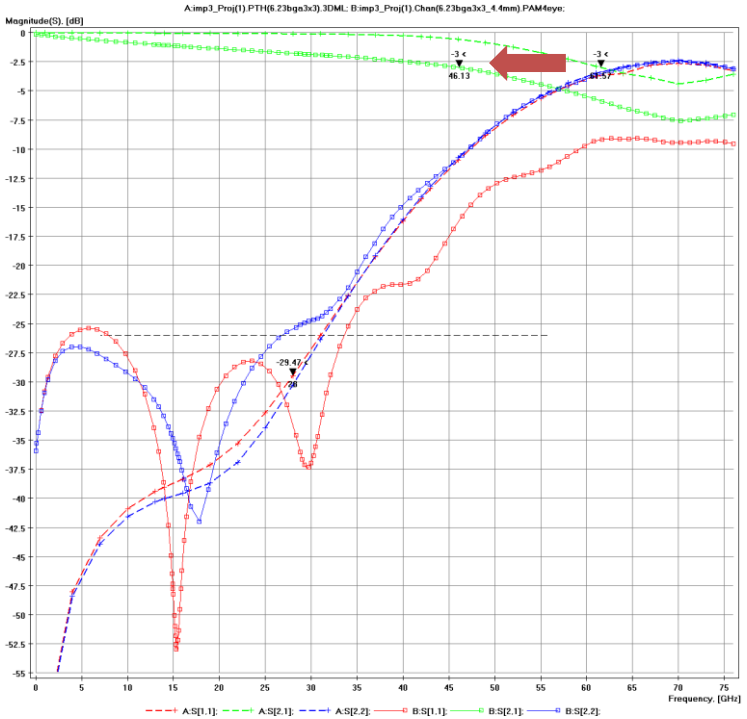
TDR of the Via



TDR of Rx2 Channel (4.4mm)

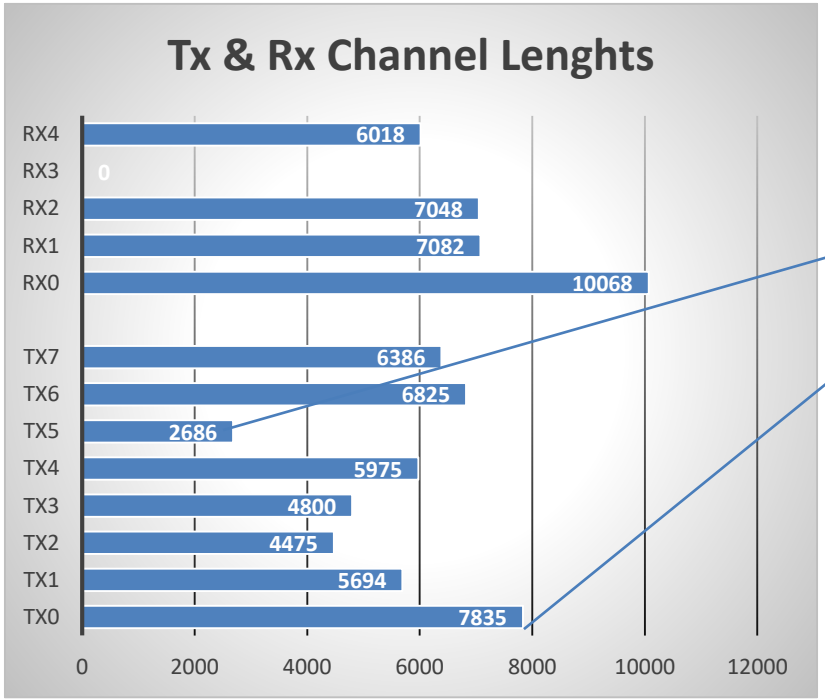


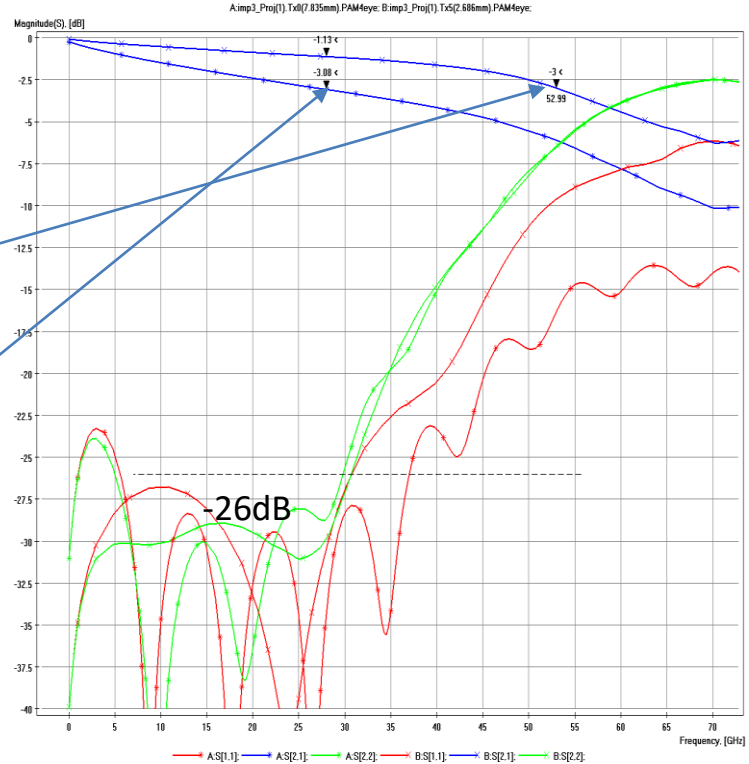
Via and Tx2 (4.4mm) Channel (Bump to Ball)



Combining the via and the 4.4mm trace into one channel reduced BW from 61GHz to 46GHz.

TV Channel Lengths & Electrical Performance Range

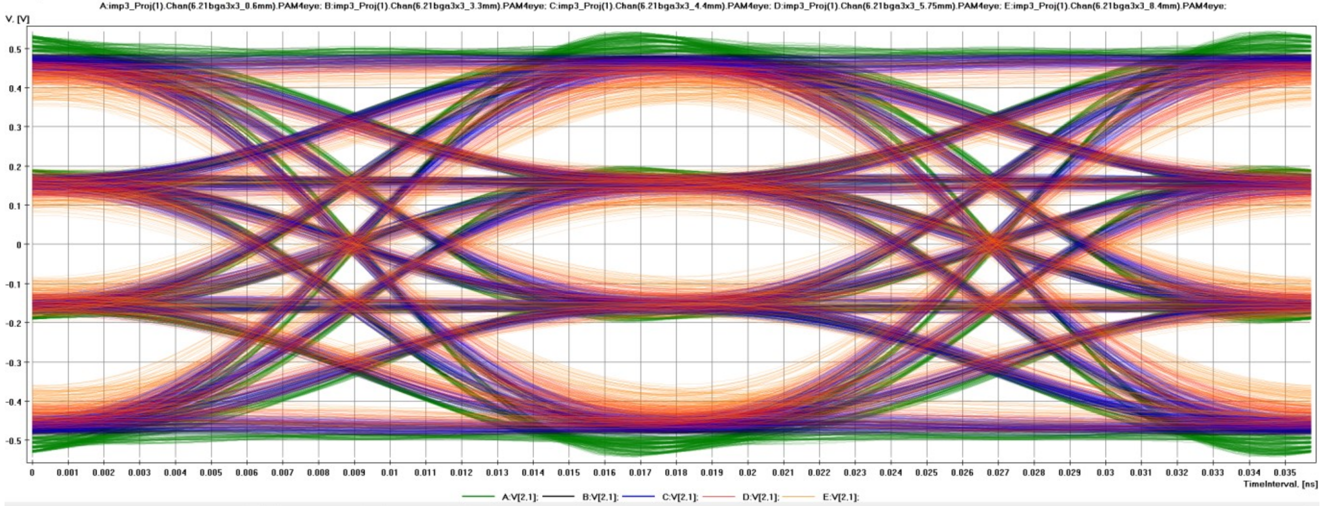




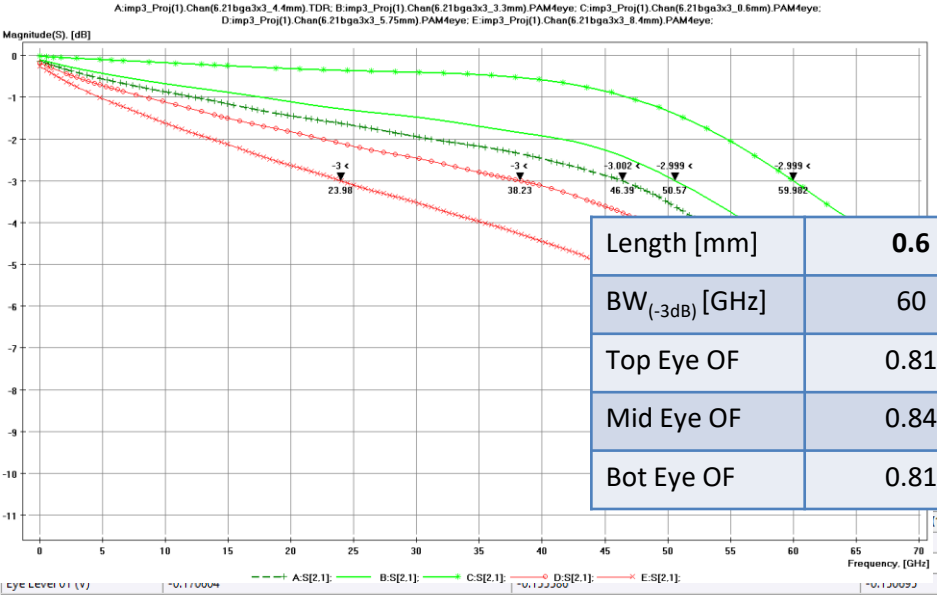
Tuning trace length is NOT important as losses are high

0.6mm	3.3mm	4.4mm	5.75mm	8.4mm

Parameter	imp3_Proj(1).Chan(6.21bga3x3_0.6mm).PAM4eye: T[2,1]	imp3_Proj(1).Chan(6.21bga3x3_3.3mm).PAM4eye: T[2,1]	imp3_Proj(1).Chan(6.21bga3x3_4.4mm).PAM4eye: T[2,1]	imp3_Proj(1).Chan(6.21bga3x3_5.75mm).PAM4eye: T[2,1]	imp3_Proj(1).Chan(6.21bga3x3_8.4mm).PAM4eye: T[2,1]
Eye Level 11 (V)	0.507975	0.468413	0.454618	0.438241	0.408753
Eye Level 10 (V)	0.170319	0.157546	0.153774	0.146411	0.132958
Eye Level 01 (V)	-0.170604	-0.155586	-0.150695	-0.147956	-0.134785
Eye Level 00 (V)	-0.508209	-0.468679	-0.455103	-0.43759	-0.407995
Upper Eye Height (V)	0.274522	0.263917	0.23704	0.201715	0.142414
Middle Eye Height (V)	0.287739	0.263611	0.236434	0.205923	0.140645
Lower Eye Height (V)	0.272827	0.264222	0.237645	0.202316	0.147722
Upper Eye Width (UI)	0.581818	0.559202	0.537916	0.514856	0.449667
Middle Eye Width (UI)	0.710865	0.668293	0.641685	0.613304	0.526386
Lower Eye Width (UI)	0.580044	0.56408	0.543681	0.514856	0.46031
Upper Eye Opening Factor	0.813023	0.848971	0.787915	0.691208	0.516378
Middle Eye Opening Factor	0.844001	0.841853	0.776546	0.699546	0.5253
Lower Eye Opening Factor	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]



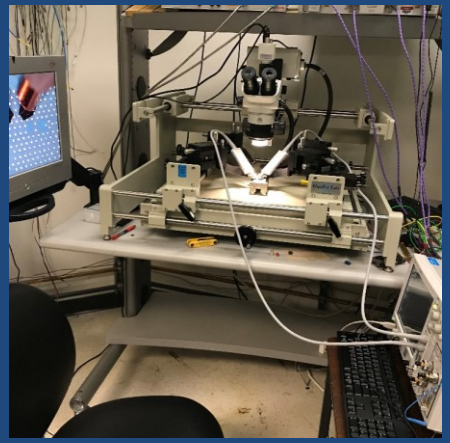
PAM4 Eye Metrics vs. Channel -3dB BW

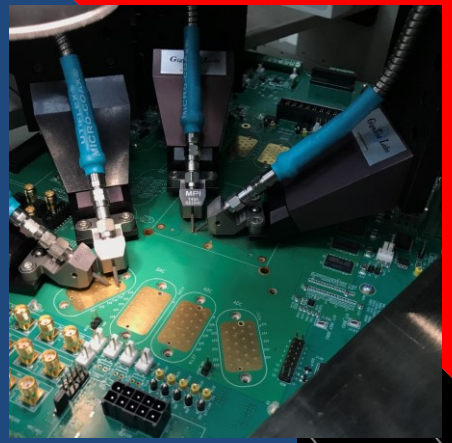


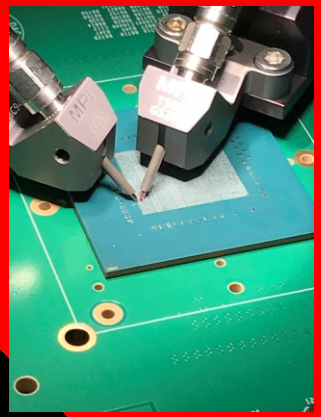
Length [mm]	**0.6**	**3.3**	**4.4**	**5.75**	**8.4**
$BW_{(-3dB)}$ [GHz]	60	50.6	46.4	38.2	24
Top Eye OF	0.81	0.85	0.79	0.69	0.52
Mid Eye OF	0.84	0.84	0.78	0.70	0.53
Bot Eye OF	0.81	0.84	0.78	0.70	0.54

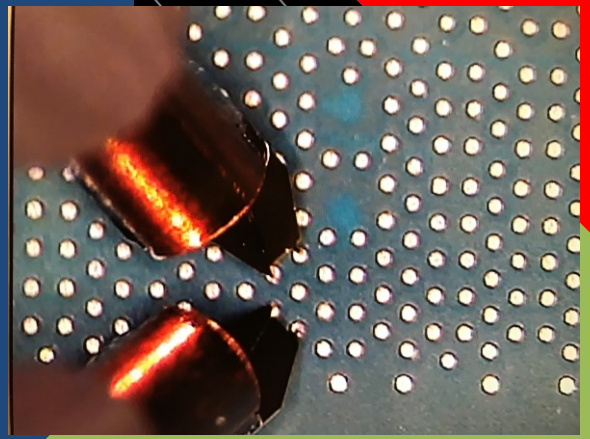
				imp3_Proj(1).Chan(6.21bga3x3_5.75mm).PAM4eye: T[2,1]	imp3_Proj(1).Chan(6.21bga3x3_8.4mm).PAM4eye: T[2,1]
				0.438241	0.408753
				0.146411	0.132958
				-0.147956	-0.134785
Eye Level 00 (V)	-0.508209	-0.468679	-0.455103	-0.43759	-0.407995
Upper Eye Height (V)	0.274522	0.263917	0.23704	0.201715	0.142414
Middle Eye Height (V)	0.287739	0.263611	0.236434	0.205923	0.140645
Lower Eye Height (V)	0.272827	0.264222	0.237645	0.202316	0.147722
Upper Eye Width (UI)	0.581818	0.559202	0.537916	0.514856	0.449667
Middle Eye Width (UI)	0.710865	0.668293	0.641685	0.613304	0.526386
Lower Eye Width (UI)	0.580044	0.56408	0.543681	0.514856	0.46031
Upper Eye Opening Factor	0.813023	0.848971	0.787915	0.691208	0.516378
Middle Eye Opening Factor	0.844001	0.841853	0.776546	0.699546	0.5253
Lower Eye Opening Factor	0.808125	0.843909	0.780679	0.698523	0.540691

Validation of Characteristic Impedance on Package Substrate with Micro-probing and Measurements



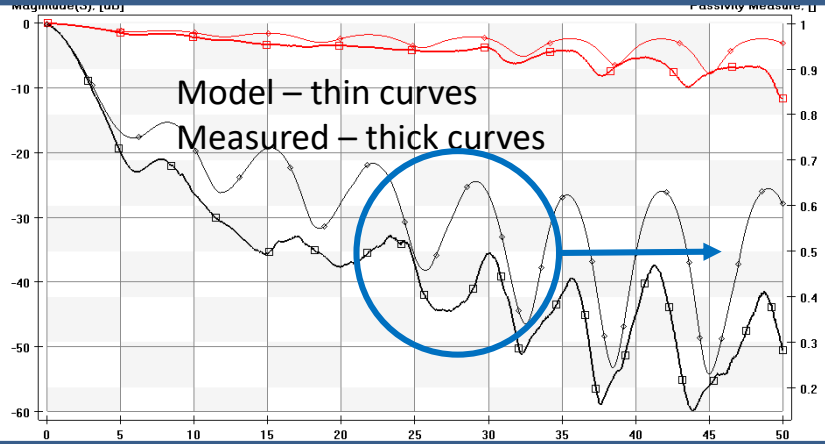


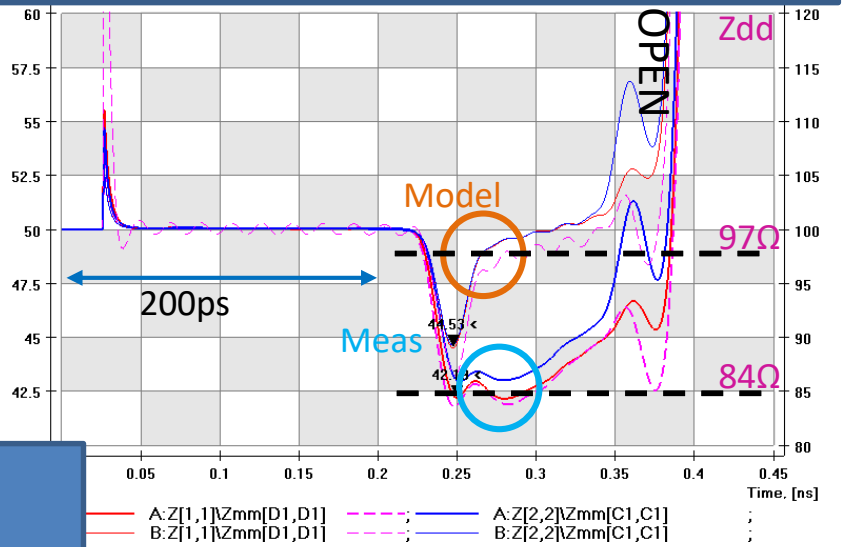




Comparison between HFSS model and 2-port Measurement from bump side with Open BGA

In regard to impedance:
The *package model Zdd* is right on target at ~97Ω but the *actual package* is at ~84Ω, or 13Ω below target impedance. Possibly the actual trace is wider or/and the dielectric layers are thinner than modeled. Cross sectioning can answer this.

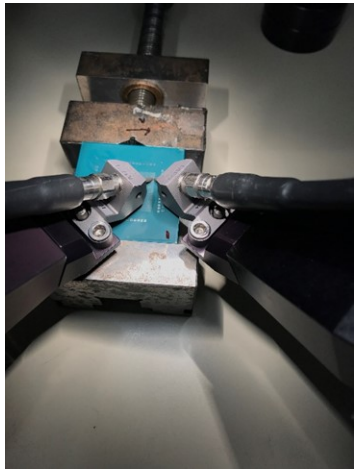


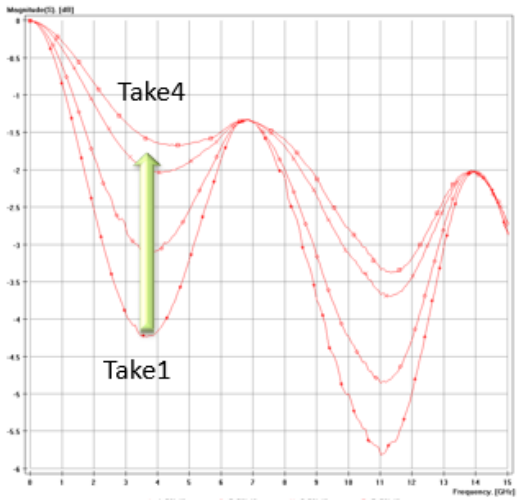


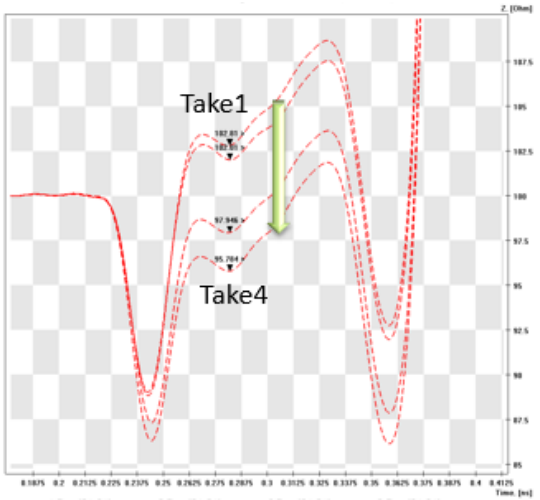
In regard to loss:
Model underestimates the loss. This is seen from
1) lower passivity and 2) TDR curves slope is lower for the model.

Subsequent landing of uProbe reduces Z perceived with TDR

High Contact resistance of SOP (Solder-On-Pad) exaggerates TDR reading up to several Ohms.

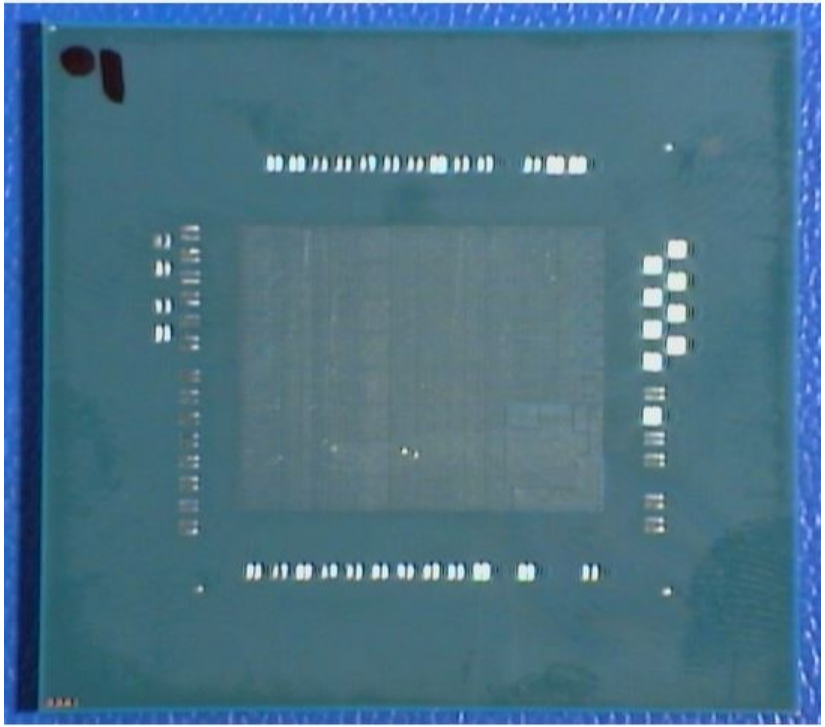


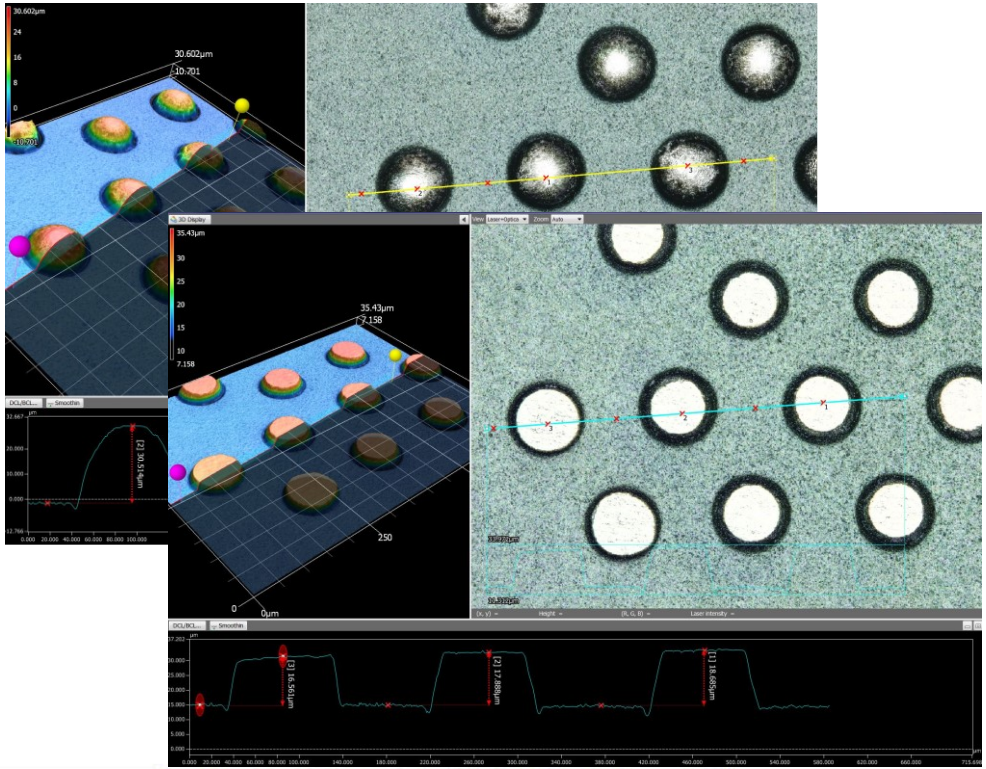




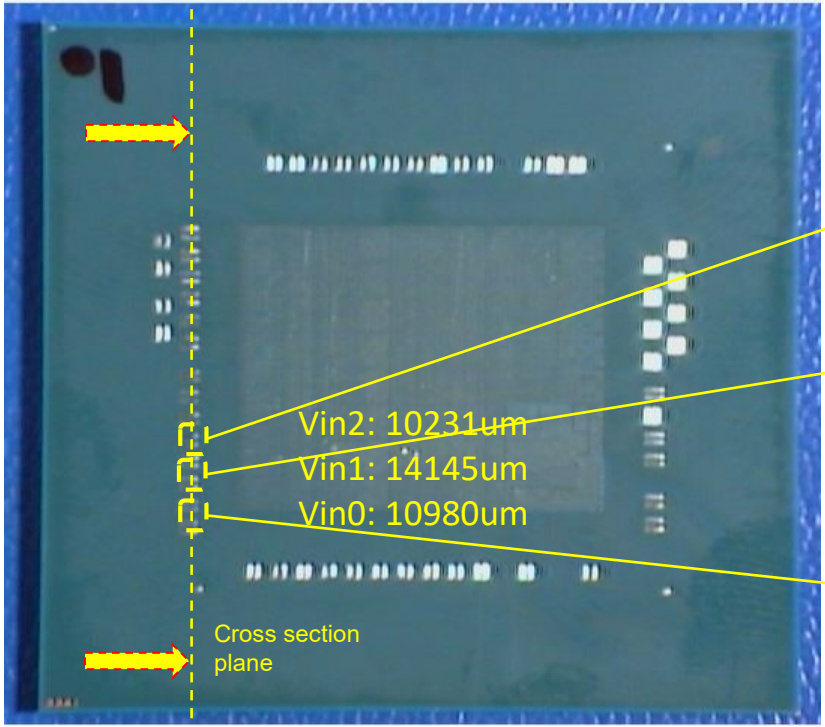
take 1	take 2	take 3	take 4		max-min
102.81	102.01	97.95	95.78		7.0

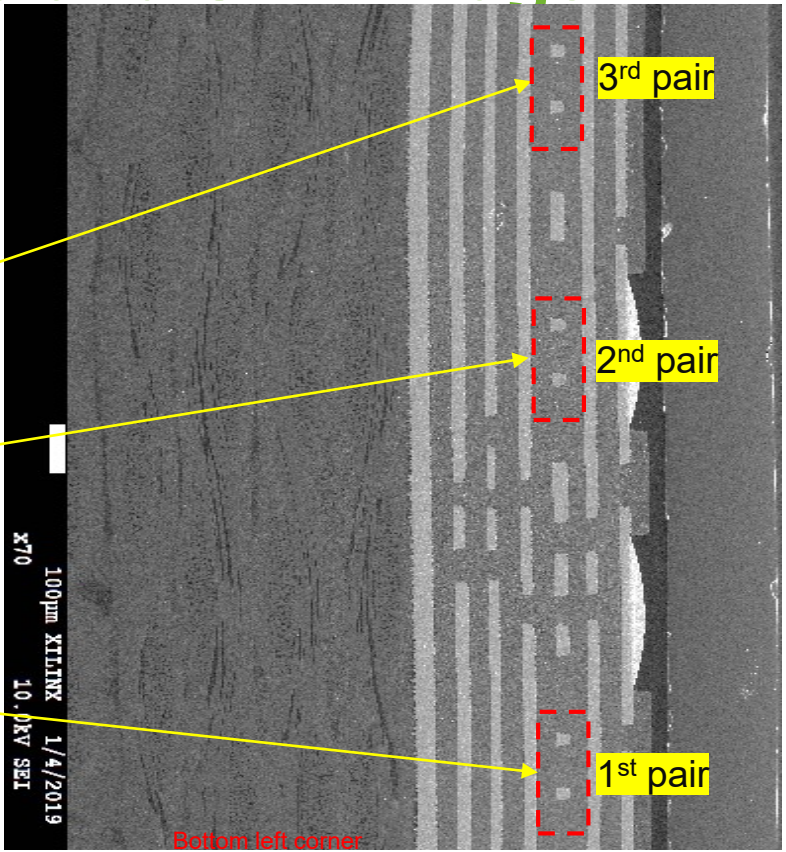
FA Lab: preparation of the Substrate sample



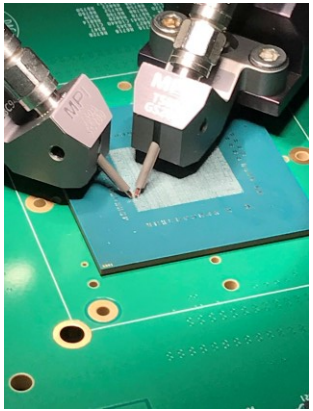


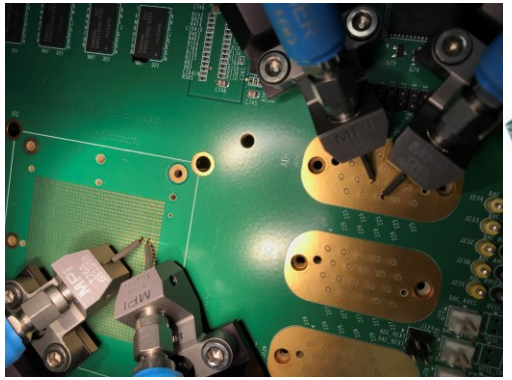
Cross-Sectioning of Substrate and SEM Image



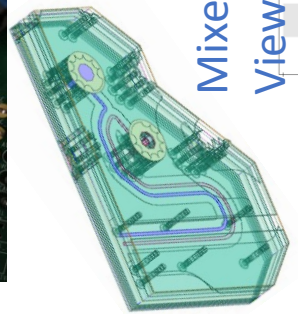


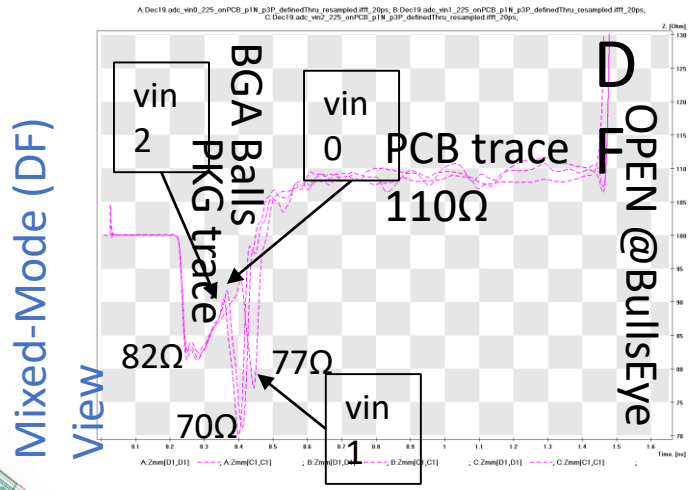
TDR of All Three Channels: PKG+PCB



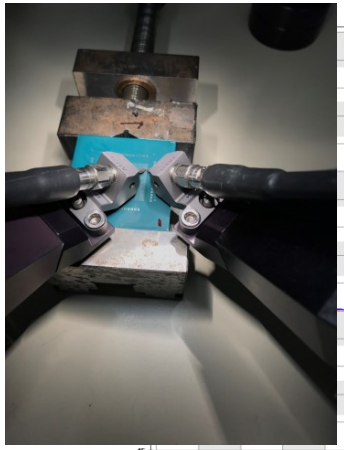


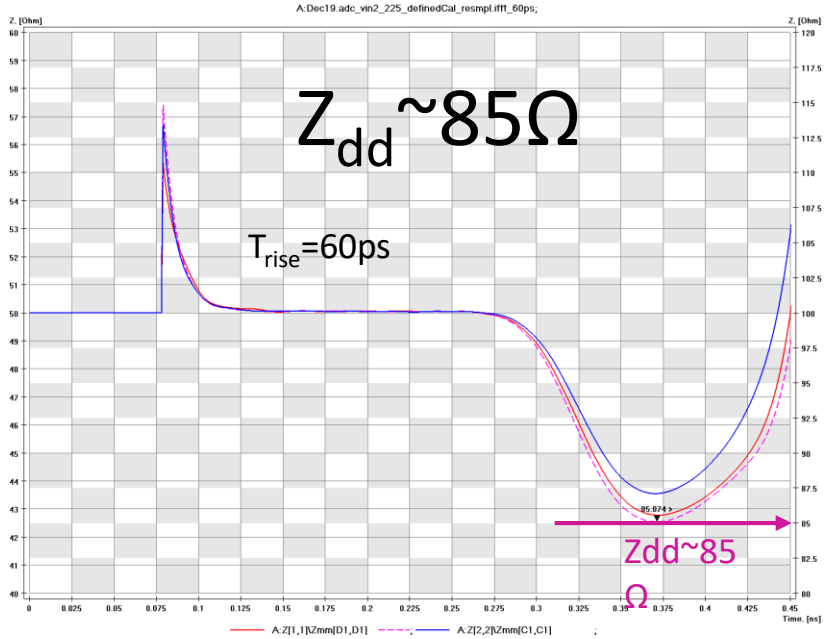
Vin2: 10231um
Vin0: 10980um
Vin1: 14145um



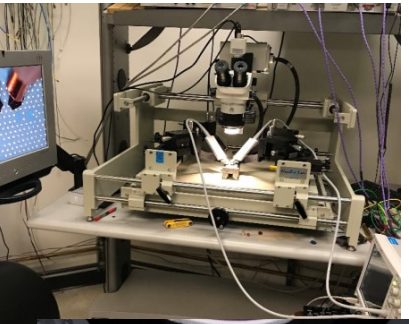


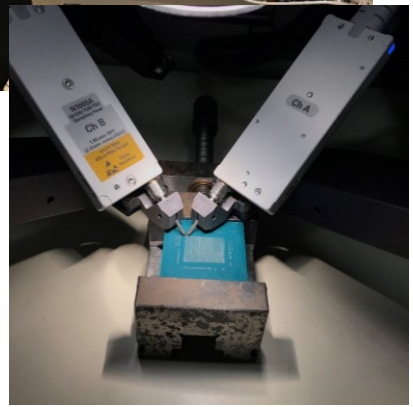
Measurement Bandwidth:
TRD impedance readings are within 1.5Ω for 20ps and 60ps edges - yet details are lost

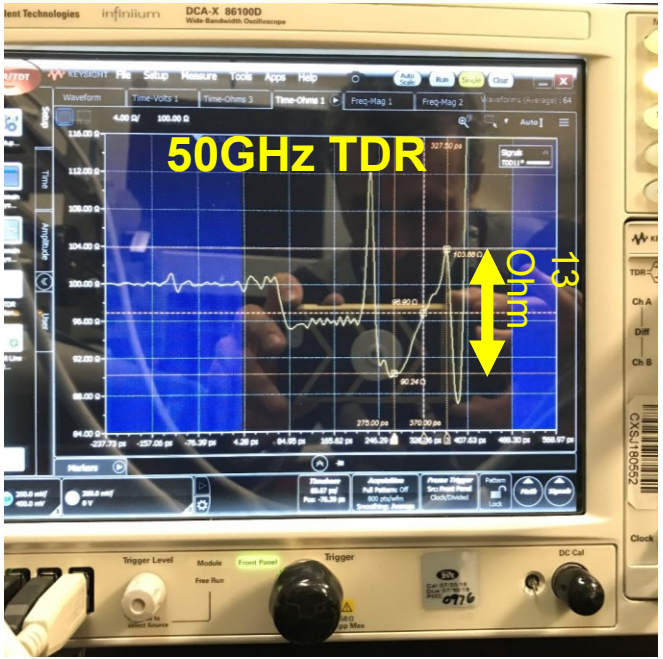


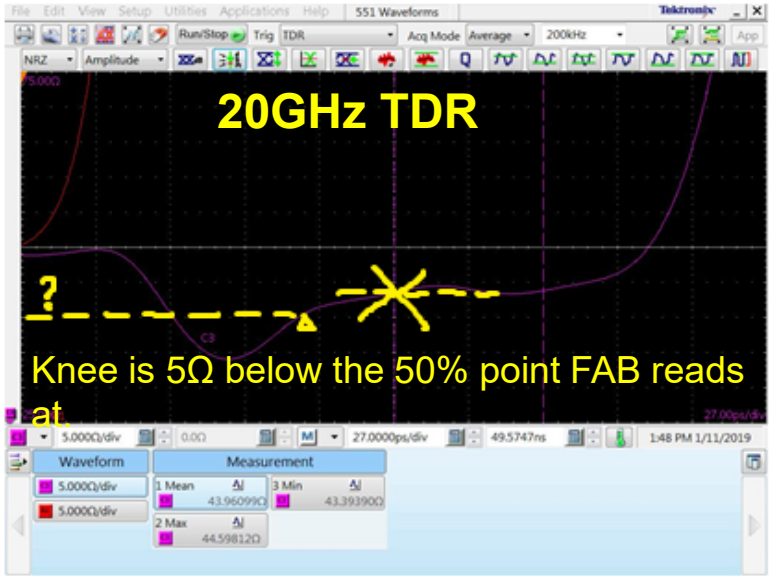


Where to read TDR plot? At the trace's left end… not @50-70% into the trace.







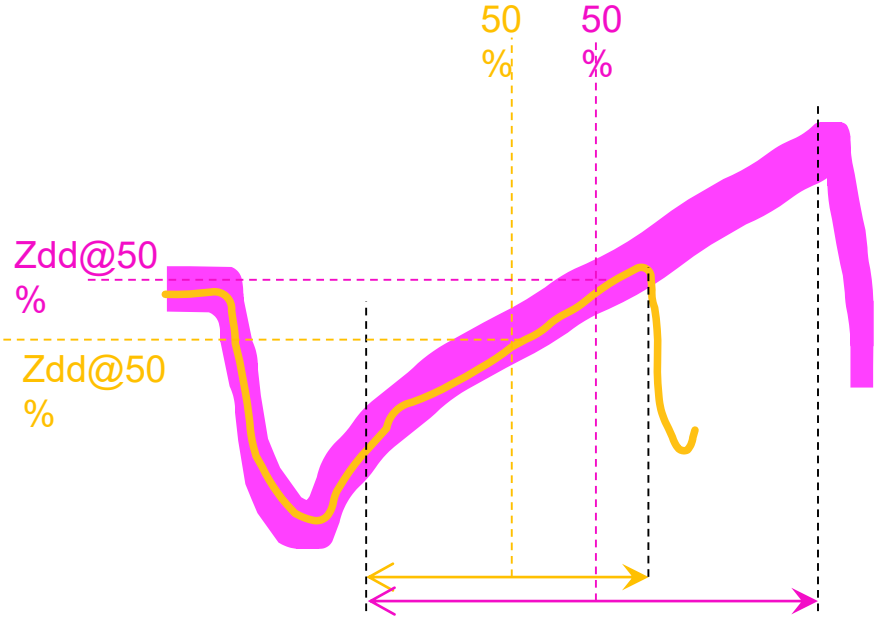


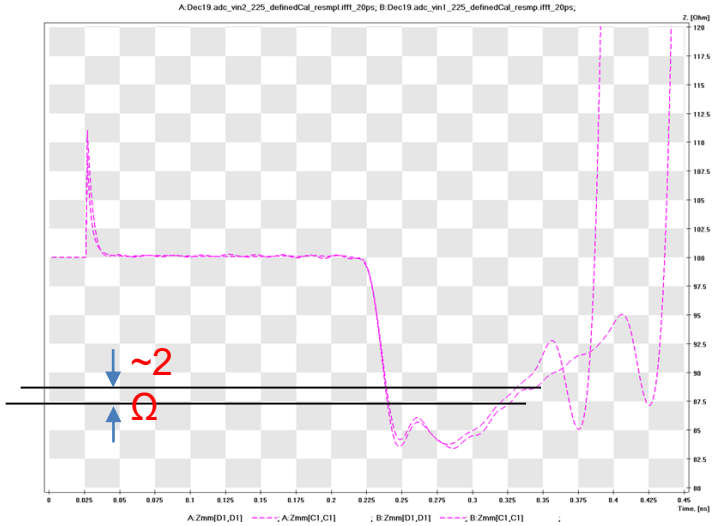
The MAX-MIN delta is >10Ω, => overestimate Zdd by >5Ω

Uncertainty of TDR reading midtrace associated with the trace length

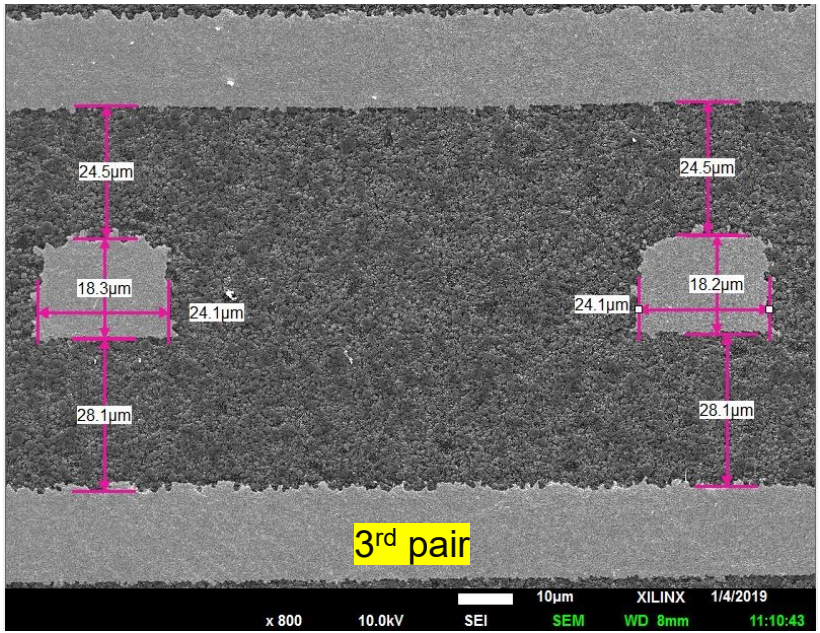
Which 50% point should be selected: in a shorter or longer trace?

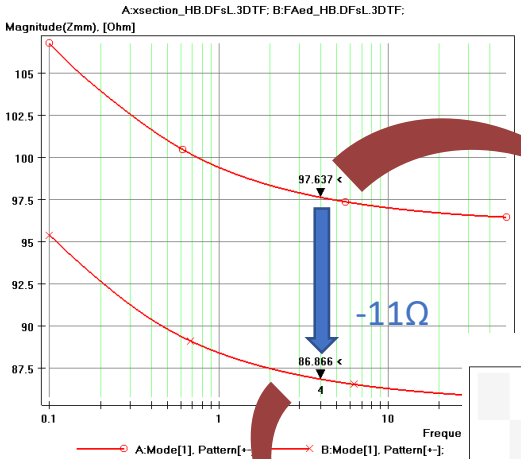
- Reading in midtrace for shorter and longer traces results into two different values, one higher than the other.

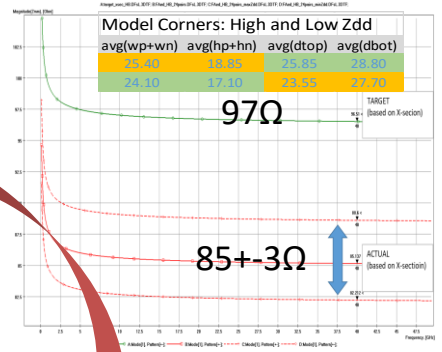


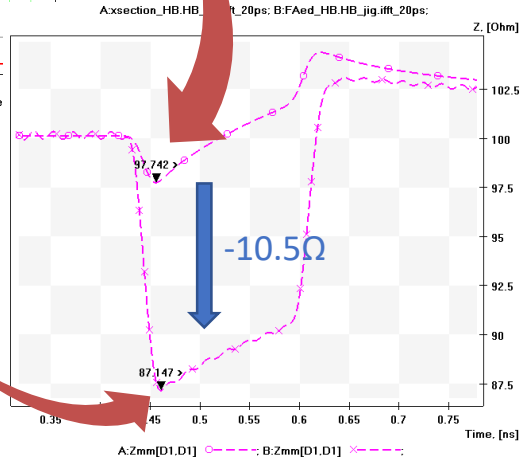


SEM Measurements of a Diff Pair on M3 vs. Model



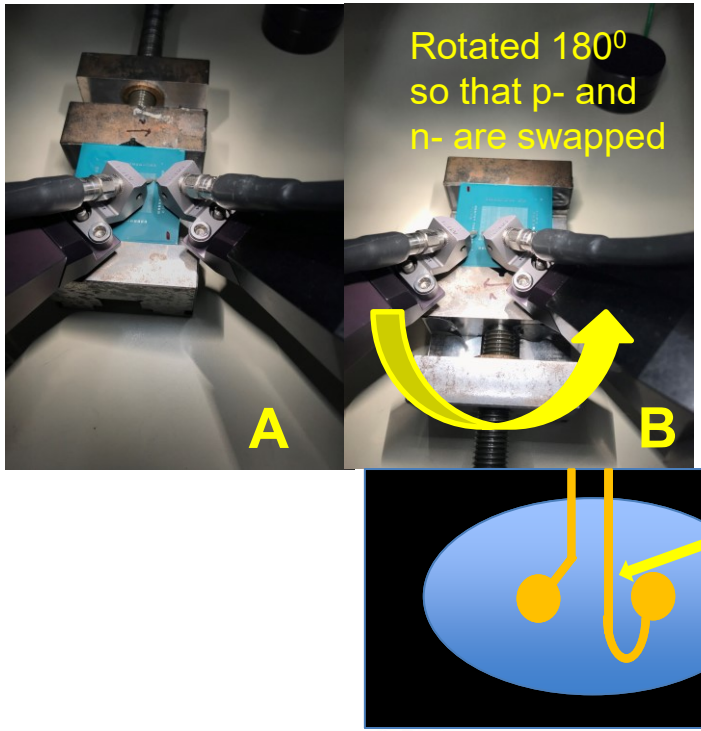




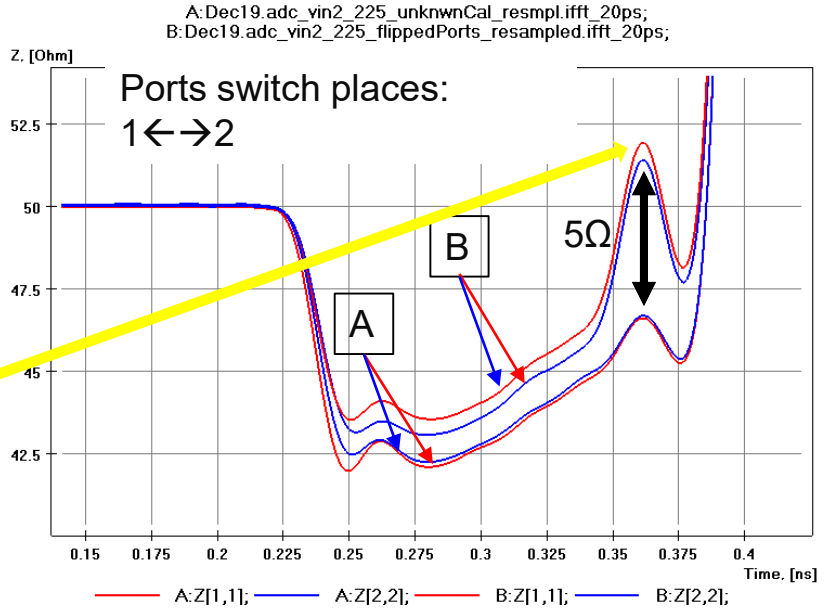


Model adjusted to match FA X-section gives Zdd~86-87Ω
This is very close to measured 83-84Ω (off by only 3Ω)

The inductive blip is caused by the DUT – not by asymmetry of DeEmbedding



Skew-matching U-turn adds a 5Ω inductive blip on TDR.

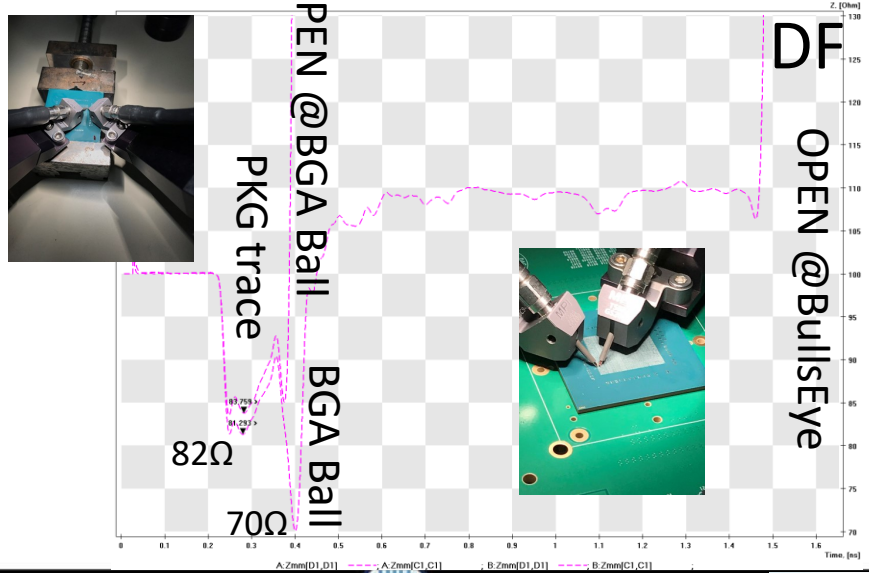


Problems at Fabs

- Lack of TDR Calibration to Probe tips
- Low TDR Bandwidth / Resolution
- Wrong readout point on TDR
- Content with having CDs within their range

Bump-end DD TDR of channel adc_vin2_225: PKG-on-PCB vs. PKG-alone

Mixed-Mode (DF) View

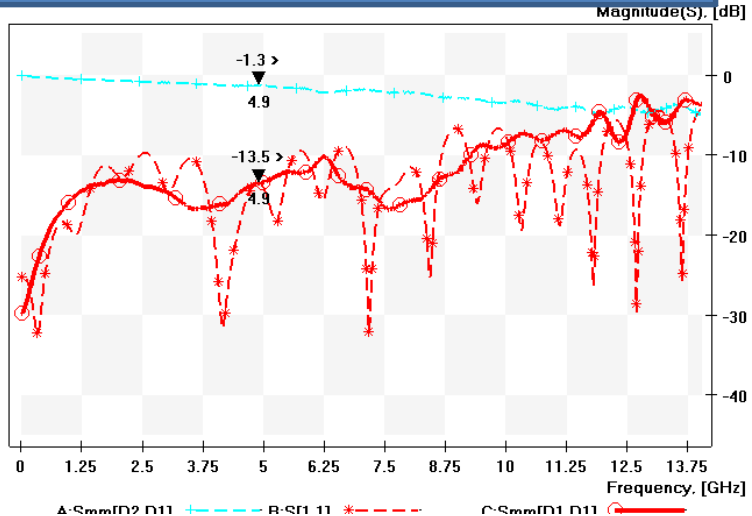


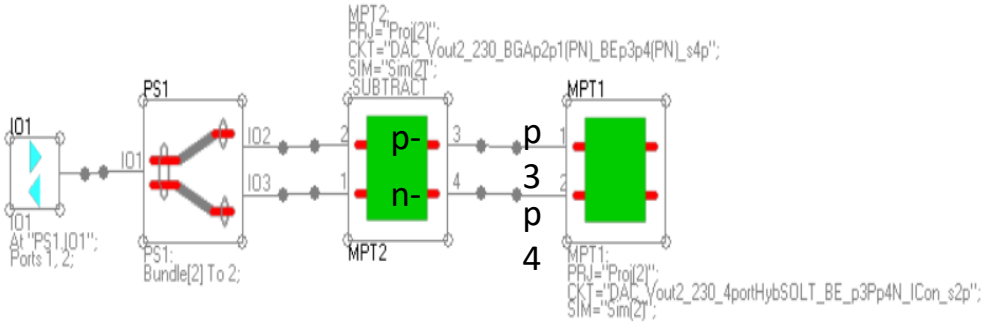
TDR of PKG-on-PCB is consistent with that of PKG-alone.

1. Length match / align between the two.
2. Trace Zdd match within 2.5Ω.
3. @BGA Ball impedance 70Ω of PKG-on-PCB is much lower due to PCB capacitive launch (both are with 20ps edge).

DAC_Vout2_230: DeEmbed vs. Raw

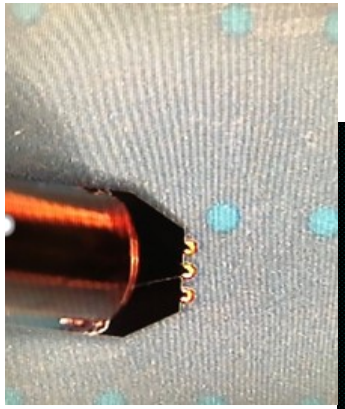
Solid Red Curve is the de-embedded RL
Dash Red Curve is the raw RL

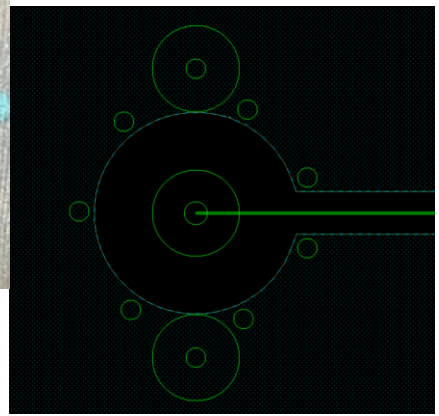


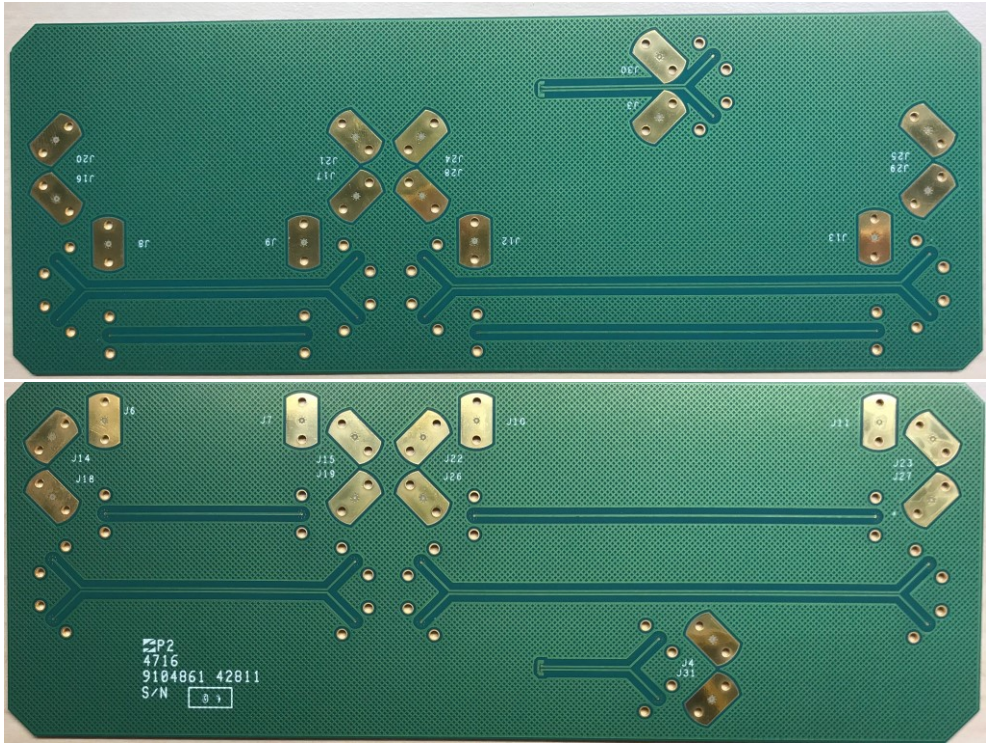


GL102 Material Property Identification with a Test Vehicle

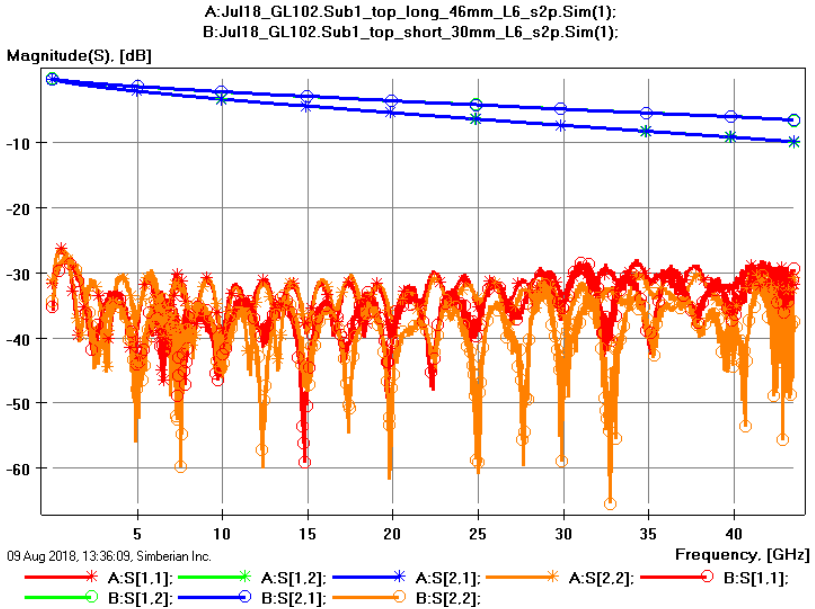
Signal Launch







Raw measurements of 46mm & 30mm striplines on L6

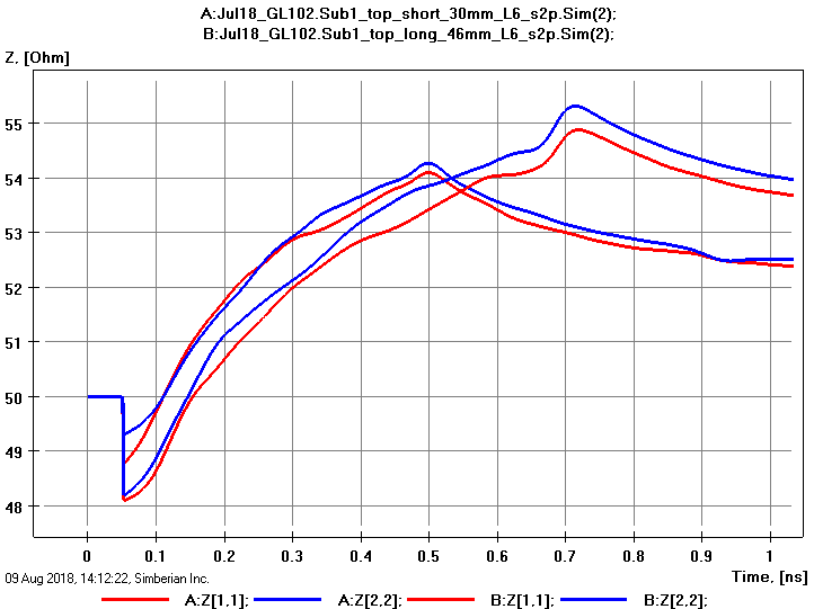


Observations:

Very clean Insertion Loss all the way to 42.5GHz;

Very low Return Loss – implying perfectly designed u-probe launches.

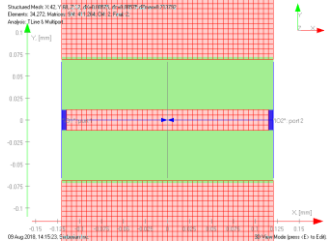
TDR – to verify clean launches

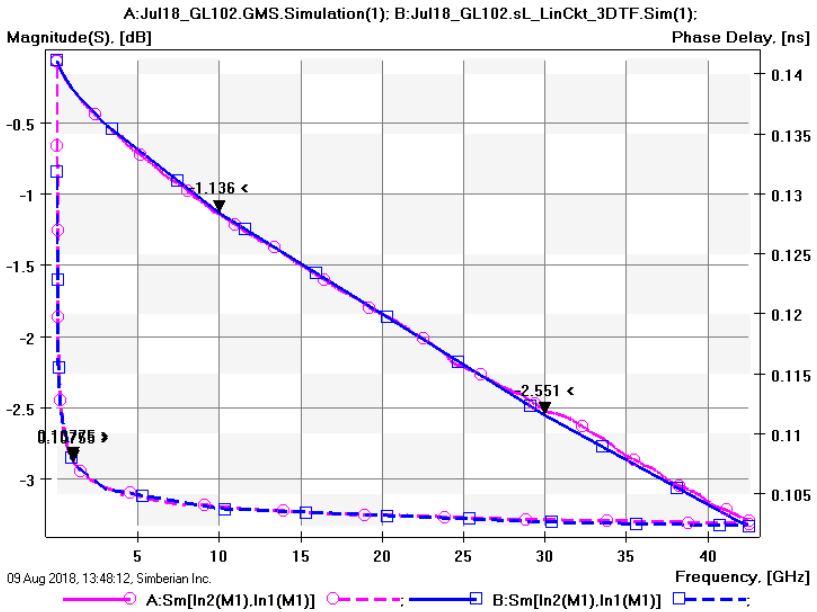


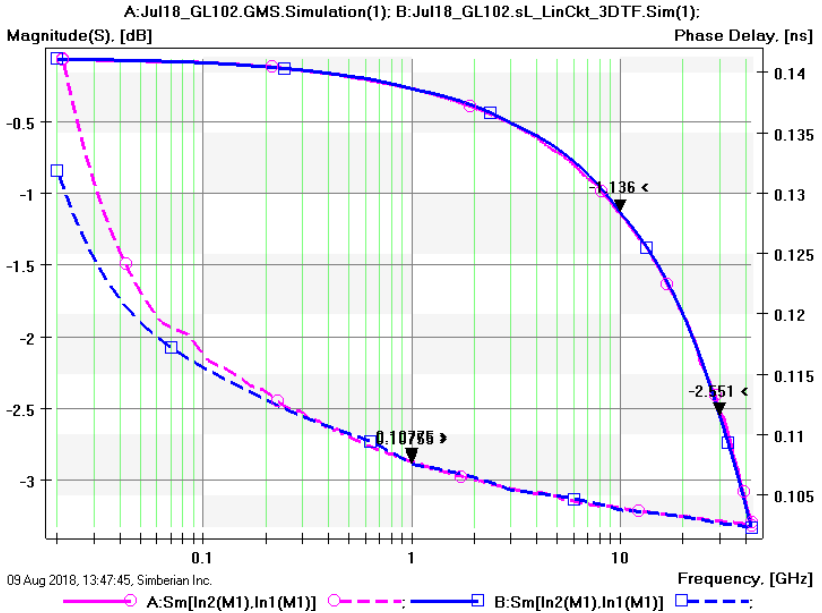
Observations:

Lunches on both long (46mm) and short (30mm) lines are within 1.5Ω of each other and within 2Ω of the 50Ω target.

IL (left axis) & Phase Delay (right axis) model (blue) fit to GMS-de-embedded data (purple) of 16mm line

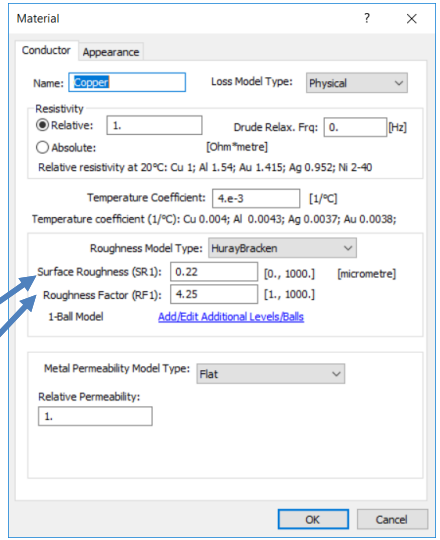






Summary of Findings

	Units	Datasheet	ID'ed NOW
Copper Relative Resistance (RR)	--	1.0	1.0
Dk [4)]	--	3.2	3.45
Df [4)]	--	4.9e-3	4.9e-3
Surface Roughness [3)]	um	Unavailable (0.25-0.3) [1)]	0.22
Roughness Factor [3)]	--	Unavailable	4.25



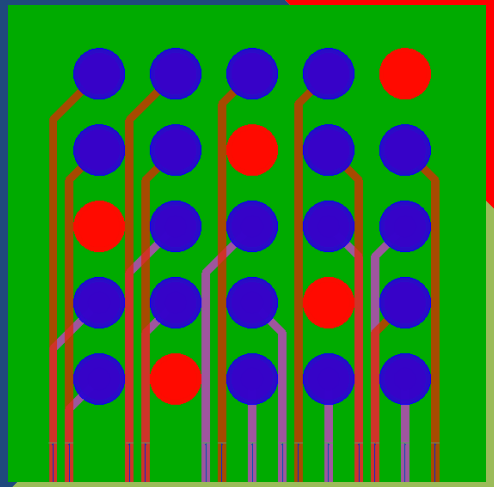
Caveats:

1. Based on info from the vendor: *"For the roughening treatment of the buildup metal layers, vendor cannot disclose the CZ number that they use. They will, however, target the Ra = 0.25 – 0.30µm that you require."*
2. Trace cross section is assumed to be as drawn: 23um x 15um.
3. Surface Roughness Model: Hurray-Bracken
4. At 10GHz, Wideband-Debye model.

Crosstalk in BGA Breakout on PCB:

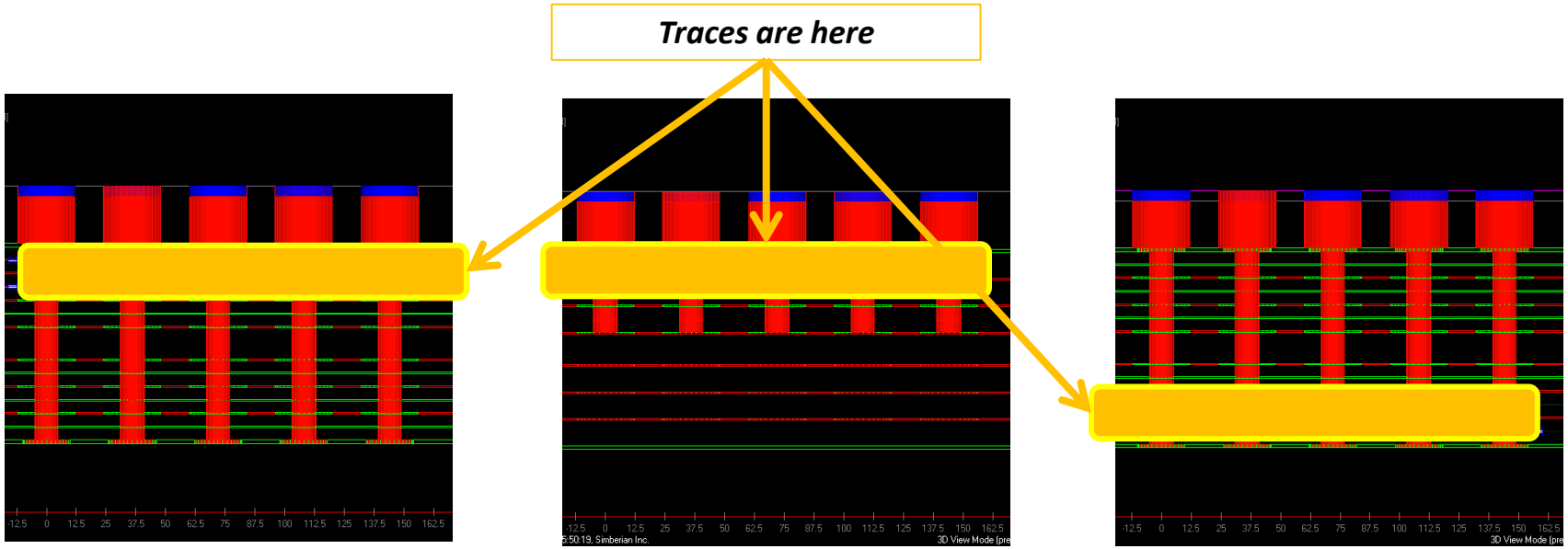
When is necessary to back drill?

How much does it help?

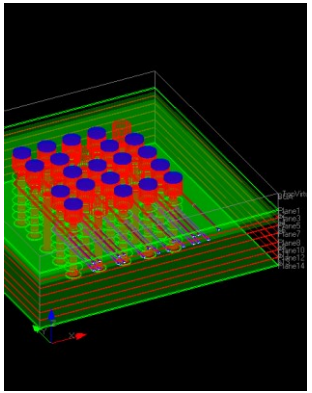


4:1 S/G

The three compared cases



4:1 S/G PSXT by Column within 5x5 via array at BGA edge

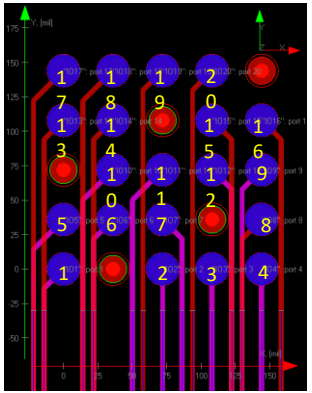


17	18	19	20	GND
13	14	GND	15	16
GND	10	11	12	9
5	6	7	GND	8
1	GND	2	3	4

Legend

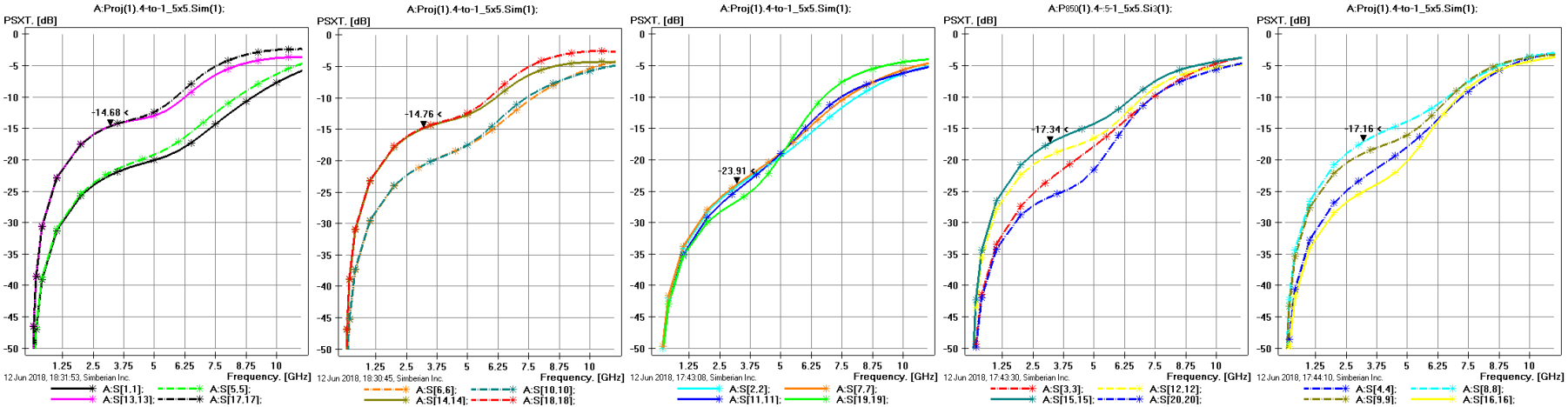
Breakout layer map

s2
s4



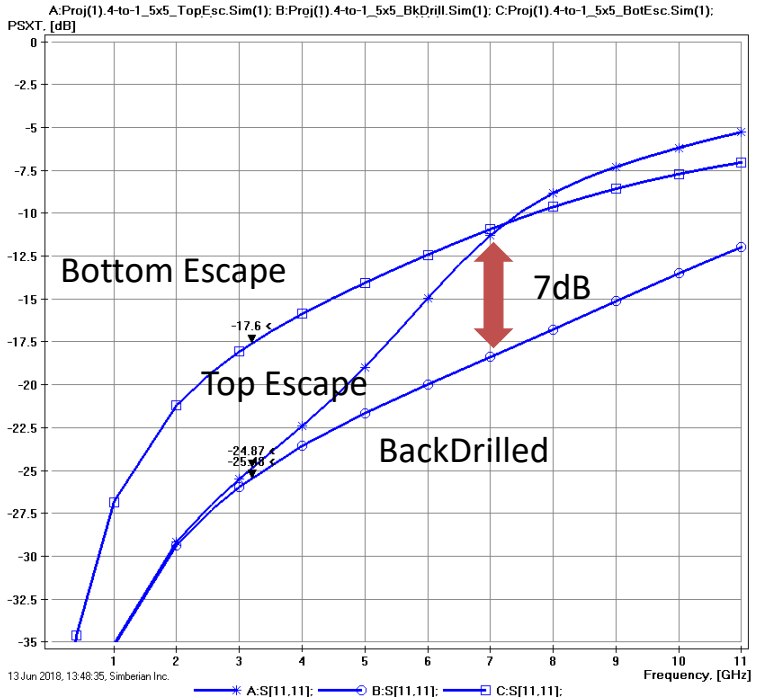
BGA Edge

Port map of trace ends																	
s2	23	24	x	27	28	x	x	30	x	x	33	x	35	36	x	38
s4	22	21	x	25	26	x	29	x	31	32	x	34	39	40	37	x



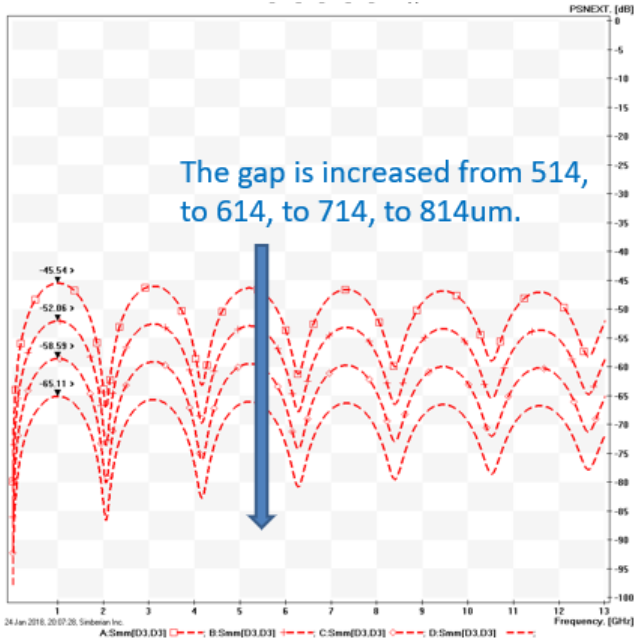
4:1 S/G PSXT: TopEscape vs. BackDrilled vs. BotEscape

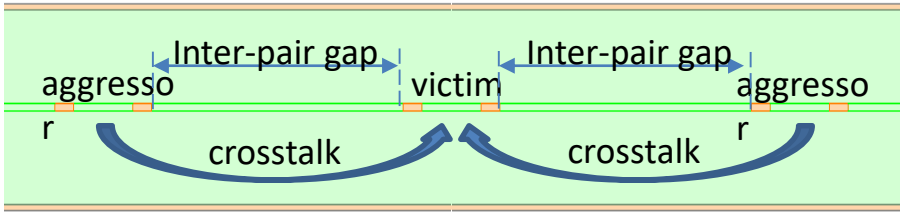
- Bottom Escape: The highest coupling from Inductive loops.
- TopEscape (w/o backdrilling) deteriorates above 3.2GHz and by 7GHz becomes as bad as BotEscape
  - Stubs in BotEscape couple capacitively and contribute to crosstalk progressively more at higher frequencies, above 3.2GHz. By 7GHz, PSXT catches up to Bottom Escape. Thus, the capacitive coupling completely offsets the benefit of escaping on top layers – if without backdrilling. At above 7GHz, backdrilling is by far the best option.



Guard Rail between Differential Pairs: Does it help? How much space does it save?

PSXT vs. inter-pair gap

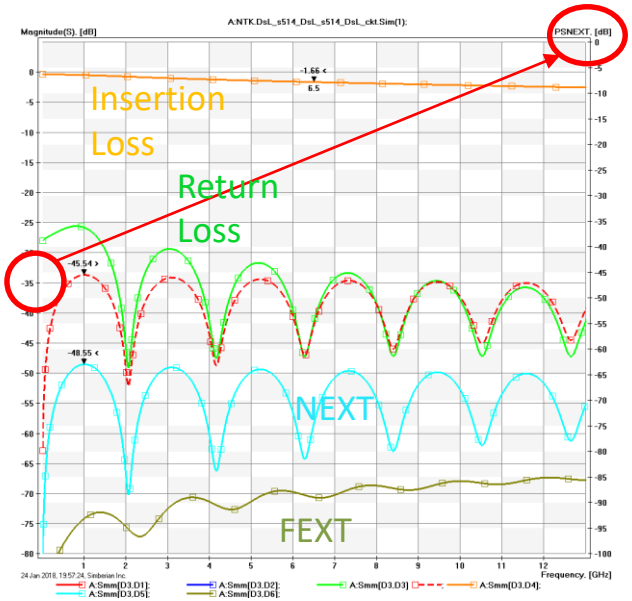




	Inter-pair gap [um]			
	514	614	714	814
Max PSXT [dB]	-45.14	-52.06	-58.59	-65.11

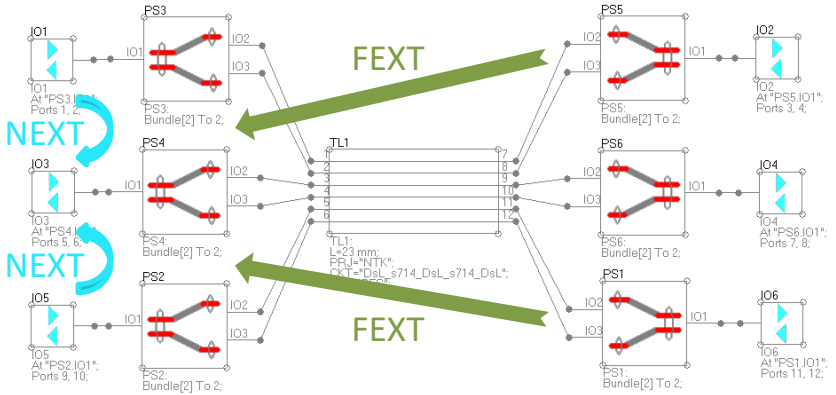
Thus, every additional 100um of inter-pair gap reduces PSXT by about 6.5dB.

Differential IL, RL, NEXT, FEXT and PSXT of only traces – not including vias.



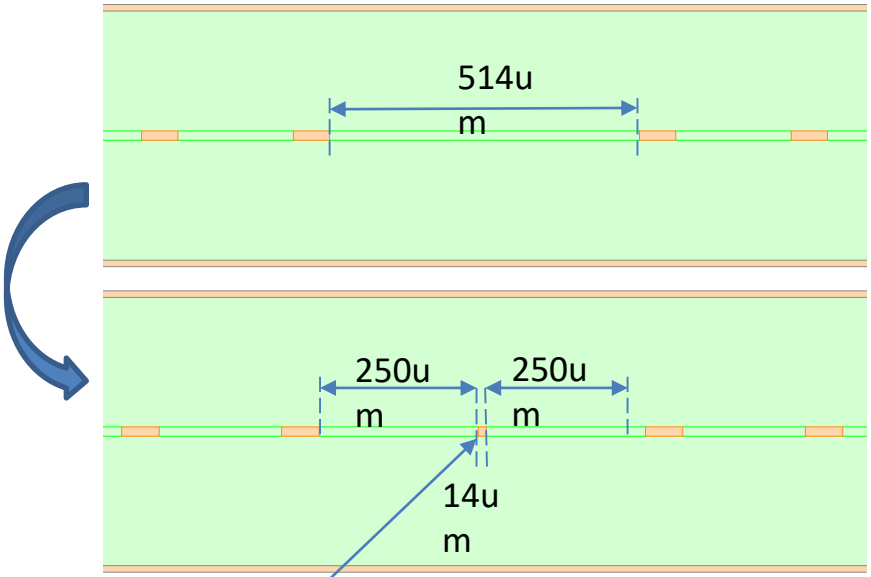
Circuit model with 23mm of extracted 3-pairs

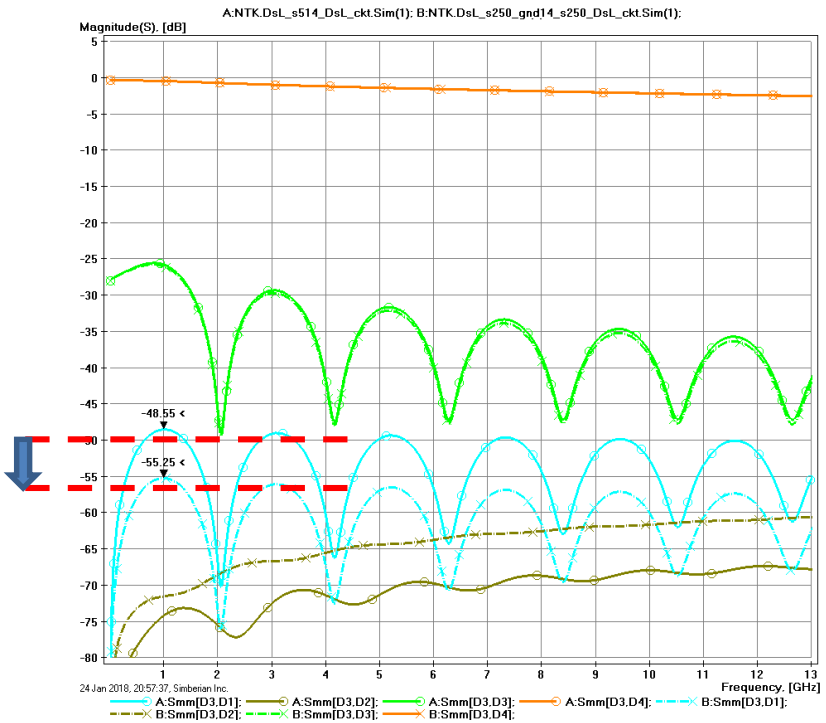
victim



*) PSXT is 3dB higher than NEXT from each of 2 neighbor aggressor traces – as it should be.

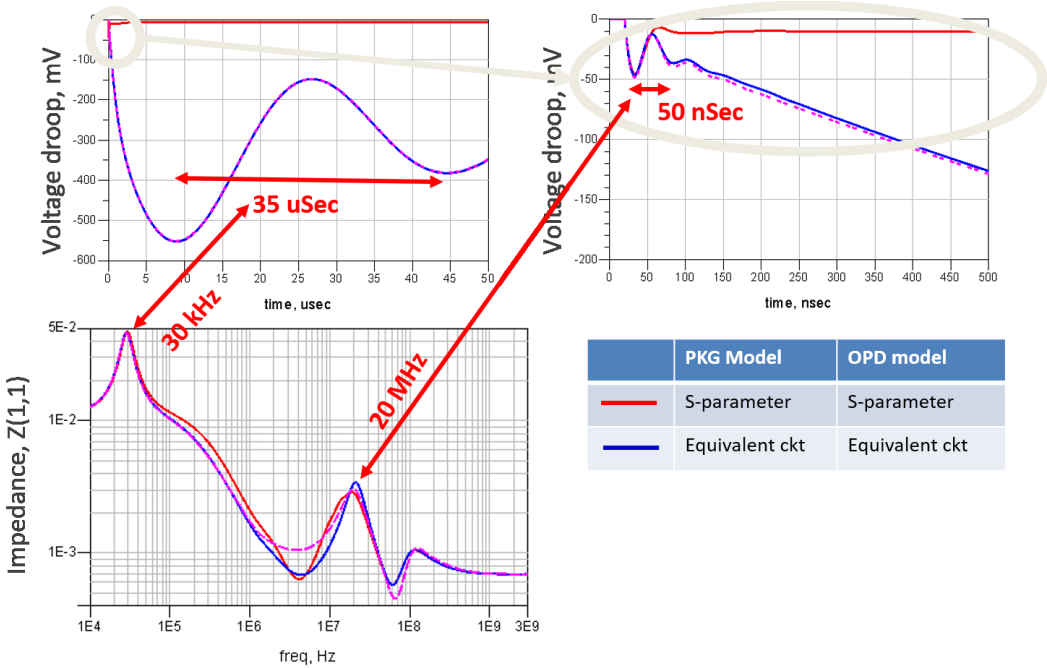
Insertion of (ideal) GND rail between differential pairs reduces Xtalk by about 6.7dB. This is comparable to adding 100um gap.





RCM use for Multi-scale time-domain PDN simulation

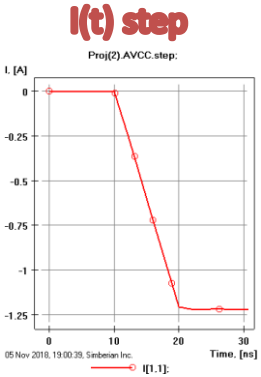
Vccint Voltage droop IS captured accurately but the slow 35uSec oscillation *IS NOT* - when only sNp models are used for both PKG PDN and OPD.

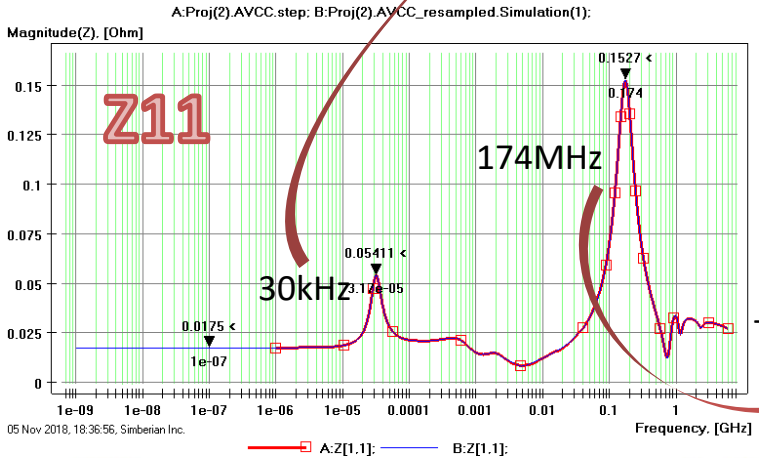


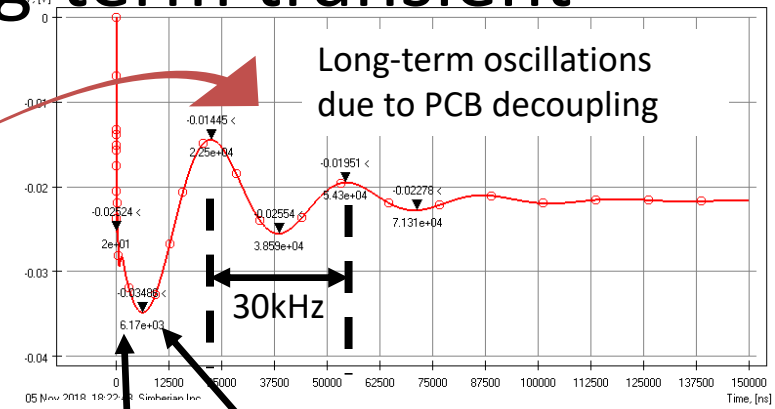
	PKG Model	OPD model
	S-parameter	S-parameter
	Equivalent ckt	Equivalent ckt

VCC first droop and long-term transient

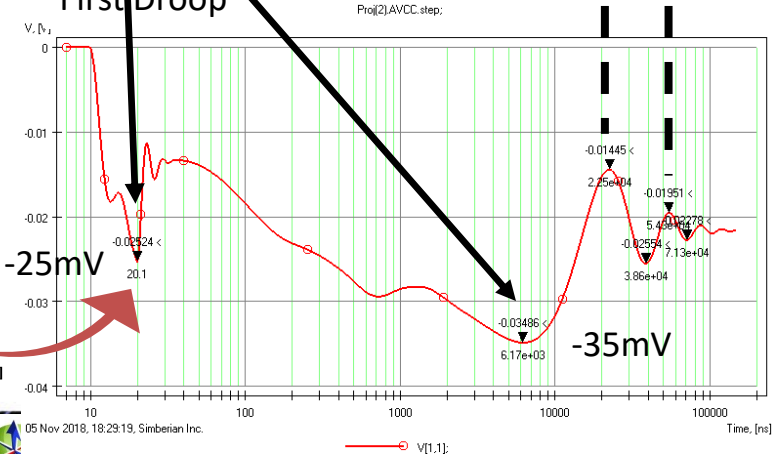
Z11 is fitted with Rational-Compact Model (RCM).
Resampled RCM, shown in blue, matches original Z11. RCM is used to synthesize V(t) with Recursive Convolution.



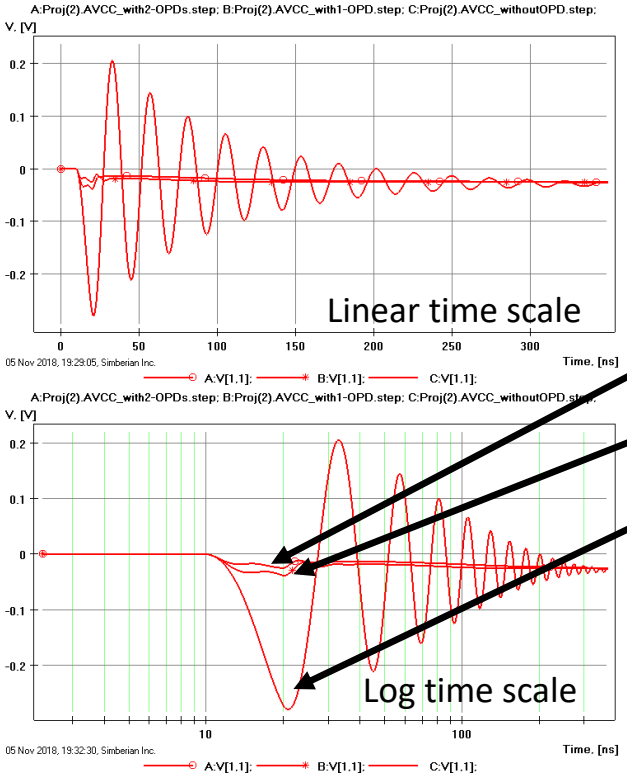




First Droop



Efficiency of OPD caps on VCC power rail



Number of OPD caps	First Droop [mV]
With 2 OPD caps	-25
With 1 OPD cap	-39
Without OPD	-280

In Search of Fundamental Limits on PCB Interconnects

Equations and solutions

Accuracy

Predictability

What are the limits on electrical signal data rates?

212-Gb/s 2:1 multiplexing selector realized in InP DHBT Electronic Letters, Dec. 2018, Nokia Bell Labs

A. Konczykowska, F. Jorge, M. Riet, V. Nodjiadjim, B. Duval, H. Mardoyan, J. M. Estaran, A. Adamiecki, G. Raybon, J.-Y. Dupuy

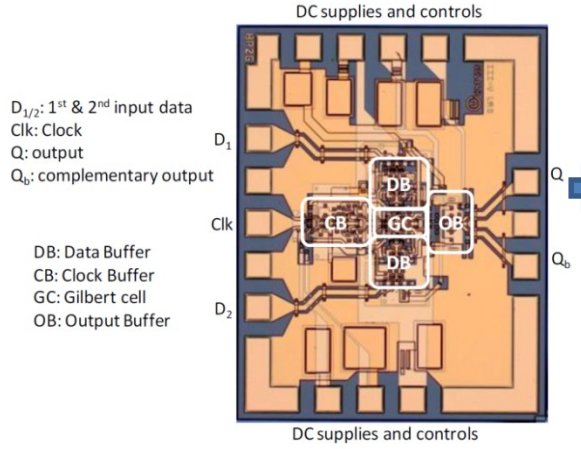


Fig. 1 *SEL chip microphotograph.*

At what distance we can transmit such signals?

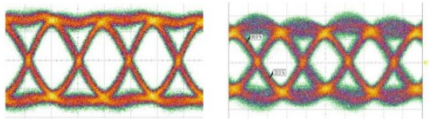


Fig. 3 *Measured 106-Gb/s input (a) and 212-Gb/s output (b) signals. (a) 100mV/div, 5ps/div, (b) 100mV/div, 2ps/div*

Hint: It is defined by interconnects…

P. J. Pupalaikis, Xi Chen, S. Chandrasekhar, S. Randel, G. Raybon, A. Adamiecki, P. Winzer, The Fastest PAM-4 Signal Ever Generated, DesignCon 2017 (Teledyne LeCroy + Nokia Bell Labs)

190 Gbps NRZ and 390 Gbps PAM4 signals generated, transmitted through 6 inch of coaxial cable(?) and measured

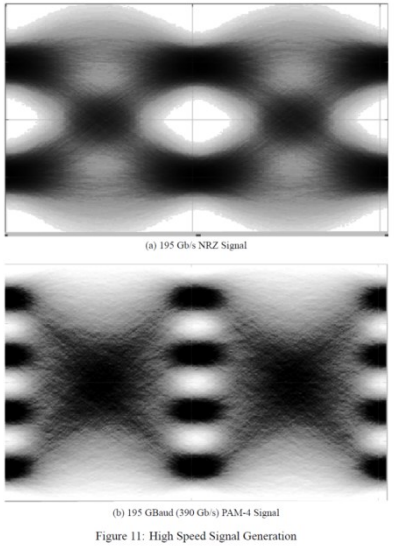


Figure 11: High Speed Signal Generation

Waveguiding technologies

Microwaves – THz - Optics

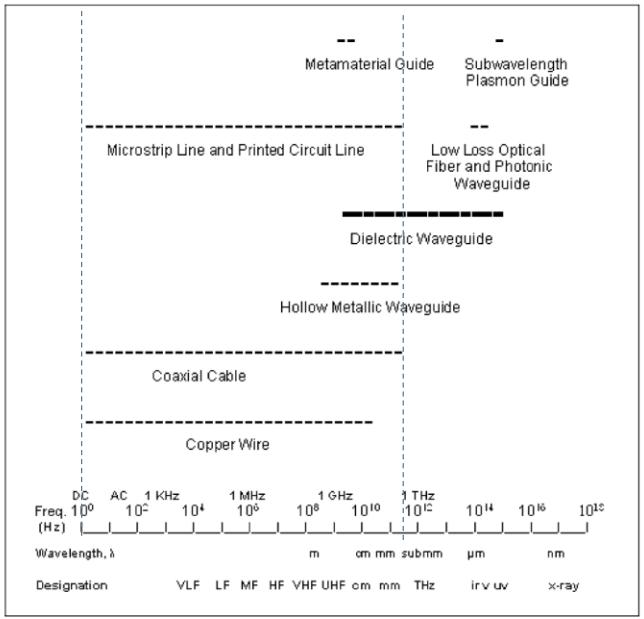


Figure 1.1. Spectral regions for various waveguides

C. Yeh, F. I. Shimabukuro, The Essence of Dielectric Waveguides, Springer, 2009

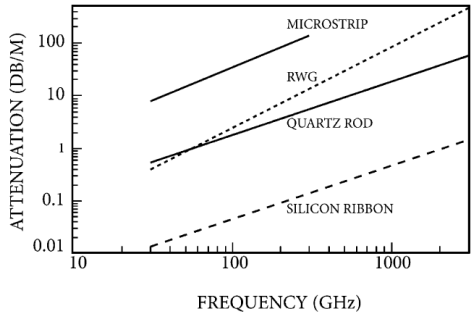
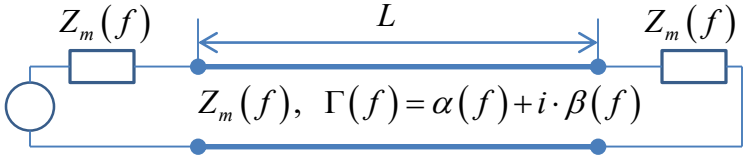


Figure 11.7. Typical performance comparison between several conventional waveguide structures and the high dielectric constant (Si) ribbon waveguide for the frequency range from 30 GHz to 3 THz. Note that the waveguide losses of typical conventional waveguides can be as much as 100 times larger than those of the ribbon waveguide in this spectrum [15]

Maxwell's equations and transmission line theory is applicable to all those waveguides up to x-ray frequencies!

Fundamental limits on TEM interconnects

T-line limits are defined by
GMS-parameters: S11=0, S21 != 0



1) Attenuation

2) Dispersion

$$\tau_G = \frac{\partial\beta}{\partial\omega}$$

Signal: $$V_{out} = V_{in}\cdot e^{-\left[\alpha(f)+i\cdot\beta(f)\right]\cdot L}$$

3) Single-mode propagation

~~$$V_{out} = \sum_{k=1}^{Nm} V_k e^{-\Gamma_k\cdot L}$$~~

$$\alpha(f) \approx \frac{R(f)}{2Z_0} + \frac{G(f)\cdot Z_0}{2}$$

conductor

$$\alpha_C \approx \frac{K_R(f)\cdot R_S(f)}{\sqrt{\mu/\varepsilon}\cdot d}$$

$$R_S = \sqrt{\pi f\cdot\mu\cdot\rho}$$

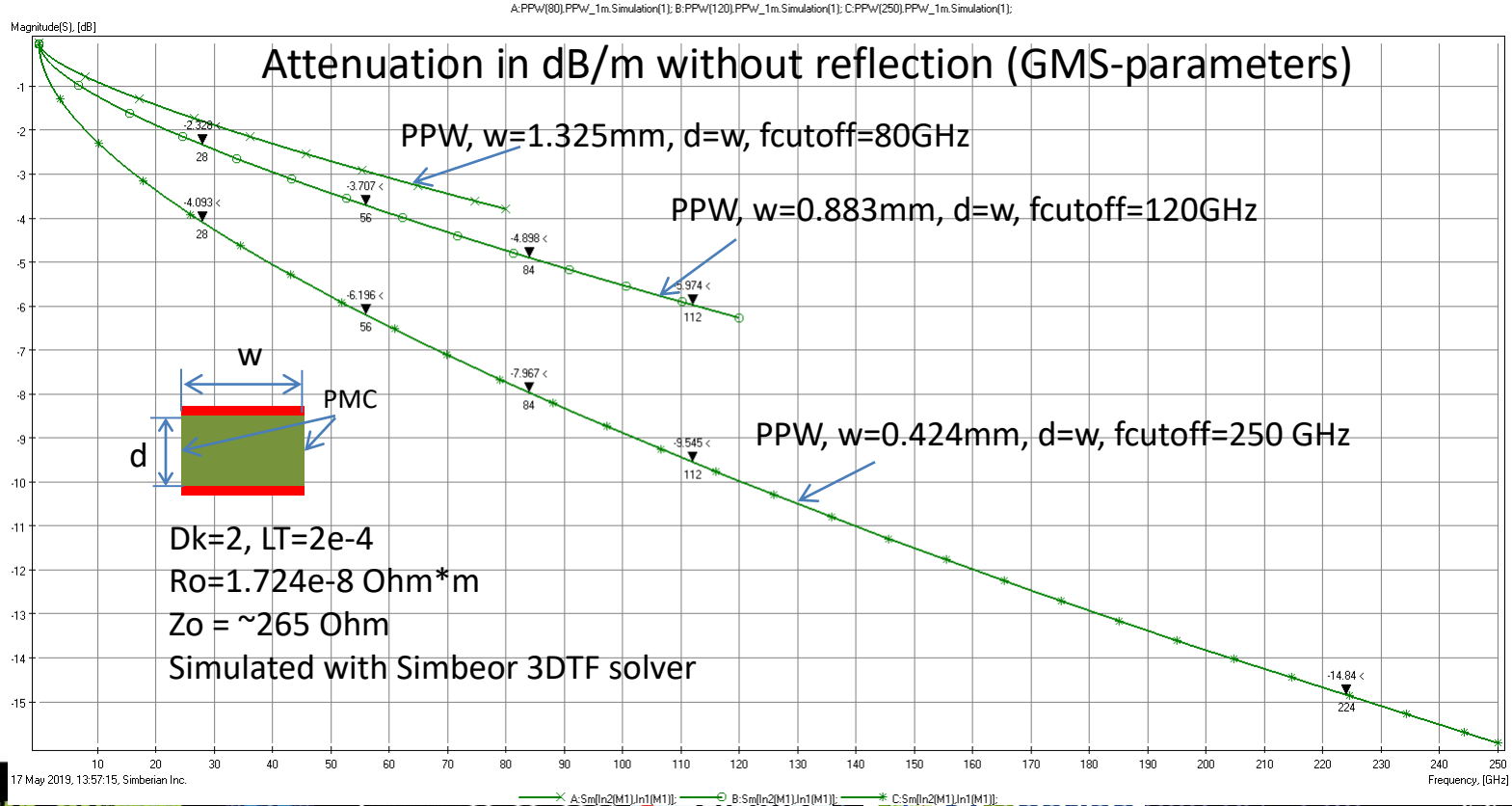
for PPW

dielectric

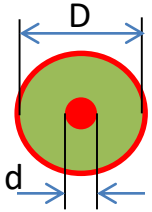
$$\alpha_D \approx \pi f\cdot\tan\delta\cdot\sqrt{\varepsilon\mu}$$

The limits on quasi-TEM mode

Example of fundamental limits on attenuation in single mode parallel-plate waveguide (PPW)



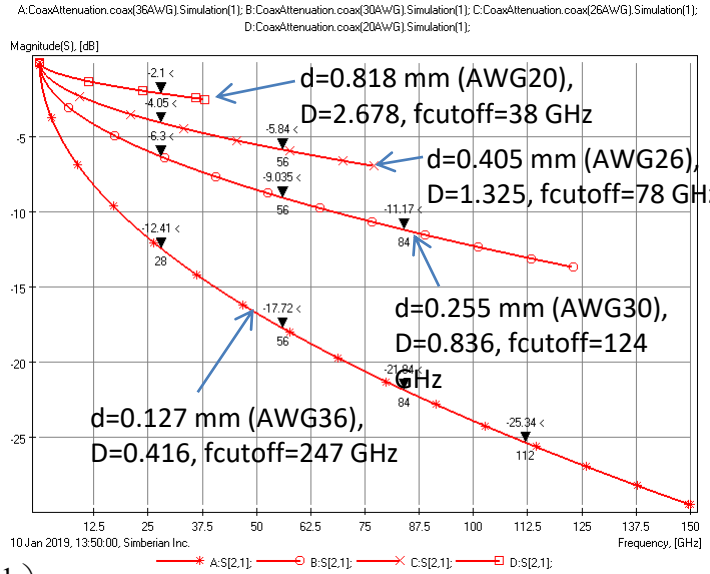
Coaxial waveguide (ancestor of planar interconnects)



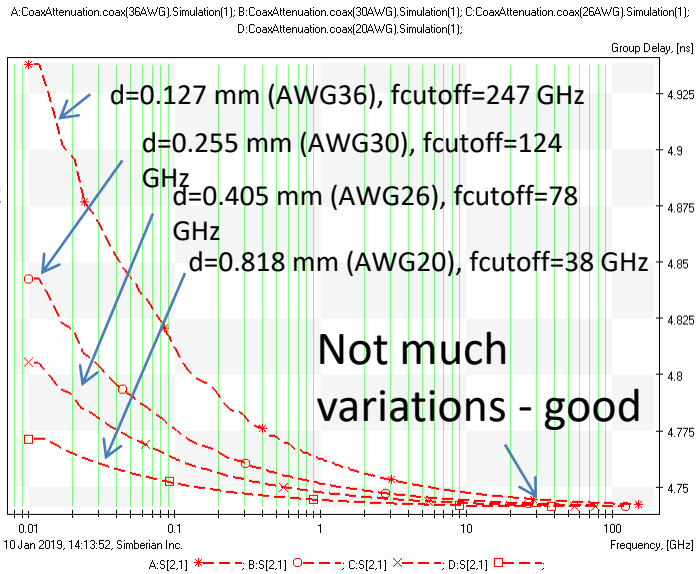
Dk=2, LT=2e-4
Ro=1.724e-8 Ohm*m
Zo=50 Ohm
Single-mode limit is defined by mode TE11:

$$f_{cutoff} \approx \frac{2c}{\pi(d+D)\sqrt{\varepsilon}}$$

1 m segment: Attenuation



Dispersion

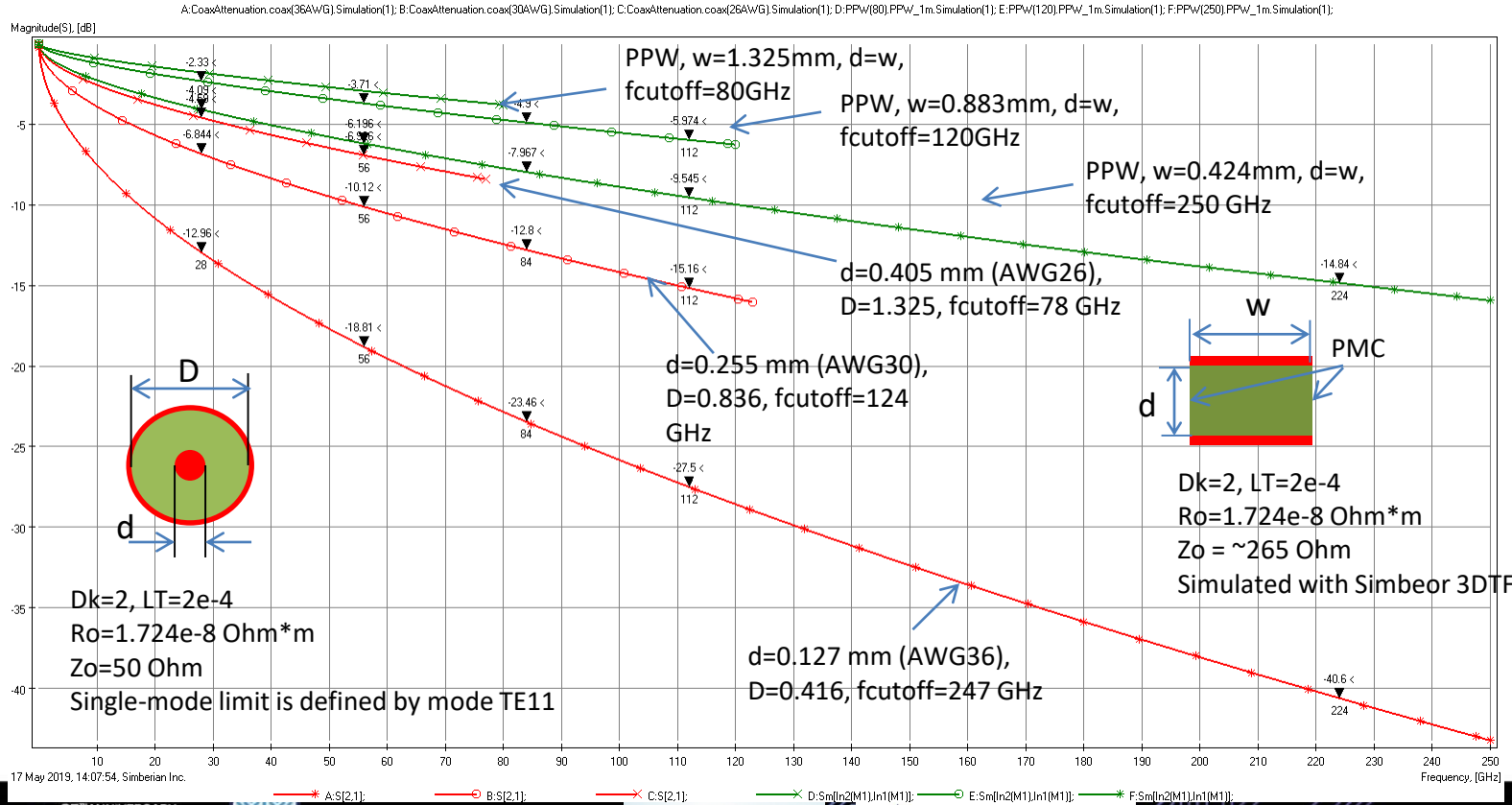


$$\alpha_C \approx \frac{K_R(f)\cdot R_s}{\sqrt{\mu/\varepsilon}\cdot\ln(D/d)}\cdot\left(\frac{1}{d}+\frac{1}{D}\right)$$

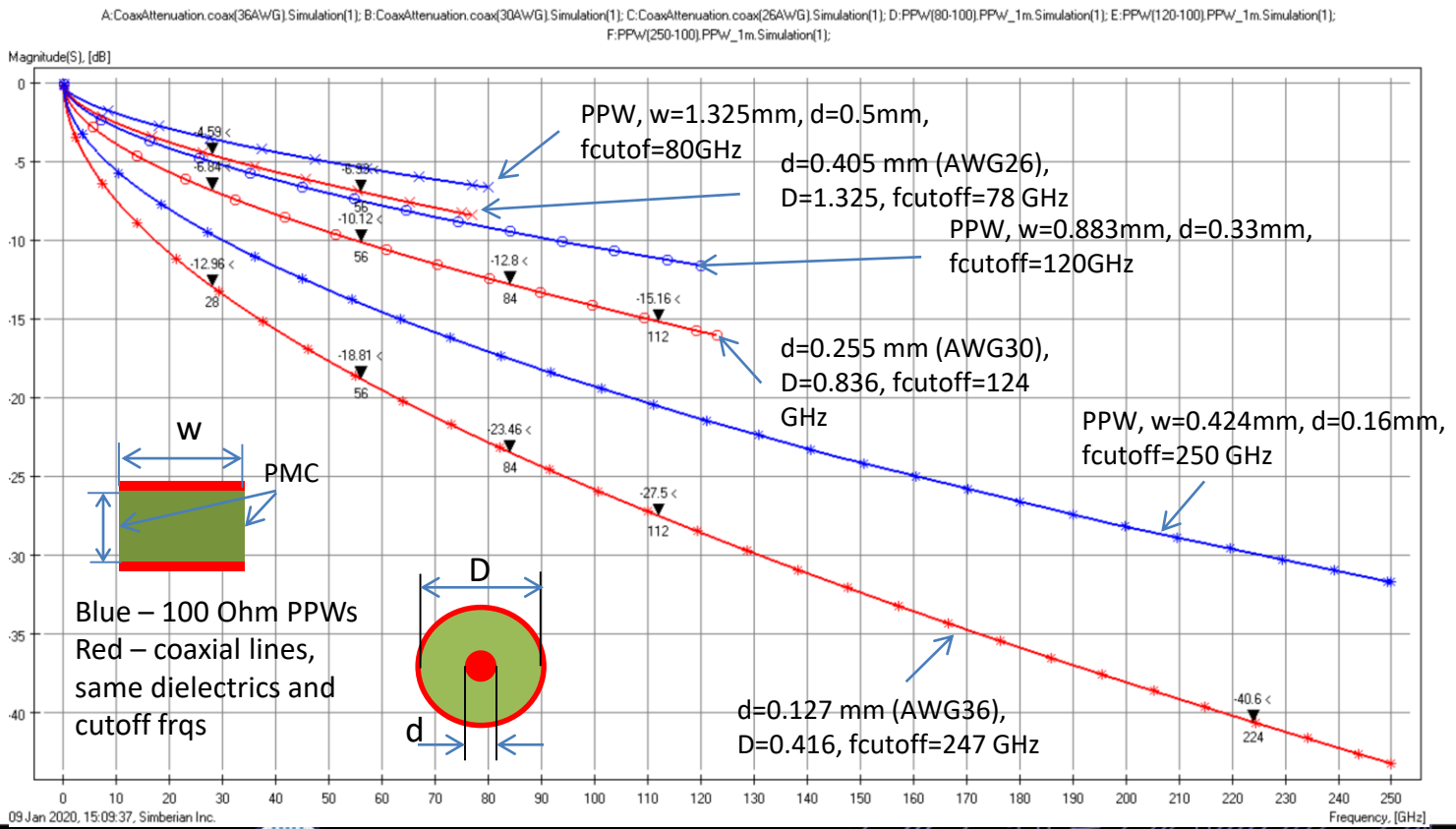
$$\alpha_D \approx \pi f\cdot\tan\delta\cdot\sqrt{\varepsilon\mu}$$

Mostly conductor losses – almost as good as it gets for waveguides with DC
The upper frequency is limited by cutoff of the first high-order mode
Though, integration is poor - requires connectors (not scalable, reliability, cost)…

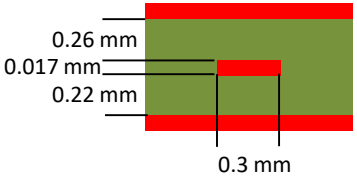
PPW vs. Coaxial: Att. in dB/m



PPW vs. Coaxial: Att. in dB/m



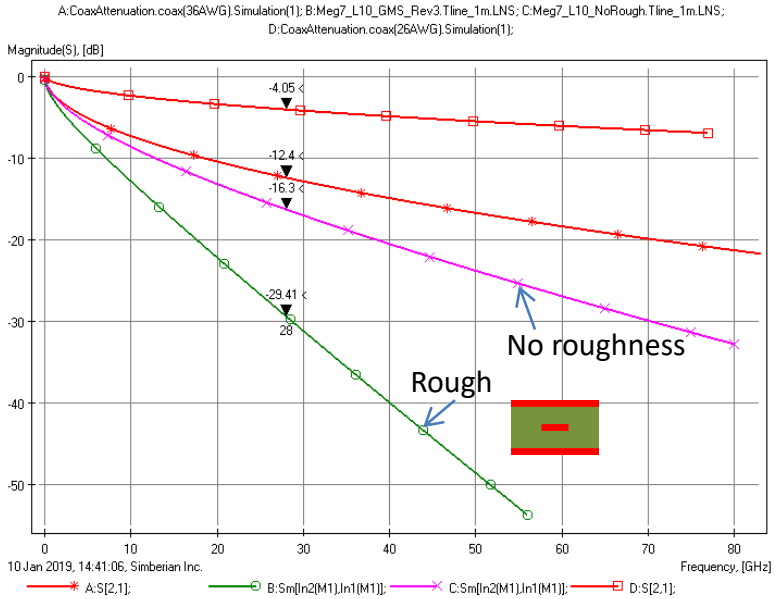
How it compares to PCB traces



Dielectric Wideband Debye:Dk=3.17, LT=0.001 @ 1 GHz
Copper RR=1.43, Huray-Bracken SR=0.14 um, RF=8.5

Material models are identified with GMS-parameters in *A. Manukovsky, Y. Shlepnev, Effect of PCB Fabrication Variations on Interconnect Loss, Delay, Impedance & Identified Material Models for 56-Gbps Interconnect Designs, DesignCon 2019 (Ballroom G, 10:00 - 10:45 AM, January 30th, 2019)*

Attenuation in 1 m segments



AWG26
d=0.405mm

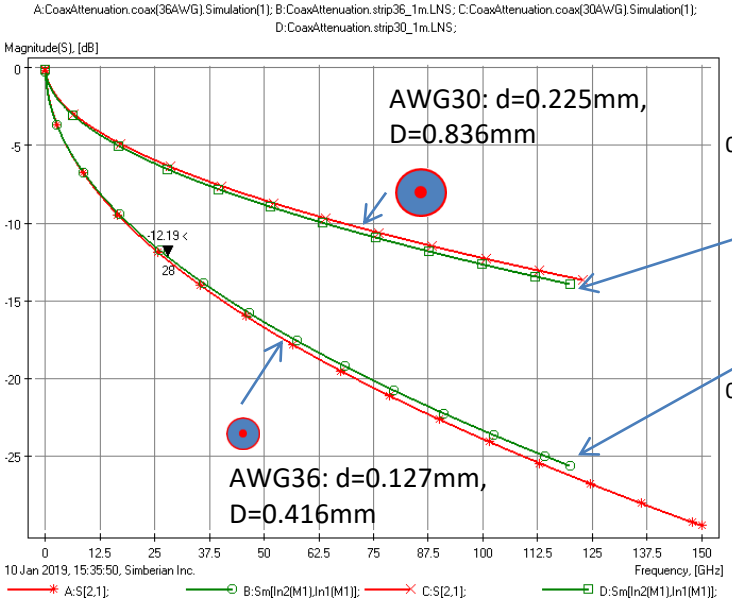
AWG36
d=0.127mm

The losses are too high

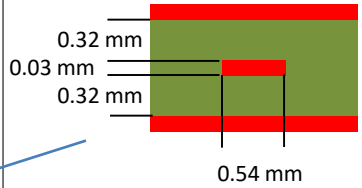
And the conductor losses is clearly the problem…

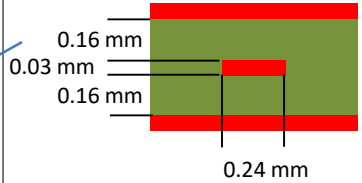
What if we use coaxial cable dielectric and more metal for strips?

1 m segment: Attenuation (GMS)



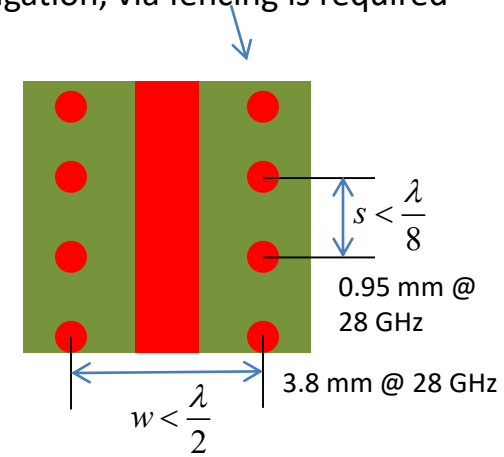
Dk=2, LT=5e-5
Res=1.724e-8 Ohm*m
Zo=50 Ohm





What is the catch?

No single-mode propagation – strip line and parallel-plate modes coexist
To enforce the single mode propagation, via fencing is required



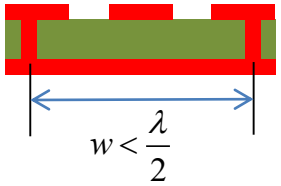
E. Holzman, Essentials of RF and Microwave Grounding

Evolution of microstrip

MSL

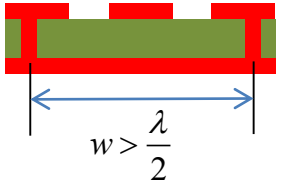
Losses are lower comparing to strip lines with the same dielectric (more metal) - good
High-frequency dispersion - acceptable
Poor field localization – increases coupling noise – not so good
No single mode propagation (TM0 surface wave has zero cutoff frequency) and no way to suppress coupling

CBCPW



Losses are lower comparing to strip and microtrip lines with the same dielectric (even more metal)
For the single mode propagation, parallel-plate waveguide modes must be suppressed with stitching vias close enough to suppress TE10

MSTL



Lowest possible losses over the wider band – quasi-TEM mode merges with TE01 of substrate integrated waveguide (SIW)
Theory is in development

F. Fesharaki , T. Djerafi, M. Chaker, Ke Wu, Mode-Selective Transmission Line for Chip-to-Chip Terabit-per-Second Data Transmission, IEEE Trans. On CPMT, VOL. 8, NO. 7, JULY 2018, p 1272-1280

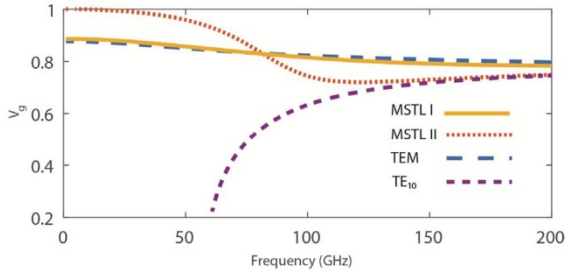
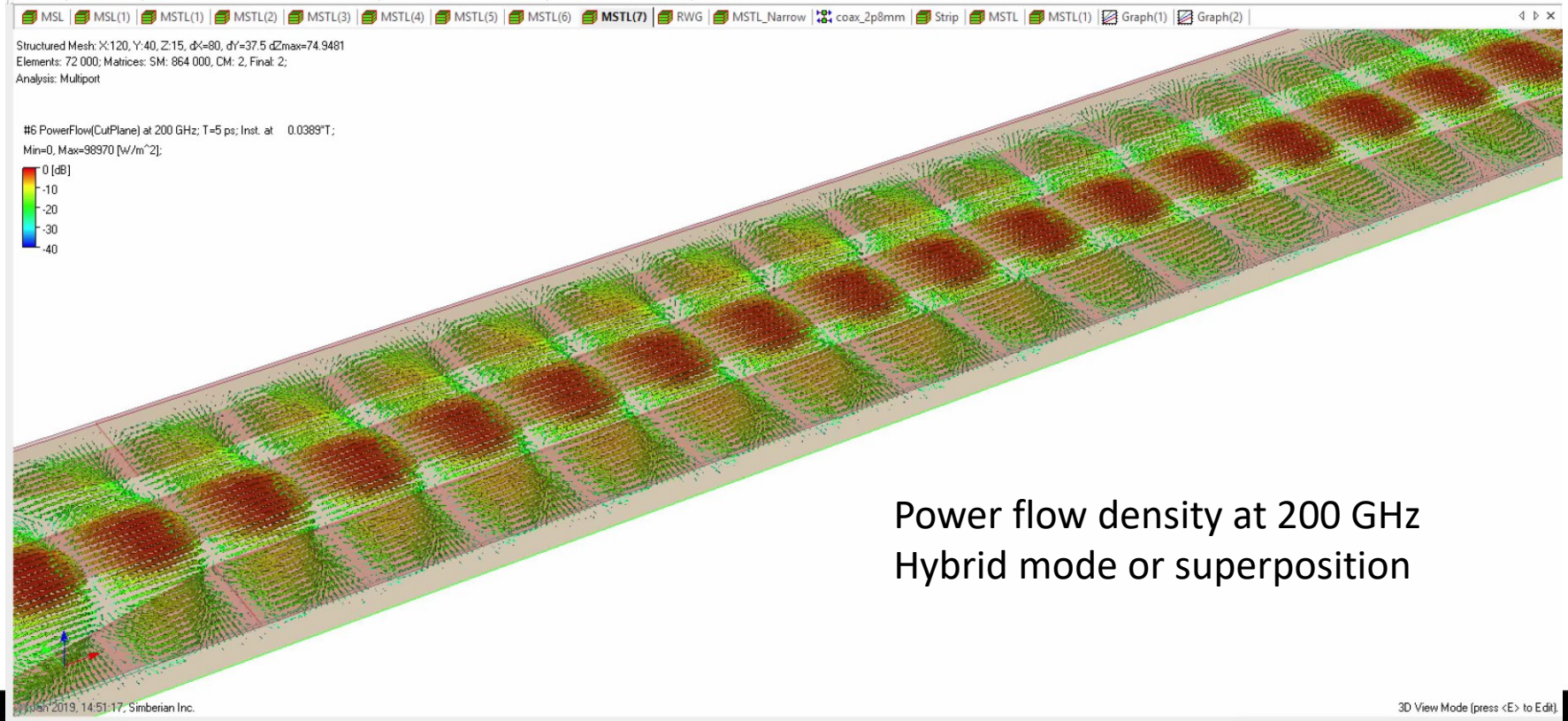


Fig. 4. Group velocity of MSTL on on Rogers RT/duroid 6002 laminates (MSTL I: $h = 127\ \mu$m, $d = 20h$, $s = 1.6h$, $w = 2.4h$, MSTL II: $h = 127\ \mu$m, $d = 20h$, $s = 0.5h$, and $w = 2.4h$) and comparison with group velocity of microstrip line TEM mode and rectangular waveguide TE_{10} mode.

Mode Selective T-Line



Power flow density at 200 GHz
Hybrid mode or superposition

Conclusion

- Design of predictable PCB/packaging interconnects operating at 6-112 Gbps is progressively challenging
  - Predictability up to about 30 Gbps NRZ or 60 Gbps PAM4 is possible with existing technologies
  - Predictability with higher data rates can be done statistically and will require advances in EDA and PCB technologies
- Predictability of interconnects over microwave and millimeter-wave frequency bandwidth is emerging domain of ***electromagnetic signal integrity***…
  - Requires understanding of signal degradation effects from models or measurements (S-parameters, TDR, SBR,…)
  - Requires understanding of what is accounted for in signal integrity software – only validation can help…
- Design processes and practices adopted at lower data rates and without software validation may lead to frustrating failures and costly re-spins…

Thank you!

QUESTIONS?