Systematic approach to PCB interconnects analysis to measurement validation

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***Abstract*— Frequency content of digital signals in PCB interconnects have increased up to 40-50 GHz in recent years. To make sure that interconnects work as expected over this bandwidth, we have to build validation boards and do the analysis to measurement correlation. This paper introduces formal systematic approach to PCB interconnects analysis to measurement validation. We go through selection of test structures, connectors and measurement equipment, demonstrate uncertainties of the analysis based on the initial pre-manufacturing assumptions and how close to reality we get with more formal approach based on the material models and manufacturer adjustments identification.**

I. Introduction

What does it take to design PCB interconnects with good analysis to measurement correlation up to 40-50 GHz? Is it doable with typical low-cost PCB materials and fabrication process, typical trace width, via back-drilling and shortage of space to place the stitching vias? Your EDA vendor shows excellent correlation of the analysis tools to measurements even up to 50 GHz, your PCB fabricator ensures that the board will be built as designed and provides all possible information on stackup and materials. Measurements with the easy-to-use TDNA or VNA should be also a "piece of cake". There is nothing to worry about and the designed interconnects should behave as expected. Unfortunately, many SI engineers already learned that this is not the case and the reality can be far from our expectations. To verify practically everything that goes into the design to manufacturing flow at this frequency bandwidth, we are actually forced to build validation boards. Moreover, re-validation has to be done every time when new PCB material or even new batch of materials or new PCB fabricator is used. The outcome of such validation should be a formal process, and following such a process we reduce the gap between the expectations and reality and are able to reliably predict the behavior of the interconnects on production boards over this bandwidth. That is the main goal of this paper. We do not just show the final analysis to measurement correlation on a case by case basis, as it is usually done in some validation projects, but report a formal procedure based on the material model and manufacturing adjustments identification. The accuracy of the analysis based on the pre-manufacturing assumptions is analyzed and reported.

II. Systematic Validation Process

One of the key elements of design success is the systematic benchmarking of manufacturing, measurements, and modelling. Systematic means analysis-to-measurement correlation observed not just for one or two structures (test coupons for instance), but rather for broad range of typical interconnects – single-ended and differential, stripline and microstrip, simple planar and with the vertical transitions or vias, etc. Such comparison should be done consistently both in frequency (magnitude and phase of S-parameters) and time (TDR and optionally eye diagram) domains. In other words, the systematic validation or benchmarking is needed to make sure that the board is manufactured as designed, measurements are taken properly and, finally, that the interconnect analysis software provides acceptable accuracy. It is a whale of a project, if you do it the first time without much experience. Fortunately, there are a number of reports about similar projects to follow [1]-[4]. Here we will use the "sink or swim" approach [4] as the basis. It can be divided into seven steps (includes the board design and manufacturing):

1. *Select materials and define PCB stackup with the manufacturer.*
2. *Design test structures with the EM analysis (simple links, launches, vias …).*
3. *Manufacture the board and mount the connectors.*
4. *Measure S-parameters and validate quality of the measurements with formal quality metrics and visual inspection.*
5. *Do a cross-section of the board and identify the manufacturing adjustments (if any).*
6. *Identify broadband dielectric and conductor roughness models with GMS-parameters or SPP Light techniques.*
7. *Simulate all structures with the identified or validated material models and confirmed adjustments. Compare consistently S-parameters and TDR with the measurements (no further manipulations with the data or "calibration" are allowed at this step).*

Next sections of this paper outline the selection of the materials and board design with the stackup structure close to a typical production board. We proceed with the measurement process description, board cross-sectioning, material parameters identification and, finally, see how close to the reality we can get by following the process.

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III. VALIDATION BOARD DESIGN

A validation platform is a very important tool to pre-qualify a manufacturer, benchmark signal integrity software or learn how to do the measurements at the microwave to millimetre wave frequency bandwidth. The accuracy and limitations of the software can be easily identified with the analysis to measurement comparisons on a typical set of interconnect structures. A validation platform can be either developed in-house or purchased from a vendor. One of the industry-first validation platforms was the physical layer reference design board (PLRD-1) from Teraspeed Consulting Group [1]. Example of a readily available validation platform is the CMP-28/32 channel modelling platform from Wild River Technology featured in [3]. Off the shelf validation platforms are convenient tools to learn, but the stackup and interconnect geometry in such platforms may be not representative for a production board. Custom validation platforms with the stackup structure similar to a production board have to be used in such cases, as it is done in this project. The board design starts from the material selection and stackup definition. Panasonic Megtron6 material was selected for the high-speed routing layers. The board has 20 layers with 8 layers assigned for the high-speed signals as shown in Fig. 1. The target impedance has been specified for PCB manufacturer ¬- the manufacturer has to fulfil it with 8% tolerance. That is too large variation to expect good correlation even up to 40 GHz, but this is the usual choice for a production board. The manufacturer provided expected trace widths and spacing adjustment. Stackup for the pre-layout analysis was defined as shown in Fig. 1 on the right side – this is the best we can do at this stage. Megtron6 specs provide dielectric constant and loss tangent at multiple frequencies. It is expected that the Wideband Debye (aka Djordjevic-Sarkar) model defined with any of the point from specs provides a good approximation over the target frequency bandwidth.

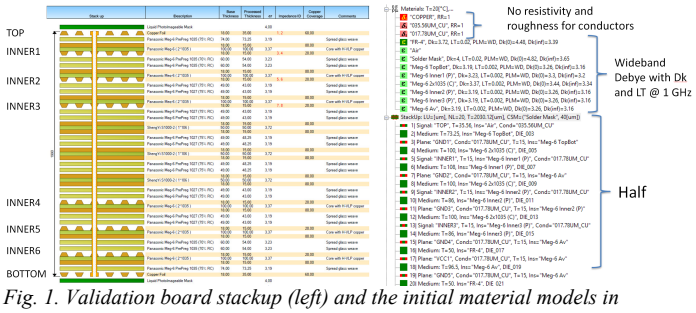

Fig. 1. Validation board stackup (left) and the initial material models in Simbeor software (right).

The values for Dk in the Fig. 1 are the ones used by PCB manufacturer based upon their experience with this material. The major problem is with the conductor roughness model – all we know that the copper foil roughness is specified as H-VLP and no other data. PCB manufacturer also roughens the shiny side of the copper foil during the board manufacturing, without any parameters for the electrical modelling. Even if we would have data for the mate side of the copper foil from the copper foil manufacturer, the PCB manufacturer treatment of the shiny side makes it practically useless. Thus, we start without the conductor roughness model and with the trace adjustments provided by the PCB manufacturer.

Considering the structures to put on the validation board, first of all, it should be structures for the material model identification/validation. For identification with GMS-parameters [5] or SPP Light [6] two segments (5 cm and 10 cm) of differential or single-ended transmission lines for each unique layer are used. In addition we use the Beatty standard (series resonator), to confirm that the extracted models work for traces with different widths. The line segments used for the material identification can be also used as tests for simple differential and single-ended links (they are similar to the traces used on production boards). In addition to that, we decided to put structures usually used in interconnects for the serial and parallel interfaces: diff. and single-ended (SE) via-holes for each routing layer; AC coupling capacitors similar to used on SERDES links; meandering line segment similar to used on DDR links; diff. link skew compensation structures. All are routed at an angle to the edge of the board to avoid the fiber weave effect. The final board layout with all structures is shown in Fig. 2.

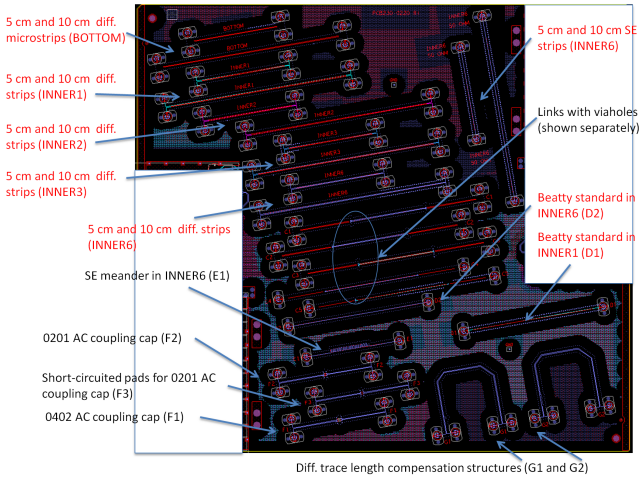

Fig 2. Layout of 20-layer validation board (red legends are for the material identification structures).

The most important elements of the validation board design are the launches. Launches for either probes or connectors have to be optimized. If launches reflect too much, it is usually make them more susceptible to manufacturing variations and more difficult to de-embed for the material identification. **The design target is to minimize the reflection and minimize the sensitivity to manufacturing variations.** The board is designed to have either 2.92 or 2.40 mm compression-mount connector mounted on the TOP layer. Connectors from two vendors were used. Five low-reflection launches were designed to connect the TOP and BOTTOM for structures with microstrip lines, TOP to INNER1,2,3 (with back-drilling), and TOP to INNER6 (with small stubs). Stackup/materials obtained from the manufacturer are used to simulate and optimize the launches. All launches are designed to be functional up to 30 GHz.

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At the end of the board layout phase we can make the following reality observations:

- *The PCB is manufactured with the "impedance control" process – all trace width and spacing are adjusted by the PCB manufacturer (must be accounted in the post-layout analysis).*
- *No information on trace shape (etching).*
- *No reliable information on solder mask shape/parameters.*
- *No information on conductor roughness model.*
- *No information on actual backdrilling.*

All this makes the post layout analysis inaccurate and practically useless for the target bandwidth.

IV. Measurements and GMS-parameters

The main goal during the measurement step of this project is to have accurate high-quality S-parameters measured from 10 MHz to 40 GHz. Also, the S-parameters should be suitable for the extraction of the reflection-less Generalized Modal S-parameters (GMS-parameters) for the material parameters identification [5] up to 30 GHz. Achieving this goal happened to be the most challenging and lengthy step.

The board was manufactured as scheduled and the S-parameters were measured first with TDNA. The formal quality metrics of these S-parameters was barely acceptable. Though, the visual inspection revealed a lot of noise in the S-parameters magnitudes. The GMS-parameters [5] computed with these S-parameters were also very noisy and considered not acceptable for the material identification. If we would proceed with the noisy GMS-parameters, the material identification becomes ambiguous above 10 GHz. Thus we decided to find the other measurement options. In the process a few attempts have been made – with 26 GHz VNA, multiple 40 GHz VNAs and one 50 GHz VNA.

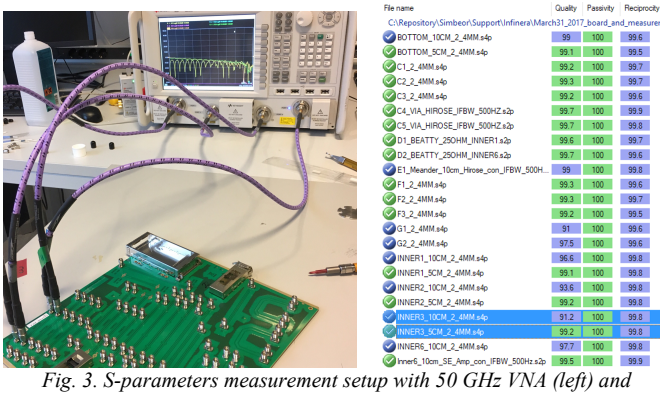

Fig. 3. S-parameters measurement setup with 50 GHz VNA (left) and final Simbeor quality metrics (right, the metrics are in process of standardization by IEEE T370 PG3).

The final measurement setup with 50 GHz VNA is shown in Fig. 3. The measurements came out with the high formal quality metrics as shown on the right side of the Fig. 3. However, a closer look at the lower frequencies revealed a problem – the reflection parameters converge to incorrect values at frequencies below 70 MHz. VNA vendor explained this as the defect of the electronic calibration kit. To overcome the problem and be able to identify conductor resistivity, we did additional measurements with a mechanical calibration kit, but it had lower bandwidth and used for the resistivity identification only.

In the conclusion to this section, we should stress that the broadband measurements of S-parameters for the signal integrity purpose are particularly challenging and not all measurement equipment is suitable – this not the common knowledge! SI problems require high accuracy over extremely broad bandwidth. Though at this step, the GMS-parameters are successfully extracted up to 30 GHz (see section VI) which is sufficient to identify the frequency-continuous material models that are expected to work up to 40-50 GHz. Also, measurements down to 10 MHz are available, to identify the copper resistivity.

V. Board Cross-Sectioning

Before the material parameters identification, we have to know the actual geometry of the traces for the material identification structures. As was observed in similar project [4], the actual geometry can be very far from the expectations and the analysis results without knowing it are unreliable.

Traces on the material identification structures, launches, Beatty in INNER6 and some viaholes have been cross-sectioned as shown in Fig. 4. This is not a statistical investigation but rather validation of how far are our expectations based on the adjustments provide by the manufacturer. Analysis of the cross-sections of traces in layers INNER1 is shown in Fig. 4 on the right. Analysis of the cross-sections in layer INNER6 and BOTTOM is shown in Fig. 5.

The first observation is that the prepreg layer thickness is 3-5 um thinner than provided by the manufacturer (expectation column in Fig. 4 and 5). With that adjustment the thickness of the interior prepreg layers becomes closer to the thickness of the core layer. The second observation is that the geometry of the stripline traces are very close to the expectations. Even without the cross-sectioning, the material identification and analysis results would be very close. Though, it is totally different for the microstrips as we can see on the Fig. 5. The final trace width and distance adjustments are summarized in Fig. 6. The most critical adjustments for the microstrips are highlighted in red. The microstrip metal layer thickness is 48 um instead of expected 35 um and solder mask layer has thickness 10 um over strips and 38 um between the strips – that was not known in advance. The analysis with the microstrip geometry from the board layout or even with the adjustments obtained from manufacturer would lead to characteristic impedance mismatch about 3 Ohm for the single-ended and about 6 Ohm for the differential microstrip traces. We can state that the analysis with the trace width and spacing specified in the original layout are not acceptable to provide good accuracy even below 10 GHz due to considerable impedance mismatch. The microstrip traces adjustments cannot be predicted and properly accounted for without the cross-sectioning. Though, the adjustments provided by the board manufacturer for stripline layers can be safely used. In addition to traces, some viaholes marked in Fig. 4 were cross-sectioned and compared with the expectations –

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the results are available in the complete report [7]. At this point everything is ready for the material models identification.

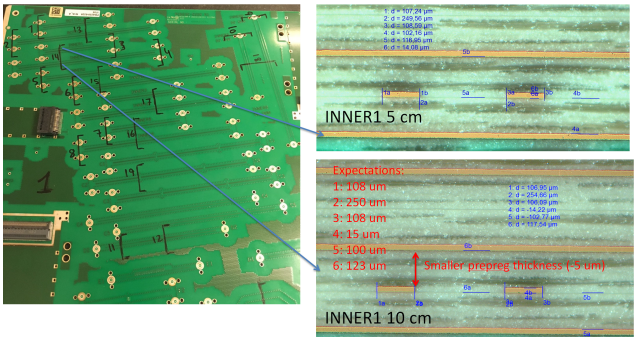

Fig. 4. Validation board cross-sectioning plan (left) and example of the cross-sectioning analysis for 5 cm and 10 cm links in layer INNER1 (right).

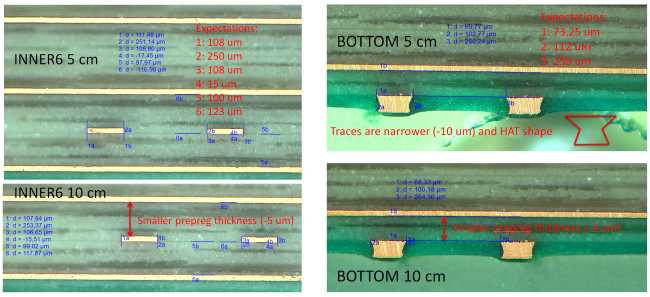

Fig. 5. Cross-sectioning analysis for 5 cm and 10 cm links in layer INNER6 (left) and in layer BOTTOM (right, large differences).

Designed trace dimensions:
BOTTOM: 120-250-120 [um]
INNER1/6: 110-250-110 [um]
INNER2/3: 100-250-100 [um]
INNER6 SE: 110 [um]
BEATTY INNER1 and INNER6:
110 um 2.5 cm, 330 um 2.5 cm

Dimensions from manufacturer:
BOTTOM: 112-258-112 [um]
INNER1/6: 107-250-107 [um]
INNER2/3: 99-245-99 [um]
INNER6 SE: 109 [um]

Dimensions after cross-sectioning:
BOTTOM: HAT(89/97)-260-HAT(89/97) [um]
INNER1/6: 107-255-107 [um]
INNER2/3: 96-254-96 [um]
INNER6 SE: 109 [um]
BEATTY INNER 6:
109 um 2.5 cm + 326 um 2.5 cm

Fig. 6. Width-distance-width adjustments for the differential traces and width adjustment for single ended traces (can be applied only for the impedance controlled segments).

VI. Material Model Identification

For the material parameters identification we use measurements obtained with 50 GHz VNA and electronic calibration kit. The measurements with the mechanical calibration kit are used to identify the copper resistivity for INNER6 layer only (used for all conductors). But first, let's see how useful the dielectric data from the manufacturer (Fig. 1). The extracted reflection-less GMS parameters allow precise analysis of the model deficiencies [5].

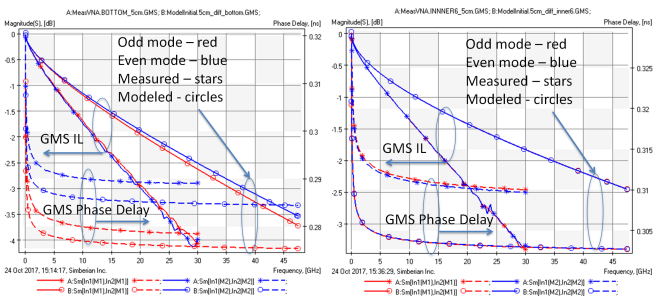

*Fig. 7. Measured (stars) and **modelled without roughness** (circles) GMS insertion loss and phase delay for 5 cm differential segment in layers BOTTOM (left plot, microstrips) and INNER6 (right plot, striplines).*

Generalized modal insertion loss and phase delay for differential microstrip and striplines are shown in Fig. 7 as an example of the initial measurement to simulation comparison. We can observe some differences in the modal phase delays – the model with manufacturer data predicts lower delays. More important, the measured and simulated modal insertion losses are dramatically different. Such difference makes any analysis with the spreadsheet or manufacturer data completely useless above about 3 GHz - this is the reality! All that is due to absence of data for the roughness model.

There are multiple ways to proceed with the material models identification (see overview in [4] and [5]). Typically, raw or de-embedded S-parameters are used to "tune" corresponding model (sometimes called "model calibration"). This is acceptable technique, but too complicated due to large number of non-zero S-parameters in the case of differential traces. The simplest way is to use just two GMS-parameters and the following formal process (identification with dielectric and conductor loss separation):

1. *Identify copper resistivity by matching measured and simulated GMS insertion loss (GMS IL) at the lowest frequencies.*
2. *Identify dielectric constant (Dk) by matching measured and simulated GMS phase delay (GMS PD).*
3. *Identify loss tangent by matching GMS IL at lower frequencies (below 1-2 GHz) and re-adjust Dk to match GMS PD (changes in LT can affect the delay).*
4. *Identify roughness model parameters by matching GMS IL at high frequencies (above 2-3 GHz) and re-adjust Dk to match GMS PD (roughness can also affect the delay).*
5. *Do it for all unique dielectrics in the stackup.*

There are multiple ways to proceed with the material identification for this stackup. One option is to stick with the core/prepreg stackup structure and identify one model for the core dielectric and three models for the stripline prepreg layers. The identified Wideband Debye models with Dk and LT @ 1 GHz (PCB manufacturer spreadsheet data for comparison are in the brackets):

Layer	Dk	LT
Core (all layers 2x1035 weave)	3.37 (3.37)	0.003 (0.002)
Prepreg INNER1/INNER6 (2x1035 weave, 70% RC)	3.37 (3.23)	0.003 (0.002)
Prepreg INNER2 (2x1027 weave, 75% RC)	3.27 (3.19)	0.002 (0.002)
Prepreg INNER3 (2x1027 weave, 75% RC)	3.25 (3.19)	0.002 (0.002)

Causal Huray-Bracken models [8] with parameters SR=0.098 um, RF=12.5 is used for all stripline layers. A non-causal model would produce about 2 Ohm difference between the measured and modelled TDR impedance [8]. Conductor resistivity was adjusted to 1.2 of the resistivity or the annealed copper. Note that the prepreg and core dielectric parameters came relatively close to the spreadsheet data. This model would be perfect, except one limitation. There will be too small difference in the propagation velocity for the odd and even modes in the differential striplines, to account for the far end cross-talk observed in the measurements (see section VII).

To account for the inhomogeneity of the layered dielectric, additional resin-rich layers around the strips are defined. "Resin-rich" in this context does not mean that this is a resin layer. It may contain different components that make

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properties of this composite material different from the layer with the fabric. The identified Wideband Debye models with Dk and LT @ 1 GHz (PCB manufacturer spreadsheet values are in the brackets):

Layer	Dk	LT
Core (all layers 2x1035 weave)	3.37 (3.37)	0.003 (0.002)
Prepreg INNER1/INNER6 (2x1035 weave, 70% RC)	3.17 (3.23)	0.003 (0.002)
Resin INNER1/INNER6	3.562	0.003
Prepreg INNER2 2-ply (2x1027 weave, 75% RC)	3.124 (3.19)	0.002 (0.002)
Prepreg INNER3 2-ply (2x1027 weave, 75% RC)	3.09 (3.19)	0.002 (0.002)
Resin INNER2/INNER3	3.425	0.002

The conductor and conductor roughness models are the same as for the previous case. The material parameters for the microstrip layer were the same for the two cases with Dk=3.40 (3.19), LT=0.006 (0.002) for prepreg and Dk=3.2 (4.0), LT=0.02 for the solder mask (both Wideband Debye models @ 1 GHz). Causal Huray-Bracken model parameters for microstrip are SR=0.229 um, RF=3.77 (rougher copper is used for the surface layers). Correspondence of the measured and identified GMS-parameters is shown in Fig. 8. There is small difference in the phase delays of the even and odd modes in the strip layers – sufficient to account for the observed far end cross-talk at about -30 dB level. Everything looks good now and we are ready to proceed with the validation step.

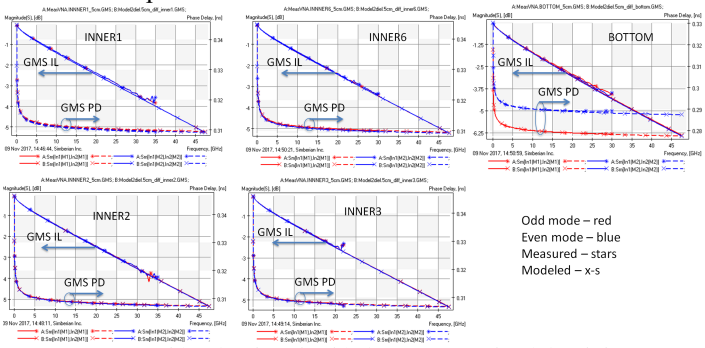
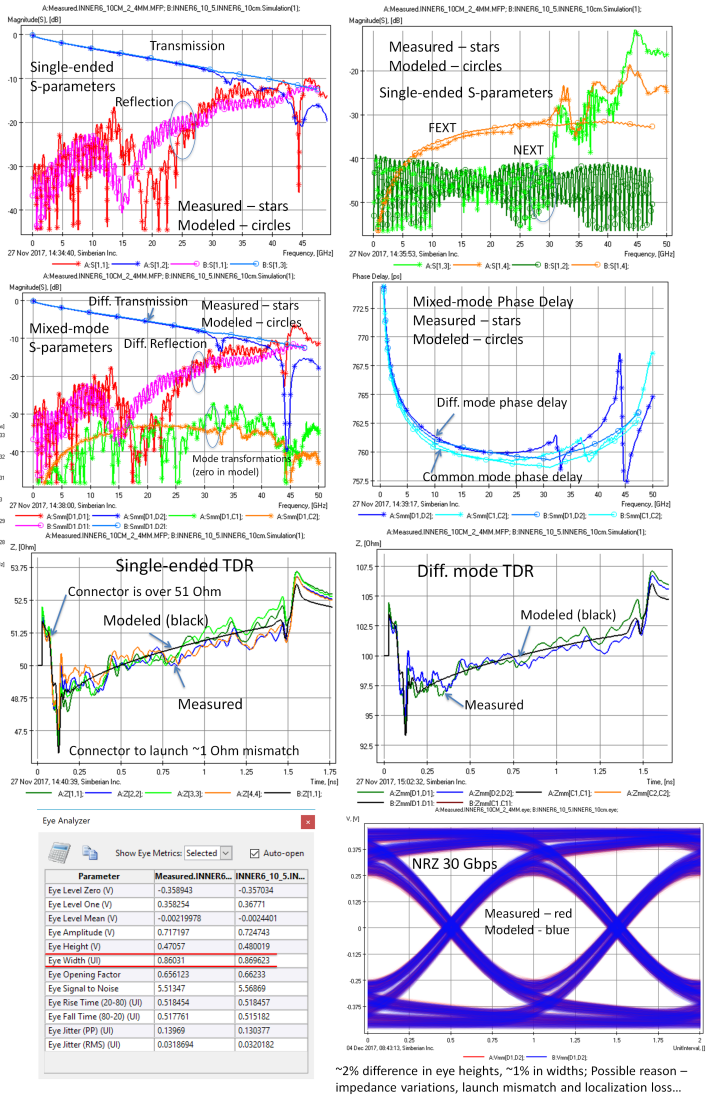


Fig. 8. Measured (stars) and simulated (x-s) GMS insertion loss (IL) and phase delay (PD) for differential transmission lines in all unique layers.

VII. Validation

At the validation step, we simulate all structures on the board with the trace width and shape adjustments identified in section V and dielectric and conductor roughness models identified in section VI. The layered dielectric structure with the "resin-rich" layer is going to be used for all transmission line segments. No further adjustments are allowed at this step. The goal here is not getting a good fit between the measurements and models by tuning the model parameters and showing that we can achieve excellent correlation, but rather to see what accuracy can be achieved based on the formal material identification and limited number of cross-sections. **This is the most important step to have confidence in the manufacturing, measurements and modelling to reveal the potential problems.**

To start the validation, we have to decide what is going to be modelled. There are two options to proceed: either de-embed connectors and launches from the measured data (simpler models) or create models of the measured links with the coaxial connectors and launches. De-embedding on PCBs is notoriously difficult due to the manufacturing variations [1]. We used it only for high-reflective structures, such as Beatty standard. The low-reflective structures are simulated with the connectors and launches. The model of the connector was simply synthesized from S-parameters measured for two connectors connected symmetrically back-to-back. In addition, models for all launches (PCB part) and discontinuities were built with the 3D electromagnetic analysis as a part of the post-layout electromagnetic de-compositional analysis in Simbeor.



~2% difference in eye heights, ~1% in widths; Possible reason – impedance variations, launch mismatch and localization loss...

Fig. 9. Example of detailed analysis to measurement correlation for 10 cm differential link in INNER6 – acceptable correlation up to 30 GHz, about 2% difference in modelled and measured eye diagrams.

Considering what to compare, technically, comparison of the magnitudes and phases of S-parameters is sufficient to make a decision on the accuracy or spot a problem. Though, comparison in time domain is usually also needed and may clarify problems. Comparison with a TDR/TDT response that

is measured directly with TDR scope requires modelling with the step function with the shape and spectrum matching the one used in the experiment – this way has some uncertainties. Here measured and modelled S-parameters can be used to do all time domain computations with exactly the same stimuli matching the bandwidth of the model. After all decisions on the modelling are made, we run the post-layout analysis for all structures on the validation board and compare the magnitudes of S-parameters, phase delays, TDR computed with Gaussian step with 20 ps 10-90% rise time and eye diagrams computed with 30 Gbps NRZ PRBS signal with 25 ps rise and fall time generated with LFSR with order 32.

Example of detailed report for 10 cm differential stripline link in layer INNER6 is provided in Fig. 9. We can observe acceptable correspondence in the single-ended as well as in the mixed-mode S-parameters, to have less than 2% difference in the modelled and simulated 30 Gbps eyes. Substantial discrepancies above 30 GHz on all structures are caused by break out of the launch localization. The main reason for discrepancies in the reflections below 30 GHz is the variation of the impedance along the transmission line that is not accounted for in the model. We do not know what caused these variations – non-homogeneity of the materials or non-uniformity of the trace cross-sections or both. If so, it would be practically impossible to include all those variations in the analysis because of lack of the statistical distributions of the geometry and material parameters. A summary report for 10 structures is provided in Table 1. The first three columns of the table list acceptable correlation bandwidth for the insertion loss (IL), reflection loss (RL), and far and near end crosstalk (FEXT&NEXT). Column TDR shows approximate absolute difference in computed and measured TDRs for single-ended and differential modes. The TDR excludes the connector to launch transition area, where 1.5 / 3.0 Ohm difference was observe on all structures. The eye column shows difference between the simulated and measured 30 Gbps NRZ eyes. Additional observations are listed in the "Notes" column. A complete report for all structures on the validation board is available on request [7].

Table 1. Analysis to measurement correlation report for 10 structures.

Structure	IL [GHz] SE & MM	RL [GHz] SE & MM	FEXT & NEXT [GHz]	TDR (Ω) ~ SE / MM	Eye (30 Gbps, diff.)	Notes
INNER1						There is uncertainty in the epoxy filling after the backdrilling, the launches is more inductive then predicted. DM/CM phase delay correlate up to 25GHz.
5cm	25	15		1 / 2		
10cm	25	15	30	1 / 2	1% EH & EW	
INNER2						Trace width seems to be 95um instead of 99um. Launch more inductive then predicted, PCB trace width variation. DM/CM phase delay correlate up 30 GHz.
5cm	30	25		1 / 2		
10cm	30	25	30	1 / 2	1% EH & EW	
INNER3						Core/prepreg dielectric models – layered anisotropy. Resonance frequency little lower than predicted. Launches have long stubs (not back-drilled).
5cm	30	30		1 / 2		
10cm	30	30	30	1 / 2	3.6% EH, 1% EW	
D2 Beatty						Loss and dispersion models work for much wider strips! Good correspondence in phase delay and TDR.
INNER6	30	30	N/A	1 / N/A	N/A	
BOTTOM						More reflections from 10 to 30 GHz (investigate)... Large variations of impedance along the traces (investigate)...
5cm	30	10-15	30	2 / 4		
10cm	30	10-15	30	2.5 / 5	6% EH, 1.5% EW	
C2 Diff via						Reality: differences in diff. reflection from 10 to 25 GHz and in transmission above 30 GHz. Mode conversions in measurement up to -30dB.
INNER6 (backdr.)	30	15	25	1 / 2	5% EH, 1% EW	

VIII. CONCLUSION

Systematic PCB interconnect analysis to measurement validation process is suggested and successfully used in this paper. The minimal number of steps is outlined, to have acceptable analysis-to-measurement correlation up to 30 GHz on the most of the structures on the validation board. Technically, this is sufficient for the reliable analysis of 28-32 Gbps links. Design of launches and reference plane stitching localization degraded the correlation above 30 GHz. To extend the predictability up to 40-50 GHz, the launches have to be re-designed and manufacturing tolerances should be reduced.

The specificity of the signal integrity problems also dictates very strict requirements for the measurement equipment – accuracy at low and high frequencies is equally important. The reality is that not all measurement equipment satisfies such requirements and this not the common knowledge. Anyone with plans to purchase the equipment (or EDA tools) should try it first without regards to the vendor profile and have software or an expert in the team to evaluate S-parameters quality and validity. The validation boards are the excellent tool to do that. The measurement and EDA tools may be very expensive and not as accurate as claimed by the vendors. The selection of the measurement equipment and components caused substantial delay in this project.

The identified dielectric parameters are very close to the vendor specs. Conductor roughness was the major contributor to the signal degradation and no models were available in advance – analysis without proper conductor roughness models is useless. Causal Huray-Bracken conductor roughness model provided good correlation in the losses and in the TDR impedance.

In conclusion we should state that this is an ongoing project and we keep investigating obtained data in preparation for the next validation board. We expect it will be actually predictable up to 40 GHz.

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