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40 GHz PCB Interconnect Validation: Expectations vs Reality

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Abstract

Frequency content of digital signals in PCB interconnects have increased up to 40-50 GHz in recent years. To ensure that interconnects work as expected over this bandwidth, we have to build validation boards. This paper reports lessons learned from a validation project with the goal to build a formal procedure for systematic prediction of the interconnect behavior up to 40 GHz. We will go through selection of test structures, connectors and measurement equipment, demonstrate uncertainties of the analysis based on the initial pre-manufacturing assumptions and how close to reality we get with more formal approach based on material models and manufacturer adjustments identification.

Author(s) Biography

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Yuriy Shlepnev is President and Founder of Simberian Inc., where he develops Simbeor electromagnetic signal integrity software. He received M.S. degree in radio engineering from Novosibirsk State Technical University in 1983, and the Ph.D. degree in computational electromagnetics from Siberian State University of Telecommunications and Informatics in 1990. He was principal developer of electromagnetic simulator for Eagleware Corporation and leading developer of electromagnetic software for simulation of signal and power distribution networks at Mentor Graphics. The results of his research are published in multiple papers and conference proceedings.

1. Introduction

What does it take to design PCB interconnects with good analysis to measurement correlation up to 40 GHz? Is it doable with typical low-cost PCB materials and fabrication process, typical trace width, via back-drilling and shortage of space to place the stitching vias? Your EDA vendor shows excellent correlation of the analysis tools to measurements even up to 50 GHz, your PCB fabricator ensures that the board will be built as designed and provides all possible information on stackup and materials. Measurements with the easy-to-use TDNA or VNA should be also a "piece of cake". There is nothing to worry about and the designed interconnects should behave as expected. Unfortunately, many SI engineers already learned that this is not the case and the reality can be far from our expectations. To verify practically everything that goes into the design to manufacturing flow at this frequency bandwidth, we are actually forced to build validation boards. Moreover, re-validation has to be done every time when new PCB material or even new batch of materials or new PCB fabricator is used. **The outcome of such validation should be a formal process, and following such a process we reduce the gap between the expectations and reality and are able to reliably predict the behavior of the interconnects on production boards over this bandwidth. That is the main goal of this project**. We do not just show the final analysis to measurement correlation on a case by case basis, as it is usually done in some validation projects, but report a formal procedure based on the material model and manufacturing adjustments identification. The accuracy of the analysis based on the pre-manufacturing assumptions is analyzed and reported. We also discuss un-expected artifacts encountered in the board design, fabrication and measurements (as we all know, stuff happens).

We start with the description of the "dream validation project" – how validation process should look like if everything goes as expected. As the framework, we use the "sink or swim" validation process that was developed and tested with multiple validation boards such as Teraspeed's PLRD-1 [1], Wild River Technology's CMP-08 and CMP-28 [2], [3], Rambus's "lessons learned" board [4]. The project described in this paper can be considered as the first detailed report of the "sink or swim" methodology application for a board with structures close to the production boards.

We proceed with the validation board planning and discuss selection of test structures. In addition to single-ended and differential transmission line segments for the material parameters identification and test structures like the Beatty standards, the board includes common high-speed PCB interconnect structures, such as AC-coupling capacitors, delay matching compensation, meandering line used in DDR circuits, differential and singled ended vias with different number of stitching vias to investigate the energy localization phenomenon. As it is usually done, all structures are designed with the stackup geometry and material parameters provided by the PCB fabricator (pre-manufacturing assumptions).

Next, we show that the bandwidth of the models based on the data available from manufacturer is very limited. Practically, for the target frequency bandwidth it is not possible to predict the interconnect behavior using just the pre-manufacturing assumptions. What would be the minimal possible adjustment of the process to increase the prediction bandwidth and improve the accuracy? First of all, we validate the geometry of the traces with the cross-sectioning. With a few cross-section samples we make new assumption that the identified trace width and shape adjustments are common for the whole board. Next, we use two transmission line segments (single-ended and differential) for each signal layer to properly identify the material models with GMS-parameters [5]. Finally, with the new set of post-manufacturing assumptions based on the limited board cross-sectioning and on S-parameters measurements for just transmission line segments, we go structure by structure and compare the improved models with the measurements. That reveals additional expected and un-expected surprises. The outcome is a relatively simple formal process with a set of recommendations for those who want to design predictable interconnects for validation projects as well as for the production boards.

2. “Sink or Swim” validation process

One of the key elements of design success is the **systematic benchmarking of manufacturing, measurements, and modeling**. Systematic means analysis-to-measurement correlation observed not just for one or two structures (test coupons for instance), but rather for broad range of typical interconnects – single-ended and differential, stripline and microstrip, simple planar and with the vertical transitions or vias, etc. Such comparison should be done consistently both in frequency (magnitude and phase of S-parameters) and time (TDR and optionally eye diagram) domains. In other words, the systematic validation or benchmarking is needed to make sure that the board is manufactured as designed, measurements are taken properly and, finally, that the interconnect analysis software provides acceptable accuracy. It is a whale of a project, if you do it the first time without much experience. Fortunately, there are a number of reports about similar projects to follow [1]-[4]. Here we will use the “sink or swim” approach [4] as the basis. It can be divided into seven steps (which includes the board design and manufacturing):

1. Select materials and define PCB stackup with the manufacturer.
2. Design test structures with the EM analysis (simple links, launches, vias …).
3. Manufacture the board and mount the connectors.
4. Measure S-parameters and validate quality of the measurements with formal quality metrics and visual inspection.
5. Do a cross-section of the board and identify the manufacturing adjustments (if any).
6. Identify broadband dielectric and conductor roughness models with GMS-parameters or SPP Light techniques.
7. Simulate all structures with the identified or validated material models and confirmed adjustments. Compare consistently S-parameters and TDR with the measurements (no further manipulations with the data or “calibration” are allowed at this step).

The initial expectation was to finish the project within 3 months. Which was easier said than done – given the low priority and low resources this project took about a year to complete and we are still investigating the data in preparation for yet another iteration. The major hurdle in this project was actually the measurement equipment. Unfortunately, the knowledge of what measurement equipment works for extremely broadband SI problems and what is not suitable is not a common knowledge and the vendors are not very helpful, to say the least – it was one of the lessons learned in this project.

3. Validation board design

A validation platform is a very important tool to pre-qualify a manufacturer, benchmark signal integrity software or learn how to do the measurements at the microwave to millimeter wave frequency bandwidth. The accuracy and limitations of the software can be easily identified with the analysis to measurement comparisons on a typical set of interconnect structures. A validation platform can be either developed in-house or purchased from a vendor. One of the industry-first validation platforms was the physical layer reference design board (PLRD-1) from Teraspeed Consulting Group [1]. Use of the PLRD-1 revealed the need and enabled development of the industry-first broadband dielectric and conductor roughness models in the Simbeor software. Example of a readily available validation platform is the CMP-28/32 channel modeling platform from Wild River Technology featured in [3]. Off the shelf validation platforms are convenient tools to learn, but the stackup and interconnect geometry in such platforms may be not representative for a production board. Custom validation platforms with the stackup structure similar to a production board have to be used in such cases, as it is done in this project.

The board design starts from the material selection and stackup definition. Panasonic Megtron6 material was selected for the high-speed routing layers. Some pre-manufacturing specs provided by the board fabricator are shown in Fig. 3.1. The board has 20 layers with 8 layers assigned for the high-speed signals as shown in Fig. 3.2. The target impedance has been specified for PCB manufacturer - the manufacturer has to fulfill it with some tolerances. This is the usual choice for a production board. The manufacturer provided expected trace width and spacing adjustments as shown in the right table in Fig 3.1. The expected impedance variations are within 8%, that is too large to expect good correlation up to 40 GHz, but it is typical value. Vias with 0.20mm (7.9 mil) padstack in board layout are to be drilled with 0.250mm diameter drill (9.85 mil). Non-functional pads on signal vias on any layer are not allowed. Via backdrilling is to be done for some structures.

General Information	Value
PCB revision	PCB230-0220_R1
Dimension	261,35 x 237.36 mm +0,00/-0,20
Unit	mm
Number of layers	20
Thickness	2 mm
Quality requirements	IPC-6012 Class 2
Controlled impedance	Yes, 8% tolerance
UL-Requirement	94V0
High Voltage	No
Material	Megtron6 R-5775(K) (2x1035) "core" with ½ oz H-VLP copper (spread weave) Megtron6 R-5670(K) Pre-preg 1035 (75% RC) (spread weave) Megtron6 R-5670(K) Pre-preg 1035 (70% RC) (spread weave) Megtron6 R-5670(K) Pre-preg 1027 (75% RC) (spread weave) FR4 "core", 50 um thick with ½ oz copper
PCB-Finish	Immersion silver
General Info	
Solder Mask Color	Green

No roughness model

Layer	Z (ohm)	Tolerance (%)	Trace dimensions using datasheet values (mm)	PCB vendor estimated trace dimensions (mm)
TOP/BOTTOM (MS)	50	≤ 10	0.135	0.127
TOP/BOTTOM (MS)	100 Diff.	≤ 10	0.120 (edge-to-edge gap: 0.250)	0.112 (edge-to-edge gap: 0.258)
INNER1/INNER6 (SL)	50	≤ 8	0.110	0.109
INNER1/INNER6 (SL)	99 Diff.	≤ 8	0.110 (edge-to-edge gap: 0.250)	0.107 (edge-to-edge gap: 0.250)
INNER2/INNER3/ (SL)	50	≤ 8	0.100	0.099
INNER2/INNER3 (SL)	99 Diff.	≤ 8	0.100 (edge-to-edge gap: 0.250)	0.099 (edge-to-edge gap: 0.245)

Fig. 3.1. Validation board materials and trace widths and adjustments obtained from manufacturer.

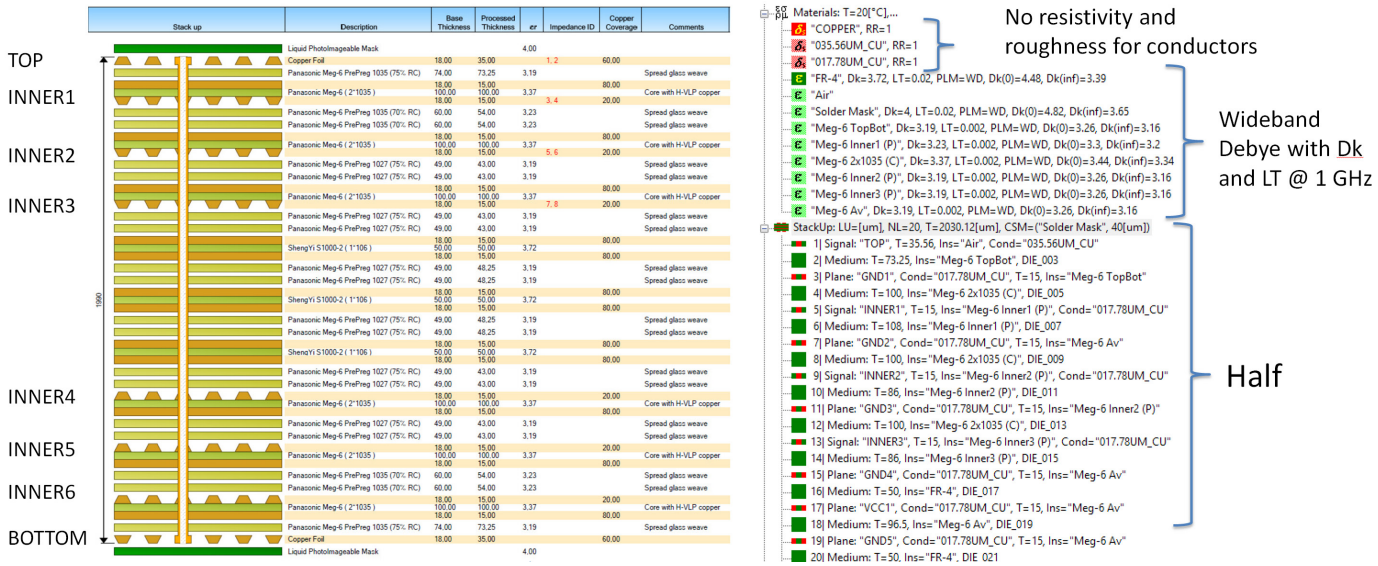


Fig. 3.2. Validation board stackup (left) and the initial material models in Simbeor software (right).

Stackup for the pre-layout analysis was defined as shown in Fig. 3.2 on the right side – this is the best we can do at this stage. Megtron6 specs provide dielectric constant and loss tangent at multiple frequencies. It is expected that the Wideband Debye (aka Djordjevic-Sarkar) model defined with any of the point from specs provides a good approximation over the target frequency bandwidth.
The values for Dk in the Fig. 3.2 are the ones used by PCB manufacturer based upon their experience with this material. The major problem is with the conductor roughness model – all we know that the

copper foil roughness is specified as H-VLP and no other data. PCB manufacturer also roughens the shiny side of the copper foil during the board manufacturing, without any parameters for the electrical modeling. Even if we would have data for the mate side of the copper foil from the copper foil manufacturer, the PCB manufacturer treatment of the shiny side makes it practically useless. Thus, we start without the conductor roughness model and with the trace adjustments provided by the PCB manufacturer. Obviously, this will not provide a good correlation for the insertion loss, and the model identification is needed – this should be expected. Though, the data may be acceptable for design of launches and vias. Ideally, a test coupon with the same stackup should be built for the material identification, to identify the conductor surface roughness model, to improve accuracy of the pre-layout analysis. The validation board may be considered as such coupon.

Considering the structures to put on the validation board, first of all, it should be structures for the material model identification/validation. For identification with GMS-parameters [5] or SPP Light [6] two segments of differential or single-ended transmission lines for each unique layer have to be used. In addition we can use the Beatty standard (series resonator), to confirm that the extracted models works for traces with different widths. The line segments used for the material identification can be also used as tests for simple differential and single-ended links (they are similar to the traces used on production boards). In addition to that, we decided to put structures usually used in interconnects for the serial and parallel interfaces: diff. and single-ended (SE) via-holes for each routing layer; AC coupling capacitors similar to used on SERDES links; meandering line segment similar to used on DDR links; diff. link skew compensation structures. All are routed at an angle to the edge of the board to avoid the fiber weave effect. The final board layout with all structures is shown in Fig. 3.3 and Fig. 3.4.

The most important elements of the validation board design are the launches. Launches for either probes or connectors have to be optimized. If launches reflect too much, it is usually make them more susceptible to manufacturing variations and more difficult to de-embed for the material identification. The design target is to minimize the reflection and minimize the sensitivity to manufacturing variations. The board is designed to have either a 2.92 or 2.4 mm compression-mount connector mounted on the TOP layer. Connectors from two vendors were used. Five low-reflection launches were designed to connect the TOP and BOTTOM for structures with microstrip lines, TOP to INNER1 (with backdrilling), TOP to INNER2 (with backdrilling), TOP to INNER3 (with backdrilling) and TOP to INNER6 (no backdrilling). Stackup/materials obtained from the manufacturer are used to simulate and optimize the launches. Examples of the launch designs are shown in Fig. 3.5 and 3.6. The launches are simulated and optimized using de-compositional approach without connectors – it degrades the model quality and the models are expected to work only up to 30 GHz. All launches are designed with 9 stitching vias located on a circle with diameter 2.3 mm (91 mil). Stitching vias connect all reference planes together and the metal patches in the TOP layer. Stitching vias have drill hole diameter 0.250 mm (9.85 mil). Distance from signal via to stitching vias is about quarter of wavelength at 30 GHz (quarter of wavelength in dielectric is about 1.35 mm) – it is expected that the launches should gradually lose the localization at about 30 GHz (the impedance of the short circuiting vias at a quarter wavelength distance becomes very high, close to open). We cannot expect good correlation above that frequency. Though, it is expected that the impedance of the return path will remain low due to large parallel planes and a lot of stitching vias placed along the transmission line segments.

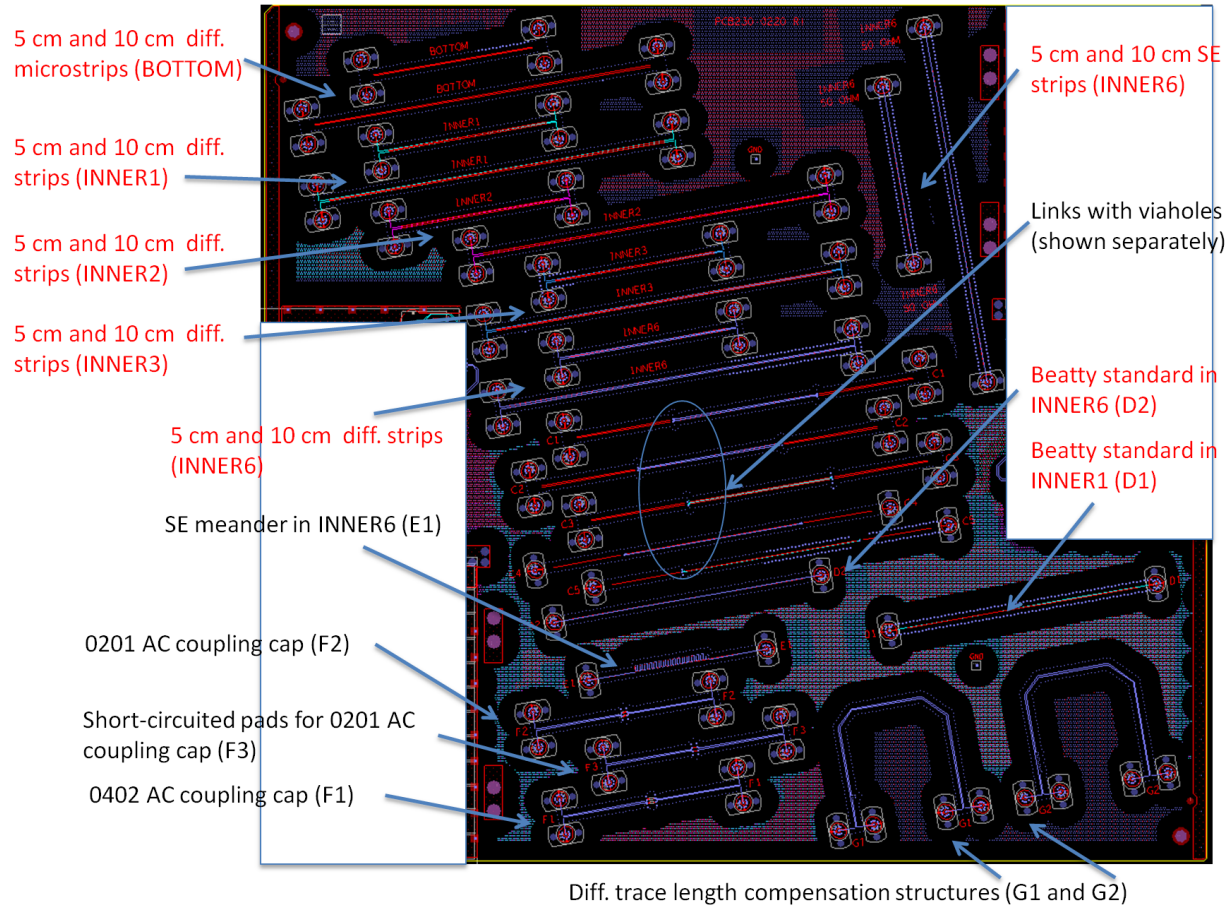


Fig 3.3. Layout of 20-layer validation board (red legends are for the material identification structures).

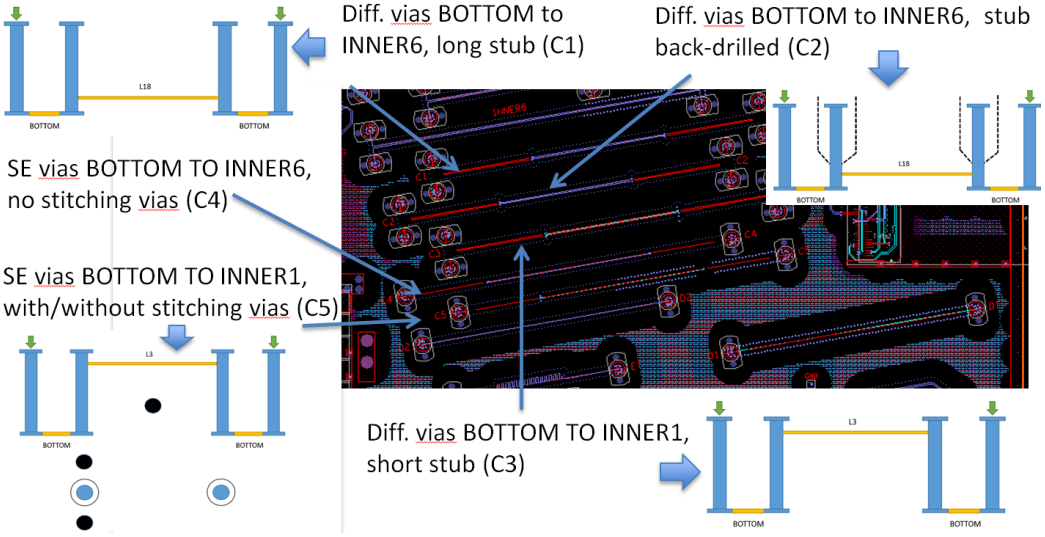


Fig. 3.4. Layout of links with single-ended (SE) and differential viaholes.

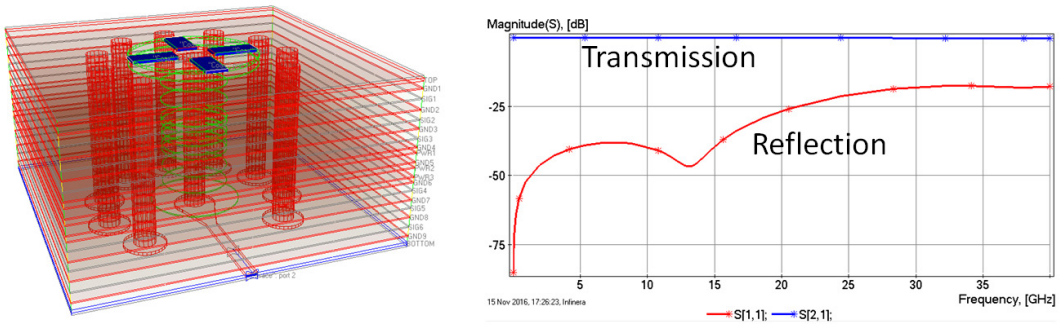


Fig. 3.5 TOP to BOTTOM layer launch design for microstrip structures – the reflection loss is below -20 dB up to 27 GHz and below -10 dB up to 40 GHz.

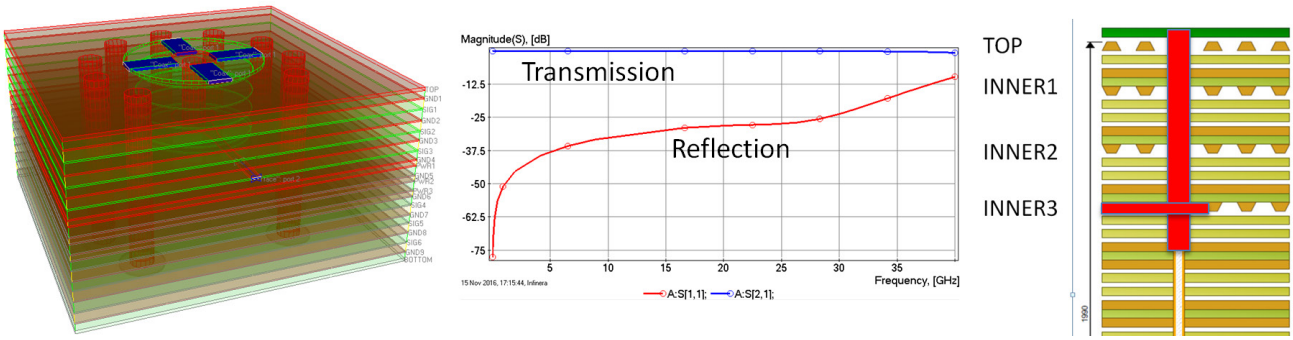


Fig. 3.6. *TOP to INNER3 layer launch design for stripline structures in layer INNER2 – the reflection loss is below -20 dB up to 33 GHz and below -10 dB up to 40 GHz.*

After the board was designed and sent to the manufacturer, we have noticed that the metal traces were put in the TOP layer as is visible on Fig. 3.3. Fortunately, that did not matter because the TOP layer was isolated from all traces on the board by the solid metal plane. In the end of the board layout phase we can make the following reality observations:

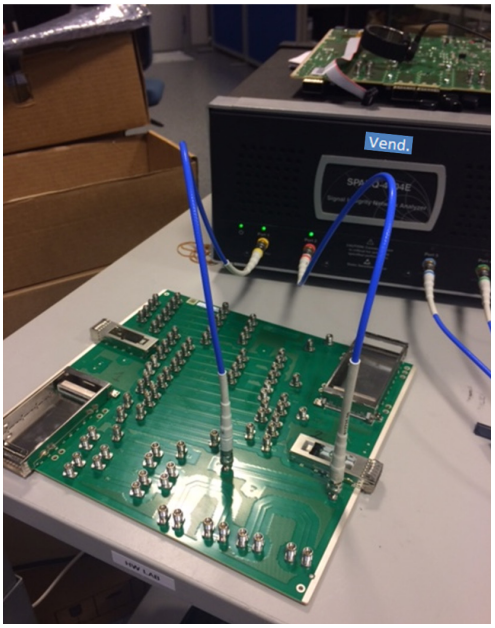
- Via diameter is defined to be 0.2 mm (7.9 mil) in layout file, but 0.25 mm drill (9.85 mil) is supposed to be used by the manufacturer – it should be accounted in the post-layout analysis.
- The PCB is manufactured with the "impedance control" process – all trace width and spacing are adjusted by the PCB manufacturer that is also not reflected in the layout file, but should be accounted for the post-layout analysis.
- No information on trace shape (important for the losses evaluation).
- No information on solder mask shape/parameters.
- No information on conductor roughness model.
- No information on actual backdrilling.

All this makes the post layout analysis inaccurate and practically useless at the target frequencies. This is mostly because of the absence of the conductor roughness model. It is expected that the H-VLP roughness and additional copper processing by the manufacturer will substantially degrade the signal above 3-5 GHz, but we have no data to evaluate these additional losses. This should be expected in any project without the test coupons built upfront with exactly the same materials and manufacturer. Though, it is expected that the dielectric parameters and stackup structure from manufacturer may be acceptable to design the vertical transitions.

4. Measurements and GMS-parameters extraction

The main goal during the measurement step is to have accurate high-quality S-parameters measured from 10 MHz to 40 GHz. Considering the manufacturing variations and launches localization, the S-parameters should be suitable for the extraction of the reflection-less Generalized Modal S-parameters (GMS-parameters) for the material parameters identification [5] up to 30 GHz. Achieving this goal happened to be the most challenging and lengthy step of this project.

The board was manufactured as scheduled and the S-parameters were measured first with TDNA as shown in Fig. 4.1. The formal quality metrics of these S-parameters was barely acceptable as shown on the right side of Fig. 4.1. Though, the visual inspection revealed a lot of noise that is clearly visible on the S-parameters magnitude plots shown for just two structures in Fig. 4.2. That level of noise may be acceptable for a preliminary validation. However, the Generalized Modal S-parameters [5] computed with these S-parameters were also very noisy as illustrated in Fig. 4.3. The reality was either to proceed with these noisy data or find other options.



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C3_c.s4p	90.2	100	90.9
C4.s2p	90.4	100	87.2
C5.s2p	89.4	100	89.5
D1.s2p	89.9	98.1	83.8
D2.s2p	90.8	100	82.8
diff_bottom_long.s4p	90.3	100	90.7
diff_bottom_short.s4p	89.4	100	88.7
diff_inner1_long.s4p	89.3	100	91.8
diff_inner1_short.s4p	90.2	100	90.6
diff_inner2_long.s4p	89.5	100	92.5
diff_inner2_short.s4p	90.1	100	90.7
diff_inner3_long.s4p	88.7	93.8	92.4
diff_inner3_short.s4p	88.5	93.1	91.5
diff_inner6_long.s4p	91.4	100	92.9
diff_inner6_short.s4p	57	100	90.7
E1_Meander.s2p	89.7	100	87.2
F1_0402.s4p	89.6	99.8	88.9
F2_0201.s4p	90.2	100	88.8
F3_strips.s4p	88.3	99.9	88.5
se_inner6_long.s2p	91	100	86.9
se_inner6_short.s2p	90.3	100	84.5

Fig. 4.1. S-parameters measurement setup with TDNA (left) and final Simbeor quality metrics (right, IEEE T370 PG3).

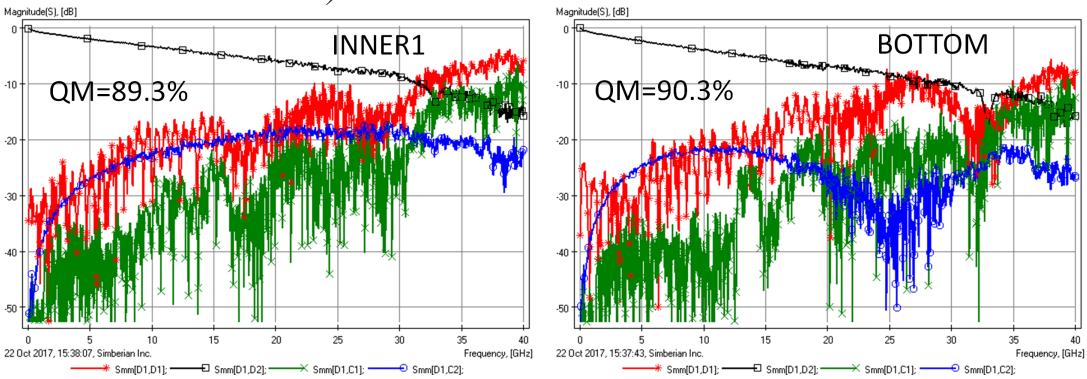


Fig. 4.2. Example mixed-mode S-parameters measured with TDNA for diff. 10 cm segments in layers INNER1 (stripline, left) and BOTTOM (microstrip, right) – acceptable quality metrics, but noisy

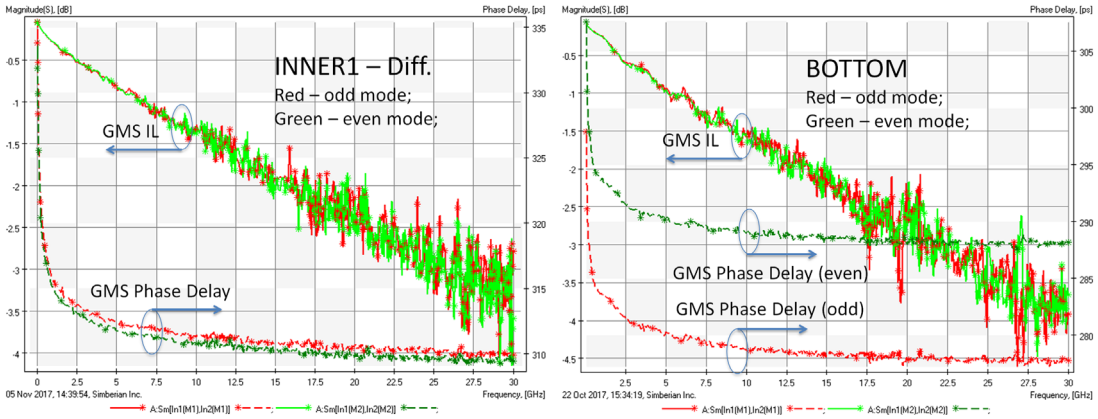
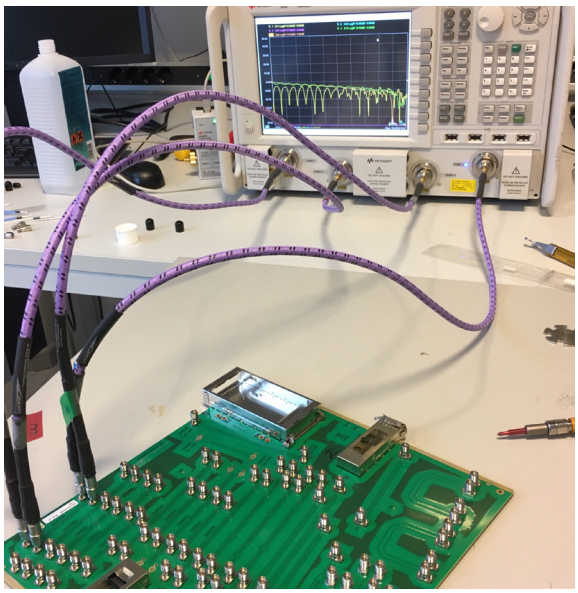


Fig. 4.3. GMS-parameters computed with S-parameters measured with TDNA for 5 cm diff. stripline in layer INNER1 (left) and 5 cm diff. microstrips (right) – may be acceptable up to 10 GHz.

If we proceed with the noisy GMS-parameters, the material identification would be ambiguous above 10 GHz – this reality fact was way too far from our expectations. Thus we decided to find the other measurement options. In the process a few attempts have been made – with 26 GHz VNA, multiple 40 GHz VNAs and one 50 GHz VNA.

The measurement setup with 50 GHz VNA is shown in Fig. 4.4. One of the first reality problems we faced with this piece of equipment was very thick cables that came with it – the measurements could not be done for the differential structures because of the connectors were placed too close. Thinner cables have been used instead with possible expected degradation of the measurement quality. The measurements came out with high formal quality metrics as shown on the right side of the Fig. 4.4. However, a closer look at the lower frequencies revealed a problem illustrated in Fig. 4.5 – it looks like the reflection parameters converge to incorrect values (it should flatten at lower frequencies). An attempt to build rational approximation and use it to extrapolate data to DC failed as illustrated on the right plot in Fig. 4.5. Note, that TDNA data at lower frequencies showed proper convergence.



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BOTTOM_5CM_2_4MM.s4p	99.1	100	99.5
C1_2_4MM.s4p	99.2	100	99.7
C2_2_4MM.s4p	99.3	100	99.7
C3_2_4MM.s4p	99.2	100	99.6
C4_VIA_HIROSE_IFBW_500HZ.s2p	99.7	100	99.9
C5_VIA_HIROSE_IFBW_500HZ.s2p	99.7	100	99.8
D1_BEATTY_25OHM_INNER1.s2p	99.6	100	99.7
D2_BEATTY_25OHM_INNER6.s2p	99.7	100	99.6
E1_Meander_10cm_Hirose_con_IFBW_500H...	99	100	99.8
F1_2_4MM.s4p	99.3	100	99.6
F2_2_4MM.s4p	99.3	100	99.7
F3_2_4MM.s4p	99.2	100	99.5
G1_2_4MM.s4p	91	100	99.6
G2_2_4MM.s4p	97.5	100	99.6
INNER1_10CM_2_4MM.s4p	96.6	100	99.8
INNER1_5CM_2_4MM.s4p	99.1	100	99.8
INNER2_10CM_2_4MM.s4p	93.6	100	99.8
INNER2_5CM_2_4MM.s4p	99.2	100	99.8
INNER3_10CM_2_4MM.s4p	91.2	100	99.8
INNER3_5CM_2_4MM.s4p	99.2	100	99.8
INNER6_10CM_2_4MM.s4p	97.7	100	99.8
Inner6_10cm_SE_Amp_con_IFBW_500Hz.s2p	99.5	100	99.9

Fig. 4.4. S-parameters measurement setup with 50 GHz VNA (left) and final Simbeor quality metrics (right, the metrics are in process of standardization by IEEE T370 PG3).

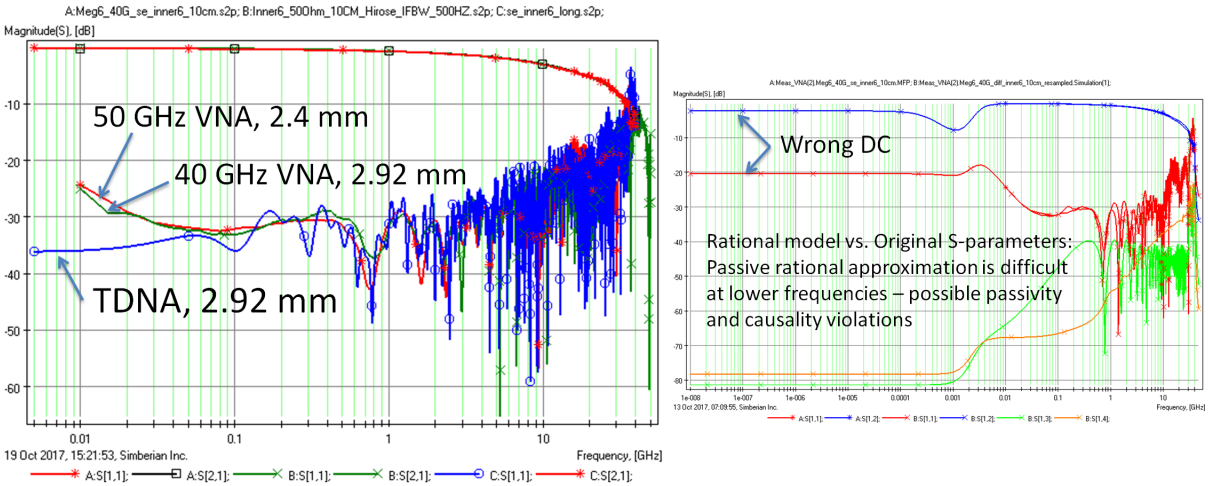

Fig. 4.5. Problem with VNA measurements at lower frequencies (left), attempt to extrapolate the results with the rational approximation (right, stars – measured, x – rational approximation).

The VNA vendor explained the low frequency divergence is caused by the electronic calibration kit and recommended to use a mechanical calibration kit instead. The mechanical calibration kit indeed helped to some extent, as illustrated in Fig. 4.5. Unfortunately, the available kit reduced the upper measurement frequency down to 26 GHz that was not acceptable. Thus, we have used these measurements to validate the results obtained with the electronic calibration kit and to identify the conductor resistivity only. To proceed with the data measured with electronic calibration kit up to 50 GHz, we have cut the measured data below 70 MHz as illustrated in Fig. 4.6.The rational approximation to DC is more realistic in this case and still indicates good quality of the remaining data, but the extrapolation to DC is not reliable – the data cannot be used for the copper resistivity identification. It may also lead to not reliable DC convergence on TDR and substantial problems with the eye diagram computation with such S-parameters. As stated in [7] "*...a 0.5 dB error injected at a lower frequency (<10 MHz) on transmission could take an 85% open eye to a fully closed eye*" – that is scary statement.

Further visual inspection of the S-parameters of the differential transmission line segments revealed big resonance in the insertion loss for the traces in layer INNER3 and smaller resonances above 30 GHz in all traces as shown in Fig. 4.7. The reality is that the stubs on the launches to INNER3 layer were not backdrilled – that reduced considerably the bandwidth of the GMS-parameters for layer INNER3. That is not big problem because of material parameters identified for layer INNER2 are expected to work for the layer INNER3 – the layers are expected to be identical.

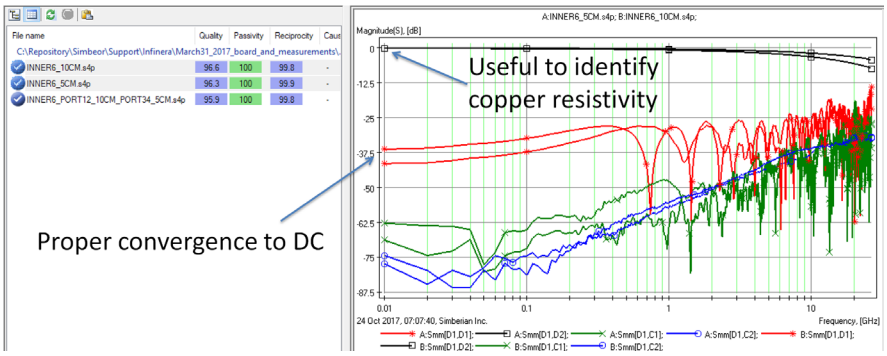

Fig. 4.6. S-parameters measured with 50 GHz VNA with mechanical calibration kit.

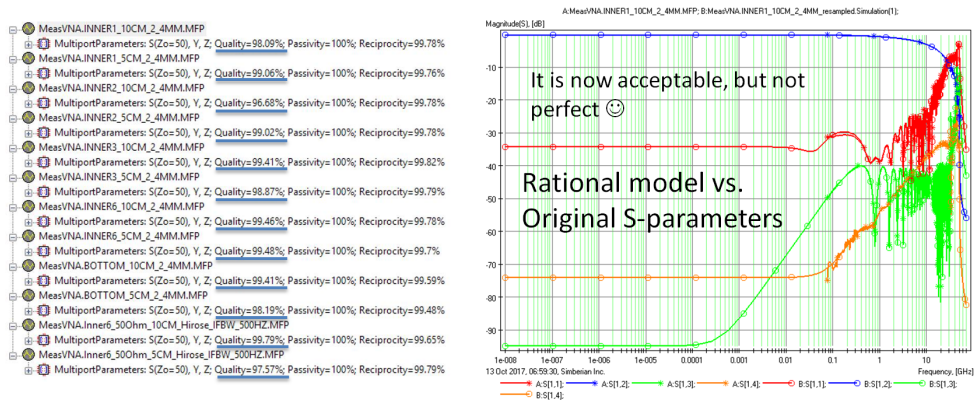

Fig. 4.7. Possible workaround for the low frequency problem – cut the measured data below 70 MHz and use rational approximation for extrapolation.

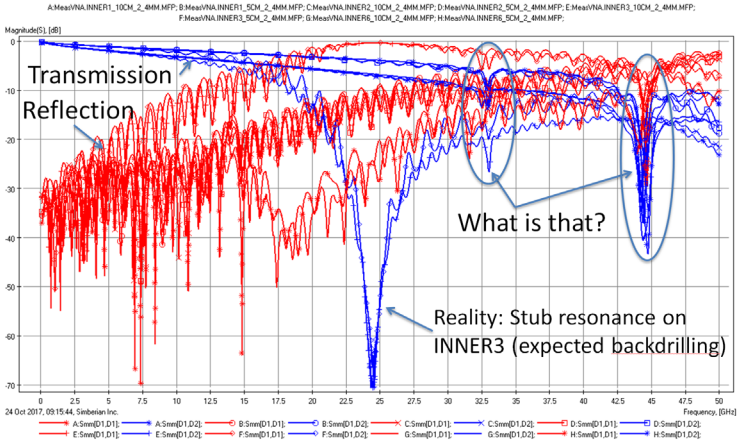

Fig. 4.8. Visual inspection of S-parameters for differential material identification structures.

The final goal of this stage is to have clean GMS-parameters for the material model identification. GMS parameters of 5 cm (about 2 inch) transmission line segments are computed from measured S-parameters of two segments with 5 cm (about 2 inch) and 10 cm (about 4 inch) lengths. GMS-parameters are S-parameters of the line segment in the modal space normalized to the characteristic impedances of the modes – they are reflection-less and do not have mode transformation parameters. This is the simplest form of S-parameters that can be used to identify the material properties with high accuracy [5]. GMS-parameters of differential transmission line segments are 4 by 4 matrices with just 2 unique non-zero elements - modal transmission parameters for odd model (mode 1) and even mode (mode 2). The reflection and mode transformation parameters are zero by definition. That makes it particularly attractive for the material identification purpose. The complex propagation constant (Gamma) can be extracted from the GMS-parameters of segment by taking the logarithm and dividing it by the segment length. Gamma can be used for the material identification as is done in the SPP Light technique [6]. Though, we did not do this additional step in this project – after all, it is an additional step. Also the results should be nearly identical as shown in [6].

The final step before the extraction of GMS-parameters is to pre-qualify the line segments with the TDR. Examples of such pre-qualification are shown on the left plots of Fig.4.7 and 4.8. The impedance variations are within 2-3 Ohms that is expected to be acceptable to extract the GMS-parameters up to 25-30 GHz (see sensitivity analysis at [8]). Examples of GMS-parameters extracted for microstrip lines and striplines in layer INNER6 are also shown in Fig. 4.9 and 4.10 respectively, on the right plots (raw

data, no post-processing). Either the manufacturing variations or the launch localization or, most likely both factors, prevented the GMS-parameters extraction above 30 GHz – the insertion losses were particularly noisy above 30 GHz (not shown on the plots). Phase delays are less sensitive to the variations [8]. GMS-parameters came out as acceptable up to 30 GHz for all structures, except for the INNER3 layer. The stub resonances visible on the Fig. 4.8 restricted the frequency bandwidth down to 20 GHz. Fortunately, the layer INNER3 is expected to have exactly the same materials and can be used for the identification.

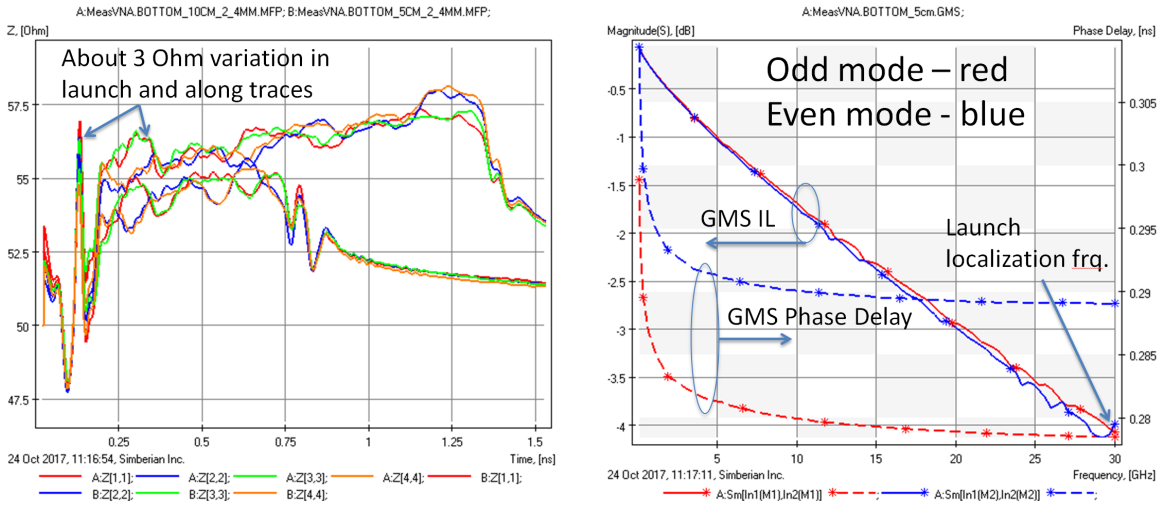

Fig. 4.9. TDR for 5 cm and 10 cm diff. microstrip traces (left plot) and GMS-parameters for the odd and even modes (insertion loss and phase delay) of the 5 cm difference segment (right plot).

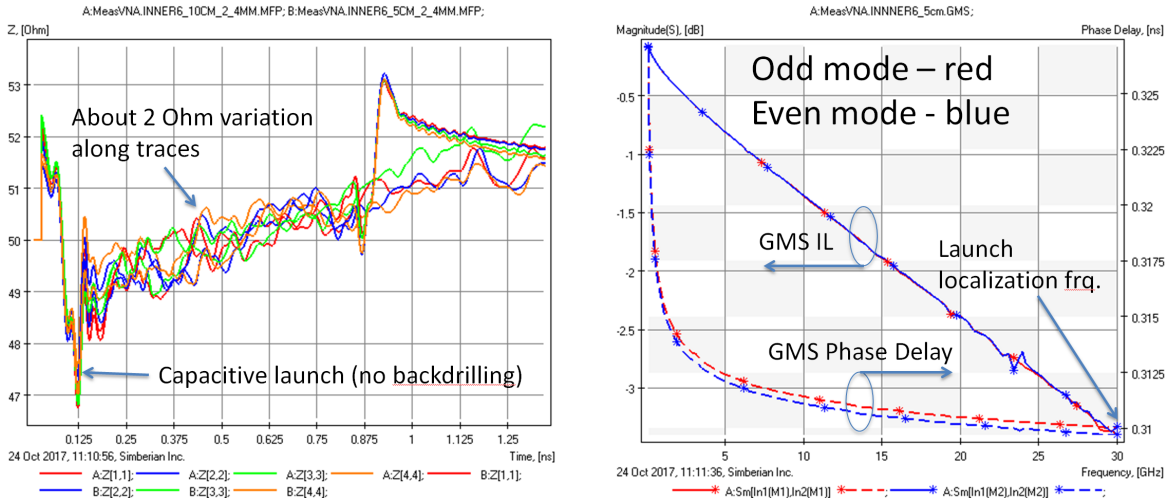

Fig. 4.10. TDR for 5 cm and 10 cm diff. stripline traces in layer INNER6 (left plot) and GMS-parameters for the odd and even modes (insertion loss and phase delay) of the 5 cm difference segment (right plot).

As we can see on the right plot of Fig. 4.9, the odd (differential) and even (common) modes have different propagation delay and attenuation that is expected for the microstrip structures (inhomogeneous dielectric). On the other hand, the stripline structures in homogeneous dielectric should have nearly identical phase delay for the odd and even modes (small differences may be due to the

internal conductor inductance). However in reality we have observed some difference of the phase delay for the odd and even modes for all stripline structures on the validation board. It is clearly visible for the stripline in layer INNER6 at the Fig. 4.10. This indicates that the dielectric has some inhomogeneity. The consequence of this inhomogeneity is the difference in the mode propagation that leads to the far end crosstalk (FEXT) that is expected to be nearly zero for the striplines.

As s conclusion to this section, we should stress that the broadband measurements of S-parameters for the signal integrity purpose are particularly challenging and not all measurement equipment is suitable – this not the common knowledge! SI problems require high accuracy over extremely broad bandwidth. Switching from one tool to another requires a lot of planning and preparation. It is one of the reality lessons learned in this project. Though at this step, **the GMS-parameters are successfully extracted up to 30 GHz which is sufficient to identify the frequency-continuous material models that are expected to work up to 40-50 GHz.** Also, measurements down to 10 MHz are available, to identify the copper resistivity.

5. What is in the board?

Before the material parameters identification, we have to know the actual geometry of the traces for the material identification structures. As was observed in similar project [4], the actual geometry can be very far from the expectations and the analysis results without knowing it are unreliable.

Traces on the material identification structures, launches, Beatty in INNER6 and some viaholes have been cross-sectioned as shown in Fig. 5.1. This is not a statistical investigation but rather validation of how far are our expectations based on the adjustments provide by the manufacturer (see Fig. 3.1). Analysis of the cross-sections of links in layers INNER1 is shown in Fig. 5.1 on the right. Analysis of the cross-sections in layer INNER6 and BOTTOM are shown in Fig. 5.2 and 5.3.

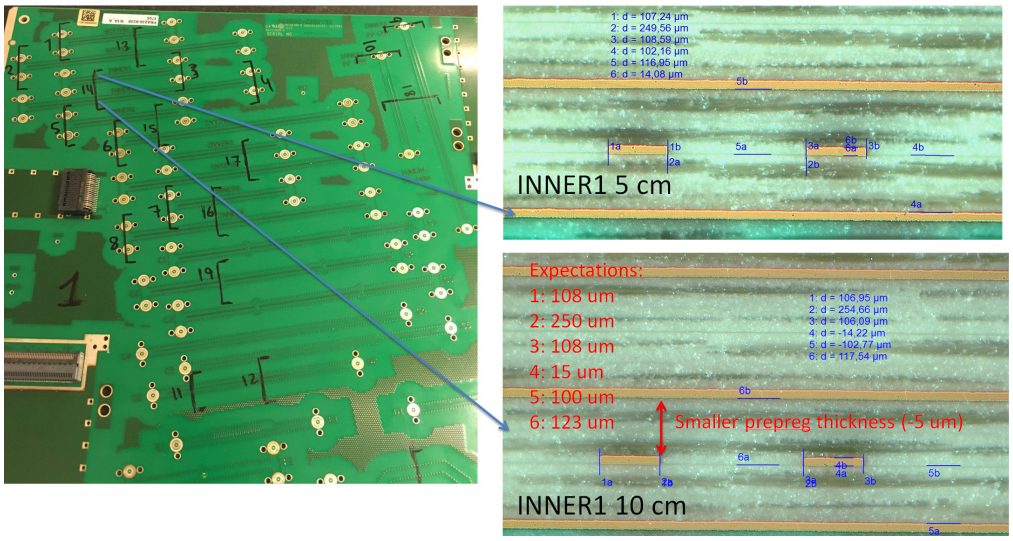

Fig. 5.1. Validation board cross-sectioning plan (left) and example of the cross-sectioning analysis for 5 cm and 10 cm links in layer INNER1 (right).

The first observation is that the pre-preg layer thickness is 3-5 um thinner than provided by the manufacturer (see Fig. 3.2). With that adjustment the thickness of the interior pre-preg layers becomes closer to the thickness of the core layer. That makes sense – pressed and baked pre-preg should be the same material as the core if both laminates are from the same manufacturer and same batch.

The second observation is that the geometry of the stripline traces are very close to the expectations. Even without the cross-sectioning, the material identification and analysis results would be very close. Though, it is totally different for the microstrips as we can see on the Fig. 5.2 and 5.3. The microstrip layer is thicker than expected, traces are narrower by about 10 um and the trace shape is not rectangular but rather "hat" or a "butterfly" shape. Also, the solder mask is very thick between the traces and thin on top of the microstrips. This is typical, but we cannot guess this at all without the cross-sectioning. Analysis based on the numbers provided by the manufacturer (Fig. 3.1 and 3.2) would give the impedance lower by 2-3 Ohm and different losses (the losses depend on the trace shape).

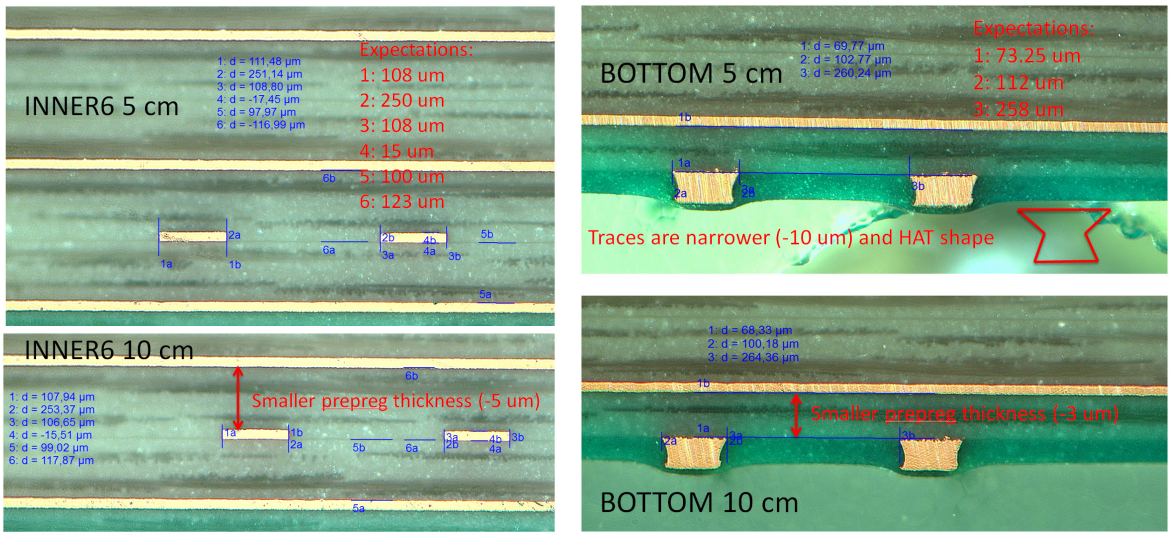

Fig. 5.2. Cross-sectioning analysis for 5 cm and 10 cm links in layer INNER6 (left) and in layer BOTTOM (right).

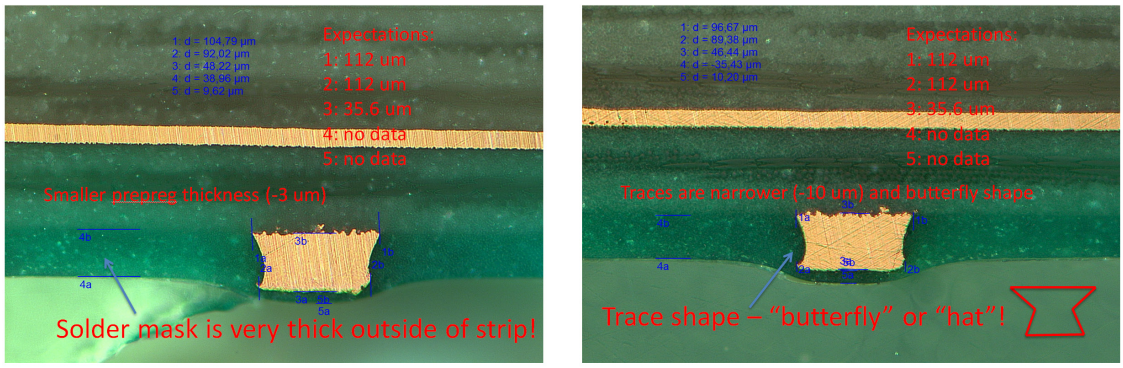

Fig. 5.3. Close up of the cross-sectioning analysis for 5 cm (left) and 10 cm (right) links in layer BOTTOM (microstrip).

Designed trace dimensions:
BOTTOM: 120-250-120 [um]
INNER1/6: 110-250-110 [um]
INNER2/3: 100-250-100 [um]
INNER6 SE: 110 [um]
BEATTY INNER1 and INNER6:
110 um 2.5 cm, 330 um 2.5 cm

→

Dimensions from manufacturer:
BOTTOM: 112-258-112 [um]
INNER1/6: 107-250-107 [um]
INNER2/3: 99-245-99 [um]
INNER6 SE: 109 [um]

→

Dimensions after cross-sectioning:
BOTTOM: HAT(89/97)-260-HAT(89/97) [um]
INNER1/6: 107-255-107 [um]
INNER2/3: 96-254-96 [um]
INNER6 SE: 109 [um]
BEATTY INNER 6:
109 um 2.5 cm + 326 um 2.5 cm

Fig. 5.4. Width-distance-width adjustments for the differential traces and width adjustment for single ended traces (can be applied only for the impedance controlled segments).

The final trace width and distance adjustments are shown in Fig. 5.4. The most critical adjustments for the microstrips are highlighted in red. Also, the microstrip metal layer thickness is 48 um instead of expected 35 um and solder mask layer has thickness 10 um over strips and 38 um between the strips – that was not known in advance. The analysis with the microstrip geometry from the board layout or even with the adjustments obtained from manufacturer would lead to characteristic impedance mismatch about 3 Ohm for the single-ended and about 6 Ohm for the differential microstrip traces. We can state that the analysis with the trace width and spacing specified in the original layout are not acceptable to provide good accuracy even below 10 GHz due to considerable impedance mismatch. The microstrip traces adjustments cannot be predicted and properly accounted for without the cross-sectioning. Though, the adjustments provided by the board manufacturer for stripline layers can be safely used. In addition to traces, some viaholes marked in Fig. 5.1 were cross-sectioned and compared with the expectations – the results are available in the complete report [9]. At this point everything is ready for the material models identification.

6. Material parameters identification

For the material parameters identification we use measurements obtained with 50 GHz VNA and electronic calibration kit. The measurements with the mechanical calibration kit are used to identify the copper resistivity for INNER6 layer only (used for all strips). But first, let's see how useful the spreadsheet data from the section 3 (Fig. 3.1 and 3.2 and middle column in Fig. 5.4). The extracted reflection-less GMS parameters allow precise analysis of the model deficiencies. Generalized modal insertion loss and phase delay for differential microstrip and striplines are shown in Fig. 6.1 as an example of the initial measurement to simulation comparison. We can observe some differences in the modal phase delays – the model predicts lower delays. This is expected due to the anisotropy of the layered laminate dielectrics (strip resonator method typically used by laminate manufacturers identifies Dk for the out-of-plane direction). More important, the measured and simulated modal insertion losses are dramatically different. **Such difference makes any analysis with the spreadsheet data useless above about 3 GHz - this is the reality.**

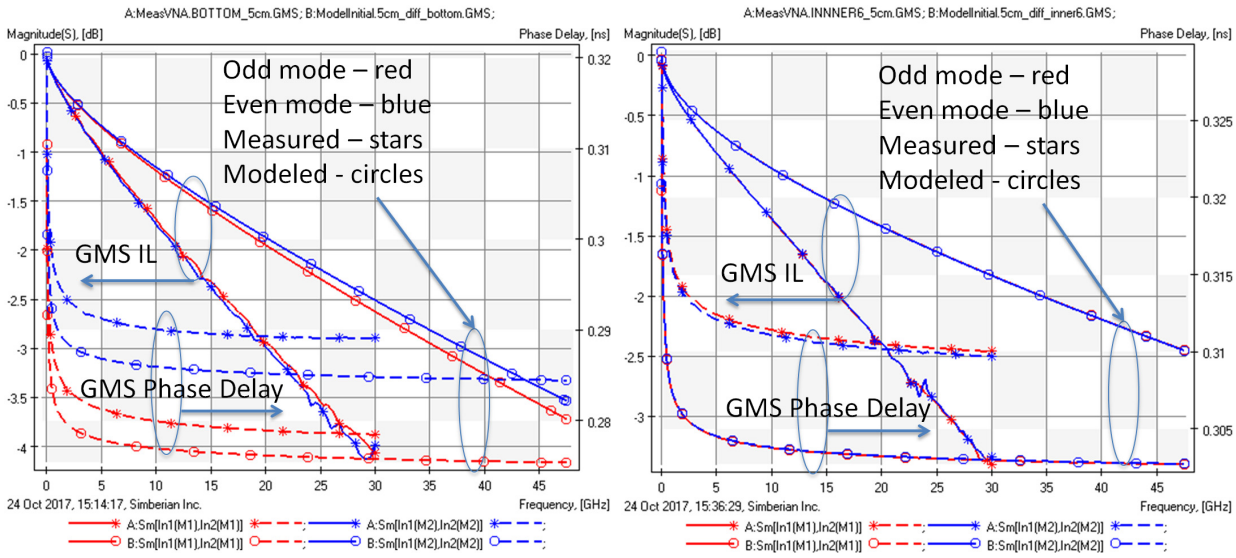

*Fig. 6.1. Measured (stars) and **modeled without roughness** (circles) GMS insertion loss and phase delay for 5 cm differential segment in layers BOTTOM (left plot, microstrips) and INNER6 (right plot, striplines).*

There are multiple ways to proceed with the material models identification (see overview in [4] and [5]). Typically, raw or de-embedded S-parameters are used to "tune" corresponding model (sometimes called "model calibration"). This is acceptable technique, but too complicated due to large number of non-zero S-parameters in the case of differential traces. The simplest way is to use just two GMS-parameters and the following formal process (identification with dielectric and conductor loss separation):

1. Identify copper resistivity by matching measured and simulated GMS insertion loss (GMS IL) at the lowest frequencies.
2. Identify dielectric constant (Dk) by matching measured and simulated GMS phase delay (GMS PD).
3. Identify loss tangent by matching GMS IL at lower frequencies (below 1-2 GHz) and re-adjust Dk to match GMS PD (changes in LT can affect the delay).
4. Identify roughness model parameters by matching GMS IL at high frequencies (above 2-3 GHz) and re-adjust Dk to match GMS PD (roughness can also affect the delay).
5. Do it for all unique dielectrics in the stackup.

There are three ways to proceed with the material identification for this stackup. The simplest way is to assume that the dielectric filling of the layers INNER1/INNER6 and INNER2/INNER3 are homogeneous. After all, the cured pre-preg should be about the same dielectric as the core. The identified Wideband Debye models with Dk and LT @ 1 GHz (PCB manufacturer spreadsheet values are in the brackets) are as follows:

Layer	Dk	LT
INNER1/INNER6 (core 1035 weave, pre-preg 1035 weave)	3.45 (3.23 & 3.37)	0.003 (0.002)
INNER2/INNER3 (core 1035 weave, pre-preg 1027 weave)	3.40 (3.19 & 3.37)	0.002 (0.002)

The conductor surface roughness for all stripline layers is identified as one-level Modified Hammerstad model with SR=0.35 um and RF=2.5. It is just 2 dielectric models – relatively easy to identify and suitable for the analysis of vias and launches, but it compromises the accuracy of trace analysis. In particular, use of non-causal roughness models results in the differential stripline impedance lower than observed on TDR by 2-3 Ohm. Also, use of homogeneous dielectric for each stripline layer results in no difference in phase delay of the even and odd modes and zero far end crosstalk.

Note that the spreadsheet dielectric constant numbers, provided in brackets just for the reference above, are taken from the PCB manufacturer spreadsheet shown in Fig 3.2.
PCB manufacturers use slightly lower Dk values than compared to values from laminate vendor datasheet, they are based on the PCB vendors experience with the material and their test TDR coupons, since they are aiming to achieve desired target impedance.
Comparing these numbers with the datasheet from the dielectric material vendor, shows that dielectric constants correspond to the 10 GHz measurement. Dielectric constants provided at Megtron6(K) datasheet are much closer to identified values, for instance core with 1035 weave has value of Dk = 3.46 – that is closer to the value identified here at 1 GHz.

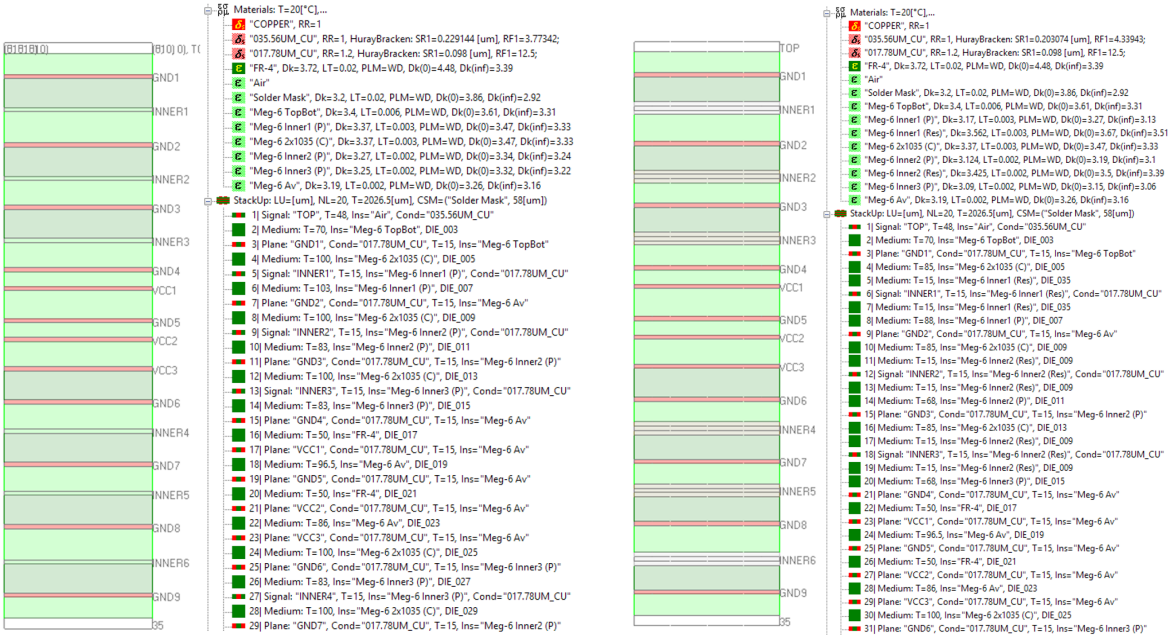

Fig. 6.2. Two possible outcomes of the material model identification – with core and pre-preg layers (left) and with additional resin-rich layer around each strip layer, to account for FEXT (right).

Another option is to stick with the core/pre-preg stackup structure and identify one model for the core dielectric and three models for the stripline pre-preg layers as shown in Fig. 6.2 on the left. The identified Wideband Debye models with Dk and LT @ 1 GHz (**PCB manufacturer spreadsheet data for comparison are in the brackets**):

Layer	Dk	LT
Core (all layers 2x1035 weave)	3.37 (3.37)	0.003 (0.002)
Pre-preg INNER1/INNER6 (2x1035 weave, 70% RC)	3.37 (3.23)	0.003 (0.002)
Pre-preg INNER2 (2x1027 weave, 75% RC)	3.27 (3.19)	0.002 (0.002)
Pre-preg INNER3 (2x1027 weave, 75% RC)	3.25 (3.19)	0.002 (0.002)

In this case causal Huray-Bracken models with parameters SR=0.098 um, RF=12.5 is used for all stripline layers, to account for the difference of the impedances observed on the preliminary TDR comparison. Conductor resistivity was adjusted to 1.2 of the resistivity or the annealed copper. The pre-preg and core dielectric parameters came close to the spreadsheet data in this case. Though, this model has practically the same limitation as the first homogeneous dielectric model. There will be too small difference in the propagation velocity for the odd and even modes in the differential striplines, to account for the FEXT observed in the measurements (see validation section).

Finally, to account for the anisotropy of the layered dielectric, additional resin-rich layers around the strips were defined in the stackup as shown in Fig. 6.2 on the right. “Resin-rich” in this context does not mean that this is a resin layer. It may contain different components that make properties of this composite material different from the layer with the fabric.
The identified Wideband Debye models with Dk and LT @ 1 GHz (PCB manufacturer spreadsheet values are in the brackets):

Layer	Dk	LT
Core (all layers 2x1035 weave)	3.37 (3.37)	0.003 (0.002)
Pre-preg INNER1/INNER6 (2x1035 weave, 70% RC)	3.17 (3.23)	0.003 (0.002)
Resin INNER1/INNER6	3.562	0.003
Pre-preg INNER2 2-ply (2x1027 weave, 75% RC)	3.124 (3.19)	0.002 (0.002)
Pre-preg INNER3 2-ply (2x1027 weave, 75% RC)	3.09 (3.19)	0.002 (0.002)
Resin INNER2/INNER3	3.425	0.002

The conductor and conductor roughness models are the same as for the previous case. The material parameters for the microstrip layer were the same for the last two cases with Dk=3.40 (3.19), LT=0.006 (0.002) for pre-preg and Dk=3.2 (4.0), LT=0.02 for the solder mask (both Wideband Debye models @ 1 GHz). Causal Huray-Bracken model parameters for microstrip are SR=0.229 um, RF=3.77.

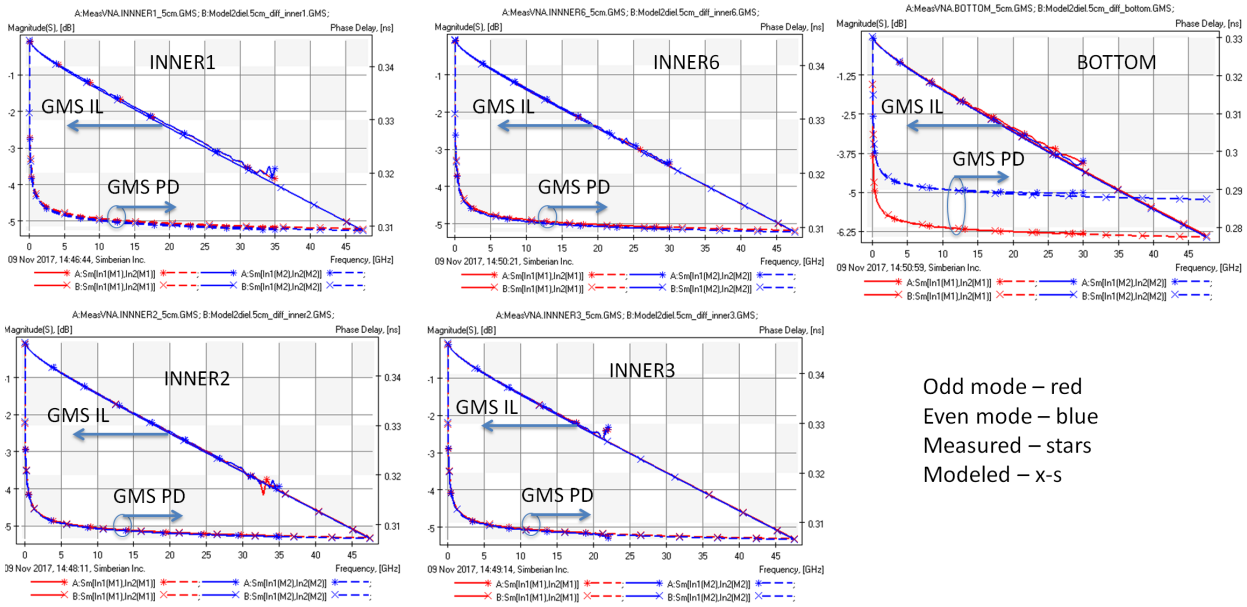

Fig. 6.3. Measured (stars) and simulated (x-s) GMS insertion loss (IL) and phase delay (PD) for differential transmission lines in all unique layers.

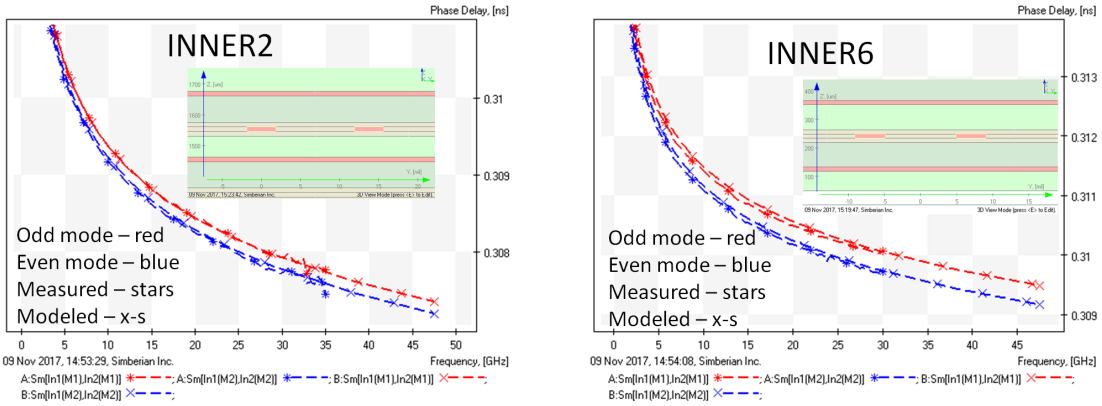

Fig. 6.4. Measured and simulated odd and even mode phase delays for traces in layers INNER2 and INNER6.

Correspondence of the measured and identified GMS-parameters is shown in Fig. 6.3. The advantage of the model with the resin-rich layer around the strips is illustrated in Fig. 6.4. Without the additional layer, phase delays of the even and odd modes are much closer to each other and the FEXT in the model is almost zero, even with different core and pre-preg models. Everything looks good now and we are ready to proceed with the validation step.

7. Validation: expectations vs. reality

At the validation step, we simulate all structures on the board with the trace width and shape adjustments identified in section 5 and dielectric and conductor roughness models identified in section 6. The layered dielectric structure with the "resin-rich" layer is going to be used as the most accurate. No further adjustments are allowed at this step. The goal here is not getting a good fit between the measurements and models by tuning the model parameters and showing that we can achieve excellent correlation, but rather to see what accuracy can be achieved based on the formal material identification and limited number of cross-sections. **This is the most important step to have confidence in the manufacturing, measurements and modeling to reveal the potential problems.**

To start the validation, we have to decide what is going to be modeled. There are two options to proceed: either de-embed connectors and launches from the measured data (simpler models) or create models of the measured links with the coaxial connectors and launches. De-embedding on PCBs is notoriously difficult due to the manufacturing variations [1]. It may distort some measurements (for low reflective structures) and also reduces the frequency bandwidth. We will use it only for high-reflective structures, such as Beatty standard. The low-reflective structures are simulated with the connectors and launches. The connector models were not available. To overcome this obstacle, the model of the connector was simply synthesized from S-parameters measured for two connectors connected symmetrically back-to-back. We used cascaded connection of two coaxial sections to model connector and then matched both magnitude and phase of the reflection and transmission of the measured S-parameters and the circuit model of the back-to-back structure. In addition, models for all launches (PCB part) were built with the 3D electromagnetic analysis as a part of the post-layout electromagnetic de-compositional analysis in Simbeor.

Considering what to compare, technically, comparison of the magnitudes and phases of S-parameters is sufficient to make a decision on the accuracy or spot a problem. Though, comparison in time domain is usually also needed and may reveal additional problems. Comparison with a TDR/TDT response that is measured directly with TDR scope requires modeling with the step function with the shape and spectrum matching the one used in the experiment. A similar procedure is required for the eye diagrams. Use of the ideal ramp step functions or PRBS with ideal trapezoidal shaped pulses may obfuscate and distort the results. Alternatively, measured and modeled S-parameters should be used to do all time domain computations with exactly the same stimuli matching the bandwidth of the model. It can be done in two ways – either with convolution with the impulse response computed directly from discrete S-parameters with IFFT or with the rational approximation and fast recursive convolution as it is done here. The rational approximation is frequency-continuous and naturally extends S-parameters to DC and to infinite frequencies. It is also causal by definition if passivity is ensured. The accuracy of the time domain analysis in this case is defined only by the accuracy of the rational approximation. In other words, the accuracy is always under control, unlike in case of analysis with IFFT where interpolation and extrapolation introduce uncontrolled errors. In addition, the recursive convolution is exact for piecewise linear signals and is much faster than the direct convolution. Thus, we will naturally use the rational approximation for all time-domain computations here. After all decisions on the modeling are made, we run the post-layout analysis for all structures on the validation board and compare the

magnitudes of S-parameters, phase delays, TDR computed with Gaussian step with 20 ps 10-90% rise time and eye diagrams computed with 30 Gbps NRZ PRBS signal with 25 ps rise and fall time generated with LFSR with order 32.

Let's first simulate the differential links used to extract GMS-parameters at the material model identification step, to see how the model scales for longer segments. Fig. 7.1 illustrates the analysis of the complete 10 cm (about 4 inch) differential stripline link in layer INNER6 with the de-compositional electromagnetic analysis in Simbeor software. The link is divided into single-ended and differential microstrip segments and connector + launch discontinuities at four ends. The results of the validation are shown in Fig. 7.2-7.4. Measured and modeled magnitudes of the single-ended S-parameters are compared in Fig. 7.2. There is good correspondence in the insertion loss, FEXT (due to matching odd and even modes as shown in Fig. 6.4) and NEXT up to about 30 GHz (what is going on above 30 GHz is explained in section 8). Though we can see some differences in the reflection parameter starting from about 10 GHz and having impact on the insertion loss around 30 GHz.

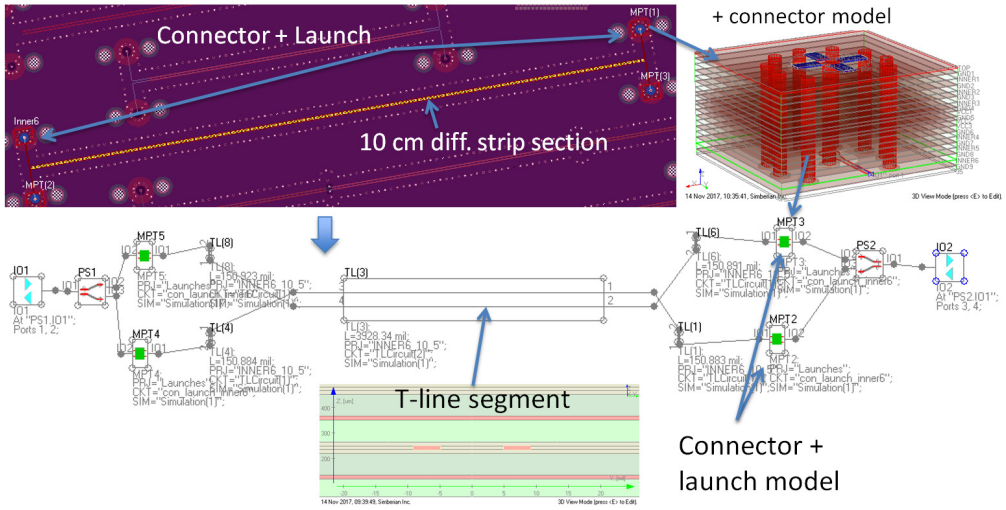

Fig. 7.1. De-compositional electromagnetic model of the diff. stripline link in layer INNER6 (Simbeor).

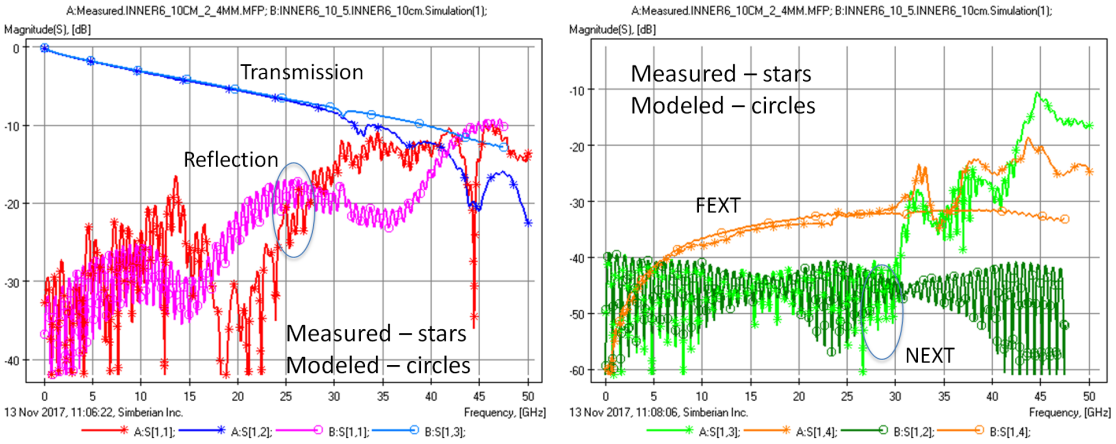

Fig. 7.2. 10 cm diff. strip link in layer INNER6 – measured and modeled magnitudes of single-ended S-parameters.

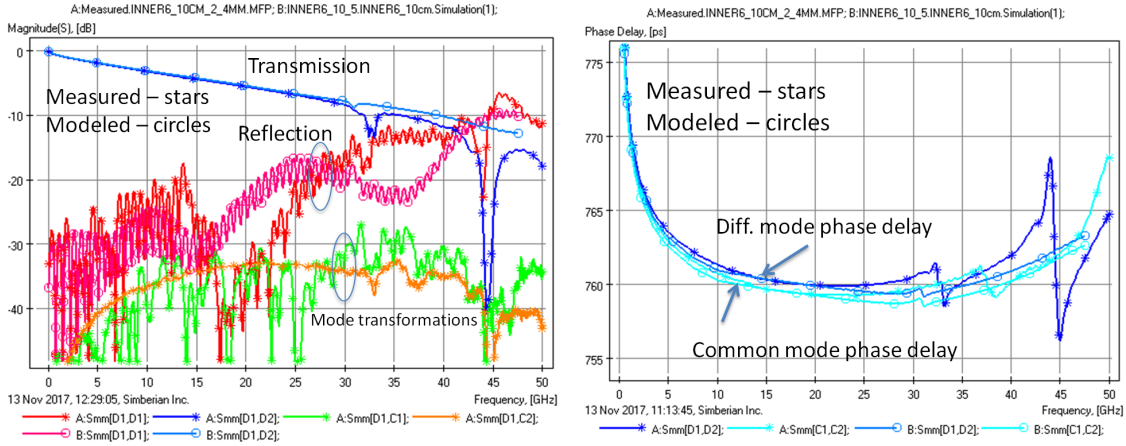

Fig. 7.3. 10 cm diff. strip link in layer INNER6 – measured and modeled mixed-mode S-parameters magnitude (left plot) and phase delay for diff. and common mode transmission parameters (right plot).

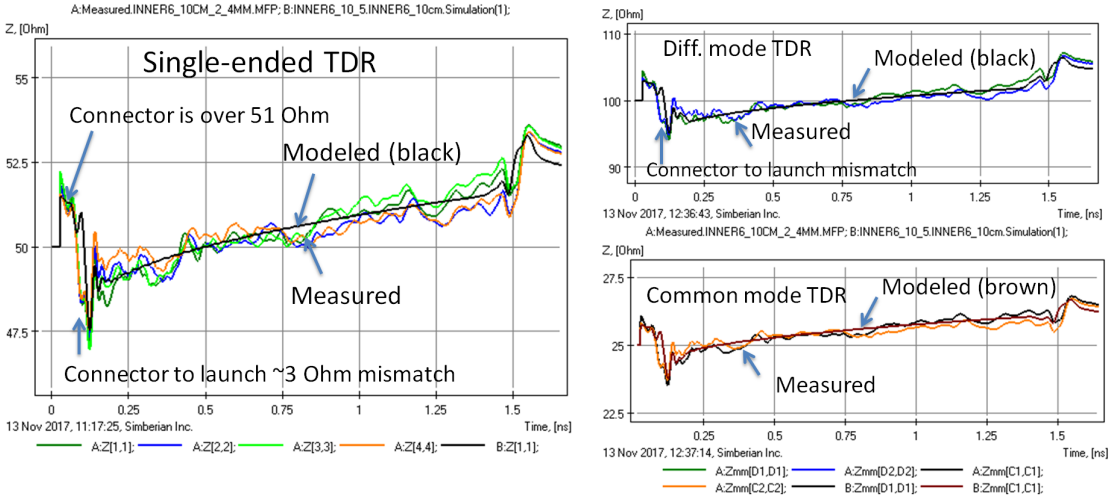

Fig. 7.4. 10 cm diff. strip link in layer INNER6 – single-ended (left plot) and mixed-mode (right plot) measured and modeled TDRs.

Magnitudes and phase delays of the mixed-mode S-parameters are compared in Fig. 7.3. Again, we can observe good correlation in the insertion losses and transmission phase delays. Though, the model predicts practically no mode transformations due to geometrical symmetry of the structure, but in reality we can observe the modal transformation at around –30 dB. Single-ended and mixed-mode TDRs shown in Fig. 7.4 reveal possible reasons of the mismatch in the reflection and mode transformation parameters –we can see about 1 Ohm impedance variations along the strips (close to the expectations based on the data provided by manufacturer – see Fig. 3.1). There is also see about 3 Ohm difference between the model and measurement at the connector to launch interface. That will be further investigated, to improve the model. Notice that the connector impedance came out closer to 51.5 Ohm, instead of 50 Ohm claimed by the manufacturer. A model from manufacturer or based on the connector geometry would not be very helpful in such case (it is usually very close to 50 Ohm). The variations along the traces have statistical nature and cannot be directly accounted for in the model. It can be done only if statistical distributions for strip width, dielectric thickness and possible variations of the dielectric parameters are known. Evaluation of the statistical manufacturing distributions should be done for each manufacturer or provided by the manufacturer. The alternative is to go with more accurate manufacturing process.

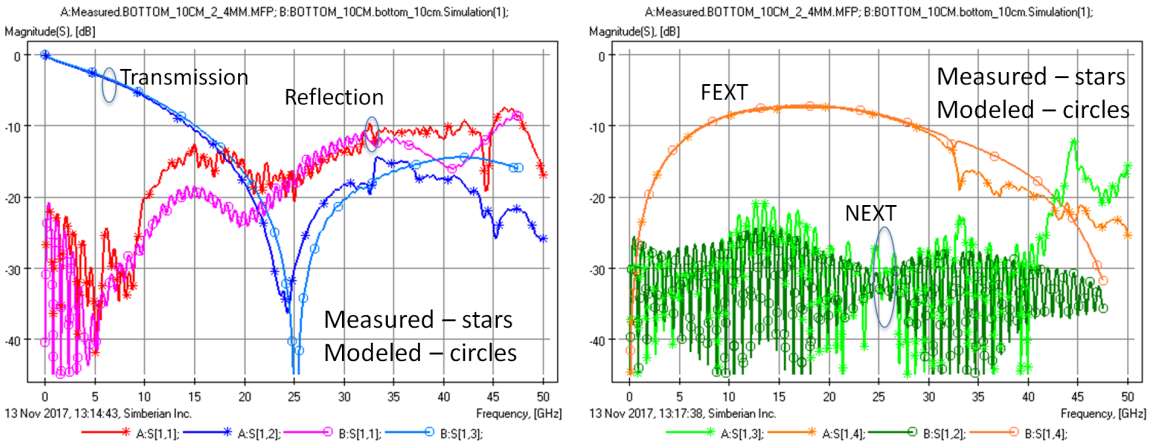

Fig. 7.5. 10 cm diff. microstrip link in layer BOTTOM – measured and modeled magnitudes of single-ended S-parameters.

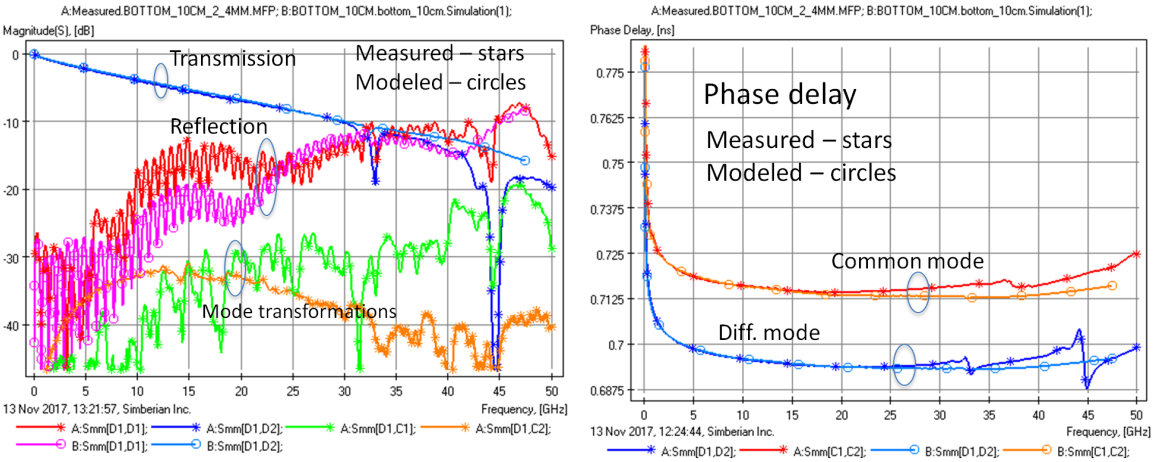

Fig. 7.6. 10 cm diff. microstrip link in layer BOTTOM – measured and modeled mixed-mode S-parameters magnitude (left plot) and phase delay for diff. and common mode transmission parameters (right plot).

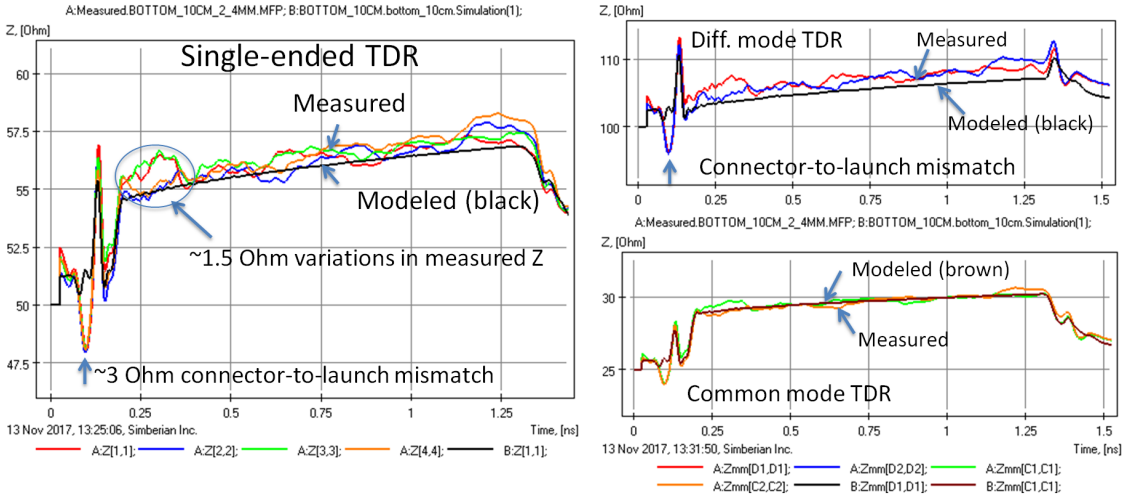

Fig. 7.7. 10 cm diff. microstrip link in layer BOTTOM – single-ended (left plot) and mixed-mode (right plot) measured and modeled TDRs.

Results of validation for the 10 cm microstrip link in layer BOTTOM are shown in Fig. 7.5-7.7. We can observe good correlation of single-ended transmission, FEXT and NEXT up to 30 GHz shown in Fig. 7.5. Though the measured reflection is larger than expected from about 10 to 25 GHz. Similar differential mode reflection mismatch can be observed in Fig. 7.6. The reason is probably the same as in the case of stripline – the mismatch at the connector to launch interface and impedance variation along the traces visible on the TDR plots in Fig. 7.7. The variations on TDR plots also explain the geometrical un-symmetry of the actual link and non-zero modal transformation parameters as the consequence as shown in Fig. 7.6. Note that widths and shape of all microstrip traces and solder mask layer parameters were adjusted as identified in the section 5. Without such adjustments, the measured and modeled impedances are about 3 Ohm off for the single-ended traces and about 6 Ohm off for the differential traces. Amazingly, this difference is within the expected 8% impedance variations (see Fig. 3.1).

To validate the dielectric and conductor roughness models, we can use the Beatty standard. It is a link with 2.5 cm wider strip section in the middle as shown in Fig. 7.8. Measured and modeled magnitudes of S-parameters are shown in Fig. 7.9. It is difficult to see where the resonances in the reflection are – resonance frequencies can be used to validate the dielectric model [1]. If the loss separation technique did not work, the dielectric will have lower or higher losses. That causes different dispersion in the real part of permittivity and shift of the resonances as the consequence. Unfortunately, the resonances in the reflection parameters are not clean with the presence of the connectors and launches. To eliminate the effect of them, we use de-embedding procedure based on the test fixture S-parameter extraction from S-parameters measured for 2 single-ended stripline segments in layer INNER6 and the cross-section model constructed during the material model identification with GMS-parameters in section 6. This de-embedding technique is available in Simbeor software. In this case the de-embedding is possible only up to 30 GHz due to the launch localization issues (see section 8).

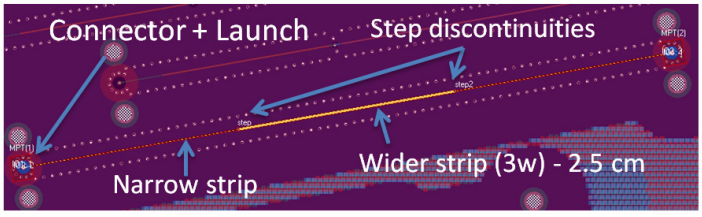

Fig. 7.8. De-compositional analysis of the structure D2 – Beatty strip standard in layer INNER6.

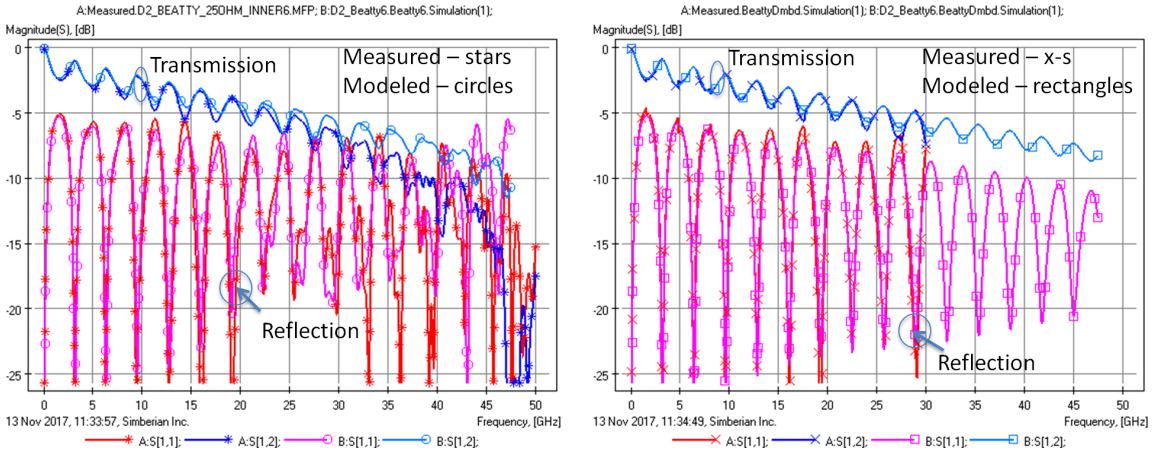

Fig. 7.9. D2 Beatty strip standard in layer INNER6 – measured and modeled magnitudes of S-parameters for complete link (left plot) and for the structure without connectors and launches (de-embedded).

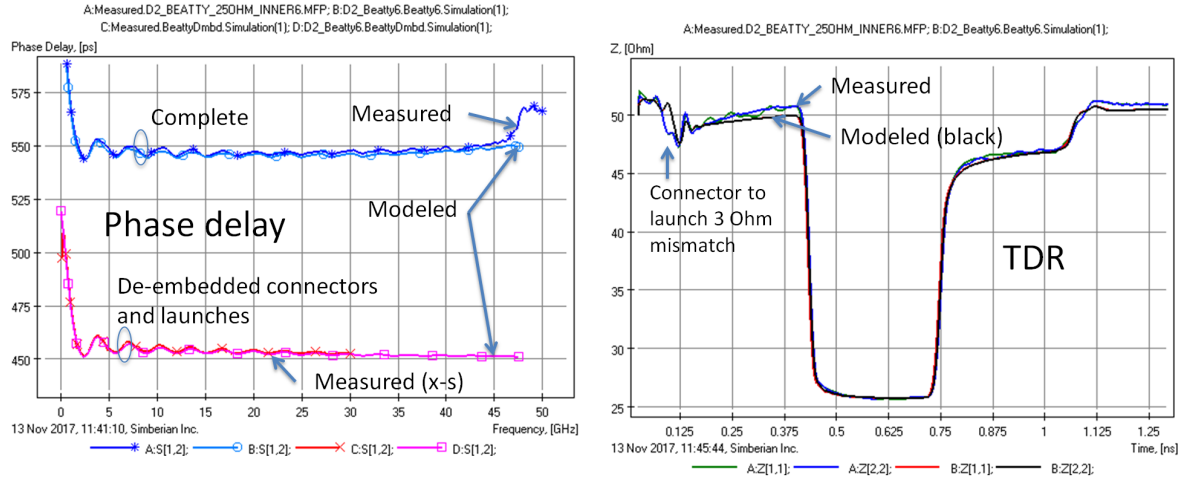

Fig. 7.10. Beatty strip standard in layer INNER6 – transmission phase delay (left plot) for the complete and de-embedded structures and TDR for the complete link (right plot).

De-embedding is done to the boundaries of the launch discontinuity selectors (see Fig. 7.8). The de-embedded results are shown in the right plot of Fig. 7.9 – we can see good correlation in the resonance frequencies and insertion loss. Phase delays for the complete and de-embedded modes are compared in Fig. 7.10 on the left plot. Measured and simulated TDRs of the complete link are shown in Fig. 7.10 on the right plot. Overall we can conclude that the dielectric and conductor roughness models are acceptable for the analysis of the strips within some range of widths.

An example of more realistic link with 2 differential backdrilled vias is the C2 structure shown in Fig. 7.11. This vias were cross-sectioned and the reality was about 30 um longer stubs (accounted in the analysis). This is very close to the expectations, considering the via performance. Measured and modeled single-ended S-parameters are compared in Fig. 7.12. There is visible mismatch in the transmission and reflection above 10 GHz and in FEXT and NEXT above 25-30 GHz. Differential transmission and reflection are shown in Fig. 7.13 on the left plot. The model predicts smaller reflection and transmission from about 10 to 25 GHz. Though, overall the result is acceptable. Differential and common mode phase delay correlate very well up to about 30 GHz as shown in Fig. 7.13 on the right plot. Further investigation with TDR shown in Fig. 7.14 reveals possible source of discrepancies – it is

the same mismatch and the connector to launch boundary and the impedance variation along the microstrips and strips observed in the other cases. Notice that the stripline impedance is more consistent with the expectations (closer to 100 Ohm differential), unlike the microstrip (about 105 Ohm).

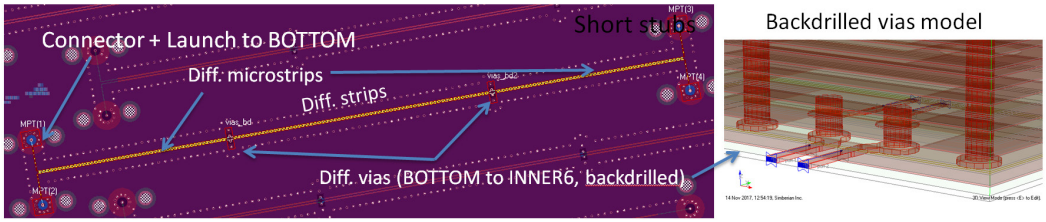

Fig. 7.11. C2 link with 2 backdrilled vias and traces in BOTTOM (microstrips) and INNER6 (strips).

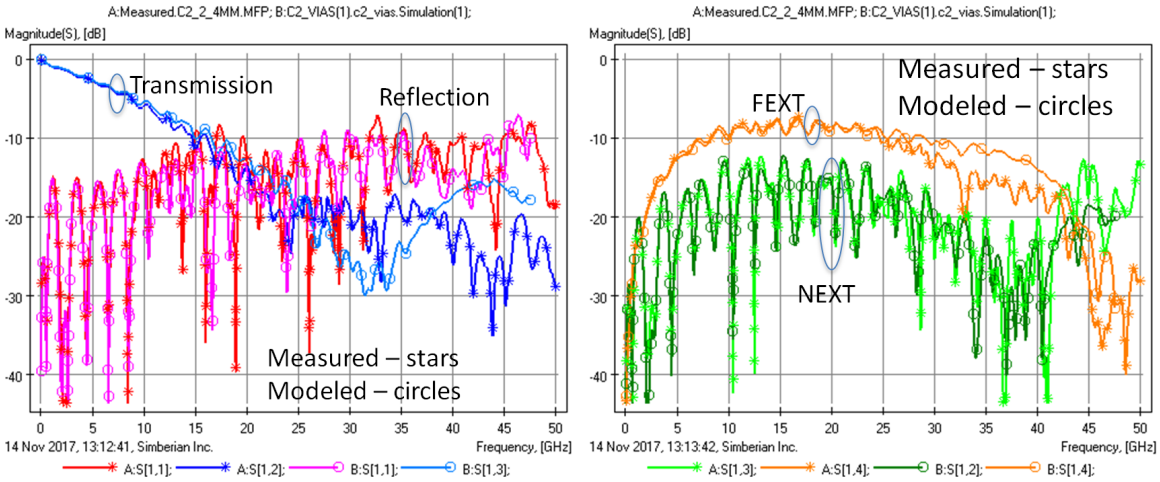

Fig. 7.12. C2 link with 2 backdrilled vias – measured and modeled magnitudes of single-ended S-parameters.

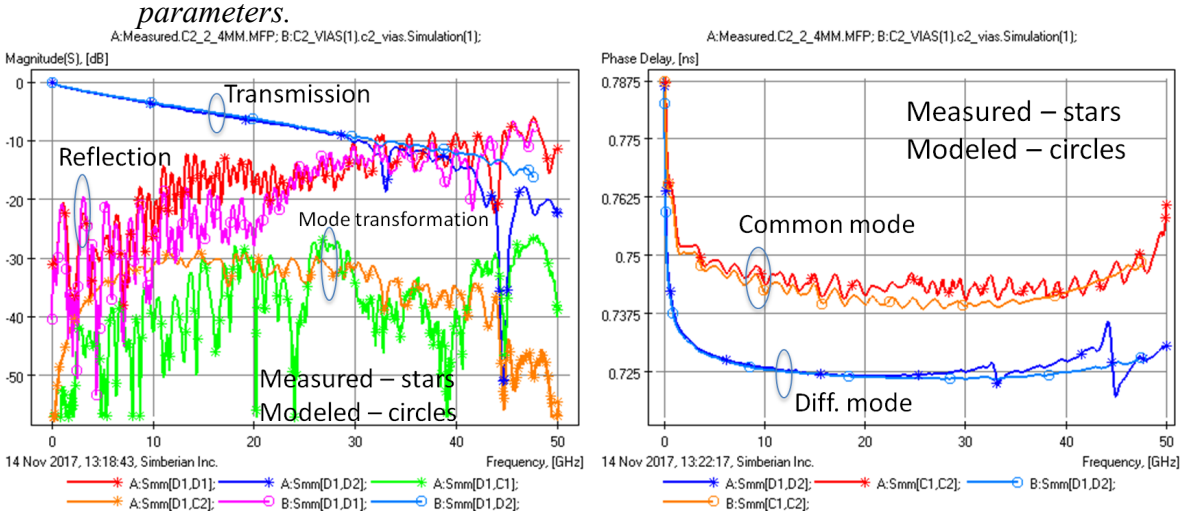

Fig. 7.13. C2 link with 2 backdrilled vias – measured and modeled mixed-mode S-parameters magnitude (left plot) and phase delay for diff. and common mode transmission parameters (right plot).

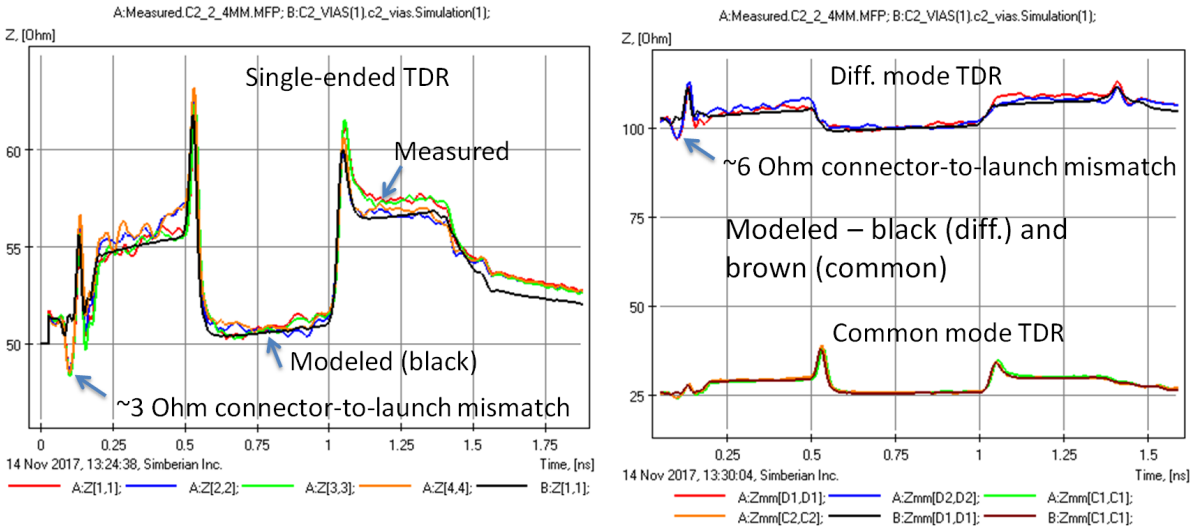

Fig. 7.14. C2 link with 2 backdrilled vias – single-ended (left plot) and mixed-mode (right plot) measured and modeled TDRs.

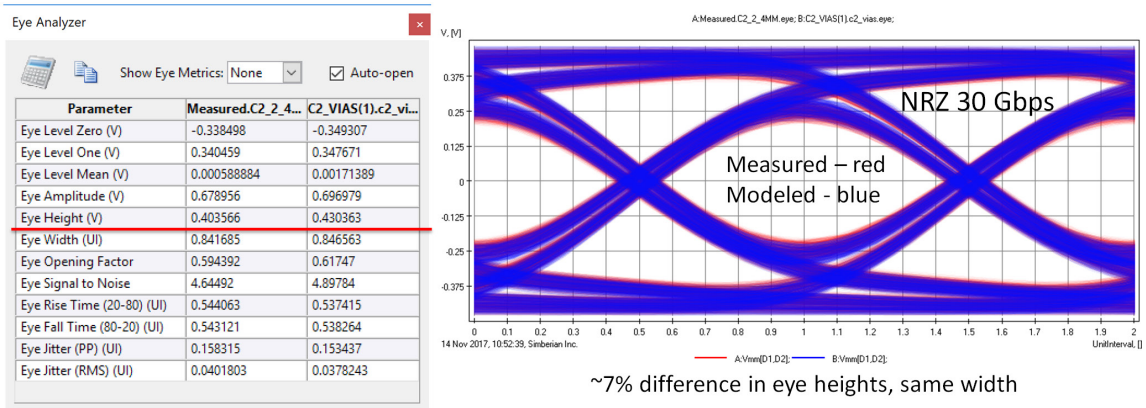

Fig. 7.15. C2 link with 2 backdrilled vias – comparison of measured and modeled eye diagrams for 30 Gbps NRZ signal (no random jitter).

Finally, comparison of the measured and modeled eye diagrams for 30 Gbps NRZ signal without random jitter is shown in Fig. 7.15. Despite all those discrepancies in the reflection and TDRs, unexpected mode transformations and problems above 30 GHz the eyes are very close to each other. Only formal analysis reveals about 7% difference in the vertical opening. The horizontal openings are practically the same. The measured vertical eye opening is smaller due to slightly larger insertion loss at about 15 GHz due to larger reflections (or cut of S-parameters below 70 MHz). These reflections are caused by the connector-to-launch mismatch and the manufacturing impedance variations. With small differences in S-parameters up to 30 GHz, one should expect almost identical eyes. On the other hand, when the measured and modeled eyes are visually different, it usually means big differences in the measured and modeled S-parameters and TDRs. This example shows that the eye comparison is the least informative metric. Though, it is practically important to gain the confidence in the approach. Thus we do it only for some test structures. Comparisons and observations for all other structures on the validation board are provided in the complete report [9]. In conclusion to this section, we can state that the models obtained following the formal procedure have accuracy acceptable up to about 30 GHz that is sufficient for the analysis of PCB links for 30 Gbps NRZ signals.

8. Reality above 30 GHz (complimentary)

Investigation of measured S-parameters above 30 GHz may be the most interesting part of this project. The first peculiarity observed in the measured insertion loss for the straight traces was the resonances around 33 GHz as shown in Fig. 8.1. The resonances were observed in S-parameters measured with TDNA and all VNAs. It is known that the fiber weave effect may cause the resonances due to periodic loading of the traces. In this case we should observe the reflections at the same frequency – periodic changes of the impedance should reflect energy. In this case, we did not observe peaks in the reflection parameters as shown in Fig. 8.1 on the right plot. So the fiber weave effect was ruled out. When we have looked at the near end and far end crosstalk parameters (NEXT and FEXT), we have observed matching peaks as shown in Fig. 8.2. A de-compositional model of the links with separate models for launches and transmission lines did not predict this coupling. Though, the electromagnetic analysis of the launch showed that the energy leaks at the launches of the wider gaps between the vias as illustrated in Fig. 8.3 at 33 GHz.

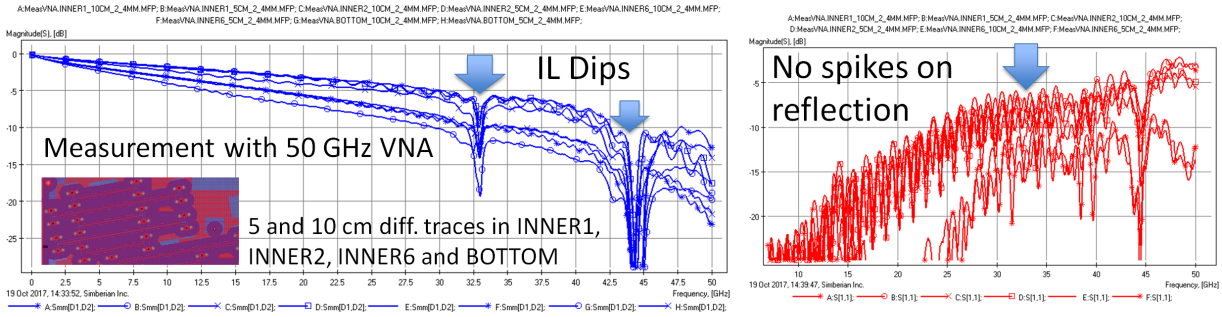

Fig. 8.1. Differential insertion loss (left plot) and reflection loss (right plot) for 3 differential links.

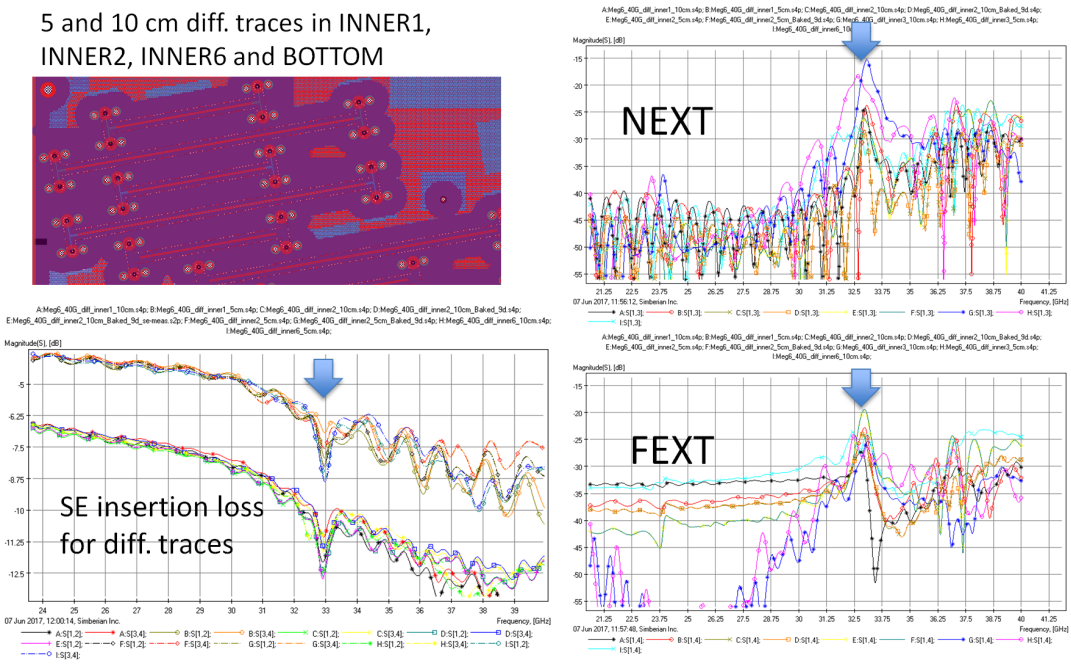

Fig. 8.2. Single ended insertion loss (left bottom plot) and near end crosstalk (NEXT, right top plot) and far end crosstalk (FEXT) for 3 differential links.

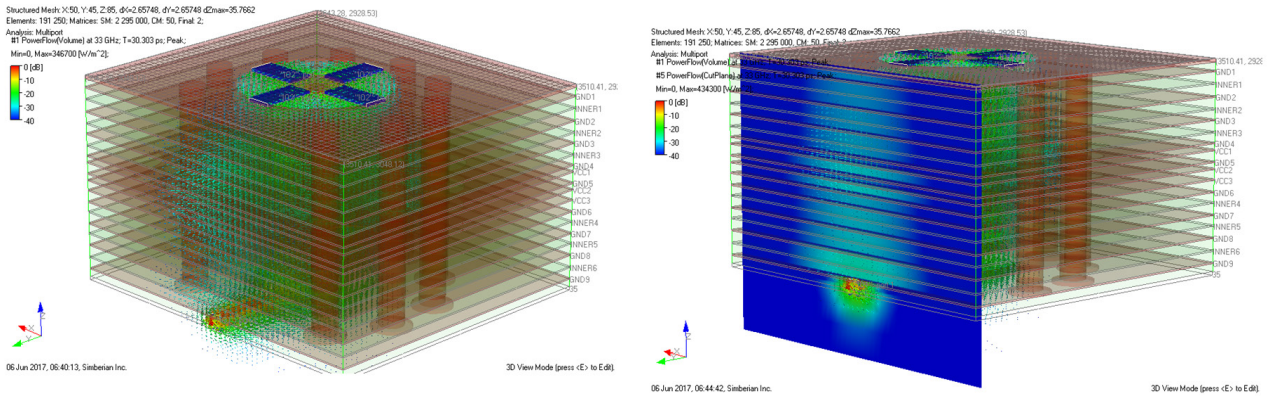

Fig. 8.3. Instantaneous power flow density at the microstrip launch at 33 GHz. The electromagnetic field is confined by the closely spaced stitching vias but "leaks" through the wider gap between the vias at the strip side.

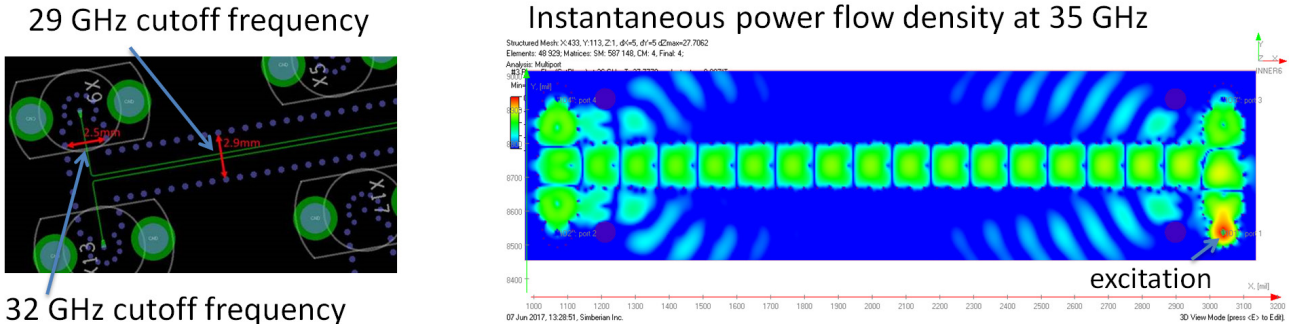

Fig. 8.4. Stitching vias along the traces form waveguides with the cutoff frequencies 29 and 32 GHz. Waves can propagate in such waveguides at any stackup layer as illustrated on the right.

The energy simply leaks into the substrate integrated waveguides (SIW) formed by rows of the stitching vias along the traces, propagates along the waveguide and can be transferred to all other ports in the structure. Every plane pair in this configuration forms the SIW and transmits the waves in addition to the stripline or microstrip lines. Pairs with larger distance transmit more energy (wave attenuation is smaller for planes with larger distance). The analysis of this effect requires analysis of the link as a whole – this is time consuming, but not necessary. We can simply predict such behavior with the analysis of the launch and evaluation of the cutoff frequency for the SIW.

Note that the striplines are waveguides with two reference planes and the **equipotentiality must always be enforced** with stitching vias, to have predictable behavior at the microwave frequencies. To extend the frequency range of the interconnects up to 40-50 GHz, here are some recommendations:

- Launch return vias should be closer to the signal via – the distance between the vias can be used to evaluate the upper localization frequency.
- Gaps between the stitching vias on the strip side should be as small as possible.
- Stitching vias along the strips should be closer to the strip – cutoff frequency of SIW can be used to compute this distance and the effect of the vias should be evaluated, to avoid the periodic loading.

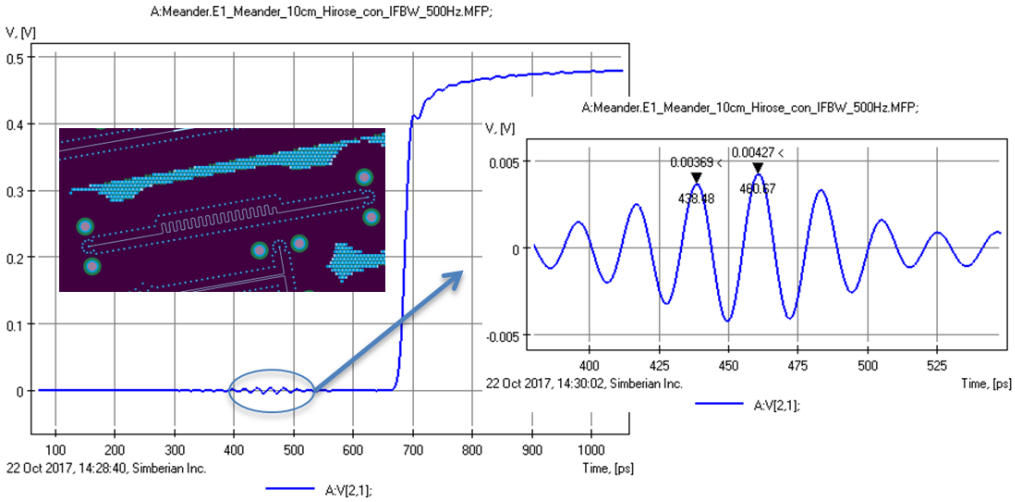

Fig. 8.4. Ripples in the TDT response of the meandering stripline in layer INNER6.

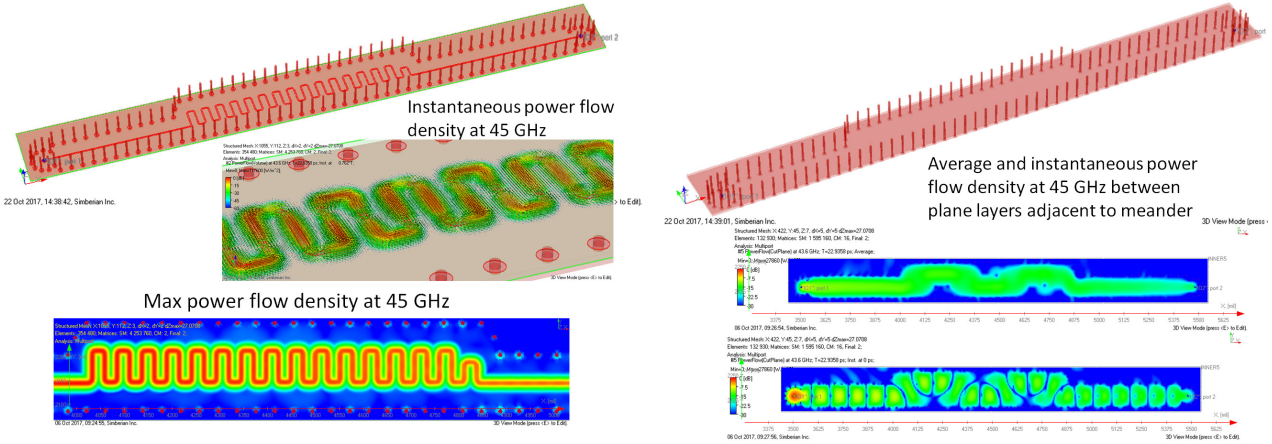

Fig. 8.5. Instantaneous power flow density in the meandering stripline (left) – power flows along the traces and along the SIW formed by stitching vias (right).

Another peculiarity observed in the measurements was the ripples in the TDT response for the meandering stripline as shown in Fig. 8.4. It looks like a non-causality at the first glance, but it is actually the multipath propagation phenomenon caused by the "leaks" from the launches and energy transmission through the SIW formed by the solid planes and rows of stitching vias as illustrated in Fig. 8.5. The power propagates along the strips and also along the SIW as visible on the left and right plots in Fig. 8.5.

Finally, coupling between the ports in two different stripline links in layer INNER6 was measured as shown in Fig. 8.6 Ideally, the coupling should be zero, but in reality it is below -70 dB up to 25-27 GHz and grow at higher frequencies. To reduce such coupling, more stitching vias should be placed between the structures and all over the board. Note that this is applicable not only for the stripline reference planes, but to all parallel plane structures – the energy can be transferred between any pair of planes.

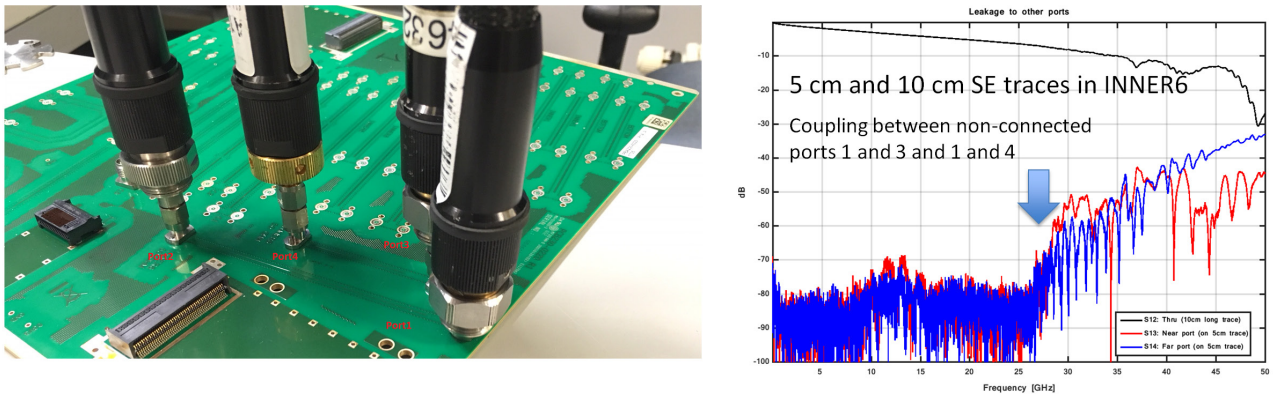

Fig. 8.6. Measurement setup to evaluate coupling between ports in two different stripline links (left) and coupling parameters (right plot).

9. Conclusion

"Sink or swim" validation process [3] has been successfully used in this "practical" analysis-to-measurement validation project. So far, the acceptable analysis-to-measurement correlation has been reached up to 30 GHz on the most of the structures. Technically, this is sufficient for the reliable analysis of 28-32 Gbps links. Design of launches and reference plane stitching localization degraded the correlation above 30 GHz. These effects are difficult to simulate and to predict even for simple validation boards. Also, the reality is that the accurate prediction of PCB behavior at the millimeter bandwidth up to 40-50 GHz with the typical trace width and low-cost manufacturing process with large geometry variations is very ambitious goal and maybe not even possible. It would be practically impossible to include all those variations in the analysis because of lack of the statistical distributions of the board geometry and material parameters. In addition to the statistical manufacturing variations, considerable differences in the microstrip trace geometry have been discovered during cross-sectioning. The bottom line – do not expect excellent analysis to measurement correlation with the low cost manufacturing processes and without cross-sectioning of the board! To extend the predictability up to 40-50 GHz, manufacturing tolerances should be substantially reduced, or trace widths increased and more homogeneous dielectrics used (or all of the above). The specificity of the signal integrity problems also dictates very strict requirements for the measurement equipment – accuracy at low and high frequencies is equally important. The reality is that not all measurement equipment satisfies such requirements and this not the common knowledge. Anyone with plans to purchase the equipment (or EDA tools) should try it first without regards to the vendor profile and have software or an expert in the team to evaluate S-parameters quality and validity. The validation boards are the excellent tool to do that. The measurement and EDA tools may be very expensive and not as accurate as claimed by the vendors. The selection of the measurement equipment and components caused substantial delay in this project. Here are some other practical observations from the project:

- Identified dielectric parameters are very close to the vendor specs.
- Conductor roughness is the major contributor to the signal degradation – analysis without proper conductor roughness models is useless.
- Causal Huray-Bracken conductor roughness model provided good correlation in the losses and in the TDR impedance.
- Cross-sectioning revealed that the stripline traces are very close to the adjusted trace geometry provided by manufacturer, however, the microstrip cross-sections are very different.

- Measurements should be planned in advance to have all matching parts (cables/connectors).
- Layout needs careful inspection before and after the manufacturing.
- Naming for stackup & nets should be consistent through the whole design/manufacturing cycle.
- To simplify comparisons, port numeration should be consistent in models and measurements.

In conclusion we should state that this is an ongoing project and we keep investigating obtained data in preparation for the next validation board. We expect it will be actually predictable up to 40 GHz.

Acknowledgments

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