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Design of optimal differential viaholes for 6-plane board



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Introduction

- Via-hole transitions are the major contributors to signal degradation in multi-gigabit data channels
- Geometry of the via-holes have to be optimized to minimize the reflection and to maximize the transition of the differential signal
- This example shows
 - How to use Simbeor 2007 to create optimal via-holes for 10 Gbps channel and
 - How to generate 3D full-wave S-parameter models and use it in the system-level analysis



Differential via-holes design example

- Stackup with 6 plane layers
- Drill diameter is 8 mil, differential traces are 6 mil wide 10 mil apart
- Goal is to design differential through-vias from Signal1 to Signal2

Solution: "OptimalDifVias" PCB6P စိုင္ကို Materials StackUp: LU=[mil], NL=15, T=86.2 1| Signal: "Signal1", T=1.4, Ins="FR4" 2| Medium: T=10, Ins="FR4" 3| Plane: "Plane1", Mat="Copper", T=1.4, Ins="FR4" 4| Medium: T=11, Ins="FR4" 5| Plane: "Plane2", Mat="Copper", T=1.4, Ins="FR4" 6| Medium: T=11, Ins="FR4" 7| Plane: "Plane3", Mat="Copper", T=1.4, Ins="FR4" 8| Medium: T=11, Ins="FR4" 9| Plane: "Plane4", Mat="Copper", T=1.4, Ins="FR4" 10| Medium: T=11, Ins="FR4" 11| Plane: "Plane5", Mat="Copper", T=1.4, Ins="FR4" 12| Medium: T=11, Ins="FR4" 13| Plane: "Plane6", Mat="Copper", T=1.4, Ins="FR4" 14| Medium: T=10, Ins="FR4" 🚥 15| Signal: "Signal2", T=1.4, Ins="FR4"

- Steps:
 - Create and optimize via-holes geometry for differential mode only (using lumped ports) by minimizing |S11| for 100-Ohm normalized S-parameters
 - 2. Add transition to differential transmission line and generate final model for the system-level analysis



Geometry synthesis and electromagnetic analysis with Simbeor 2007



Simulation in time domain with system-level simulator HyperLynx 7.7 with Eldo





Comparison of reflection in time-domain



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Comparison of transmission in time-domain



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Final via-holes design and 4-port model



Reflection and transmission of differential mode in time domain





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Not optimal via-holes can significantly degrade the signal



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10-mil vias are 24 mil apart with 24 mil anti-pads and 16 mil pads in all layers, traces are 6 mil wide 10 mil apart

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Pads in plane layers increase the capacitance and decrease the effective impedance of vias to 60 Ohm

Conclusion

- Geometry of differential via-holes have to be optimized to have reflection for differential mode at least below -25 dB
 - Simbeor 2007 via-holes creation wizard allows to synthesize "impedance-controlled" vias without long electromagnetic optimization
- Even optimal vias require 3D full-wave S-parameters models for the system-level analysis of a complete channel (small reflections can cause system-level resonances)
- Non-optimal via-holes can cause significant degradation of 10 Gbps signal and even malfunction of the complete channel
- Generated with a 3D full-wave solver localized models without stitching vias are valid only in case of small or no common mode at the via-hole transition
 - Vias stitching the top and bottom reference planes have to be added to create accurate localized model that includes the common mode
 - Common mode analysis without stitching vias requires a hybrid systemlevel model with all planes and decoupling structures)



Solutions and contact

Solution files and HyperLynx schematic files are available for download from the simberian web site

http://www.simberian.com/AppNotes/Solutions/OptimalDifViaholesDesign6pPCB_2007_08.zip

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