Life beyond 10 Gbps: Localize or Fail!

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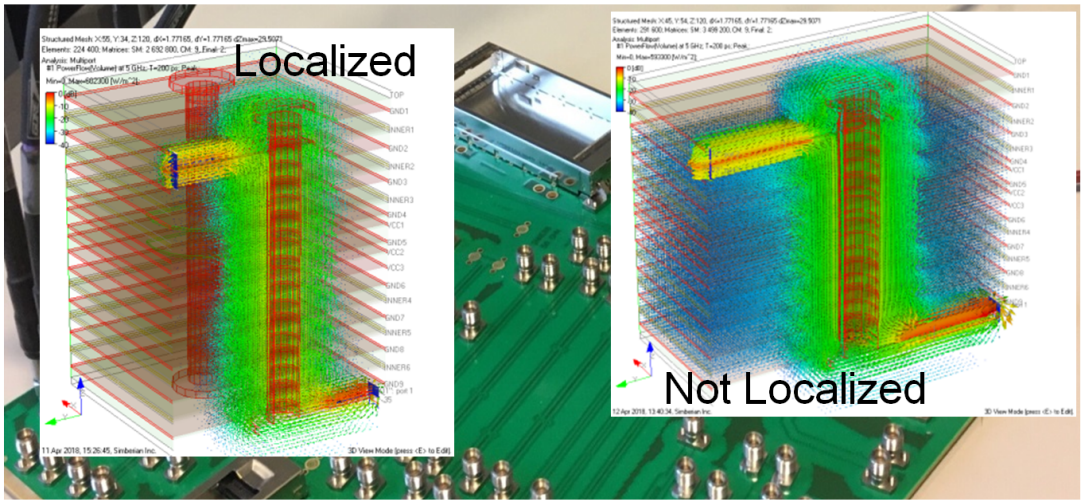
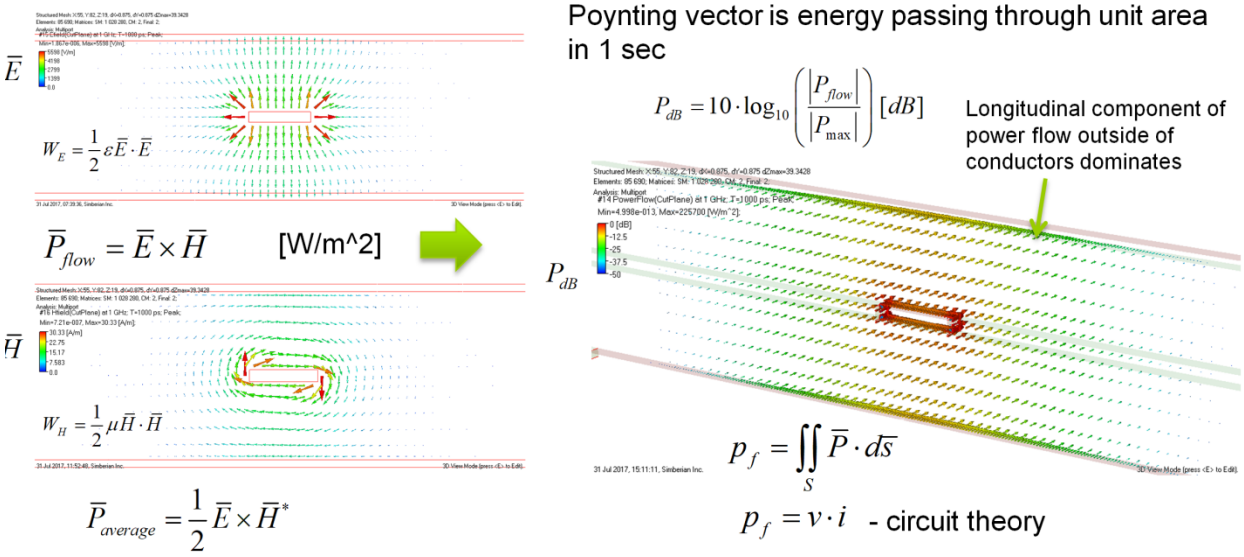


What does it take to design predictable PCB or packaging interconnects operating at tens of Gbps? Properly identified dielectric and conductor roughness models, known manufacturer geometry adjustments, properly validated simulation tools – those are necessary conditions. **One of the sufficient conditions is the localization property – to be predictable, all elements of an interconnect link must be localized up to a target frequency!** This article introduces and illustrates the localization concept with the power flow density computed with unique Trefftz finite element solver available in Simbeor THz software.

Ideally, all interconnects should look like uniform transmission lines (or waveguiding structures) with the specified characteristic impedance. In reality, an interconnect link is typically composed with transmission lines of different types (micro-strip, strip, coplanar, coaxial, etc.) and transitions between them such as vias, connectors, breakouts and so on. Transmission lines may be coupled to each other that cause crosstalk. The transitions may reflect and radiate energy due to discontinuities in signal and reference conductors. The crosstalk, reflections and radiation cause unwanted and sometime unpredictable signal degradation. **If analysis of traces or viahole transitions is possible in isolation from the rest of the board up to a target frequency, the structure is called localized** (see more at app notes #2009_05 and #2013_05 at http://www.simberian.com/AppNotes.php). Structures with the behavior dependent on the other structures and on board geometry are called not localized and should not be used in multi-gigabit interconnects in general. Examples of non-localized structures are coupled traces, strip lines with not connected reference planes, traces crossing gaps in reference planes, vias with far, no or insufficient number of stitching vias (vias connecting reference planes of the connected traces). Analysis of non-localized structures is usually possible only at the post-layout stage with substantial model simplifications that degrade accuracy at higher frequencies. **To design predictable interconnects, only localized structures must be used– this is one of the most important elements for design success.** The localization is always bandwidth limited for strip

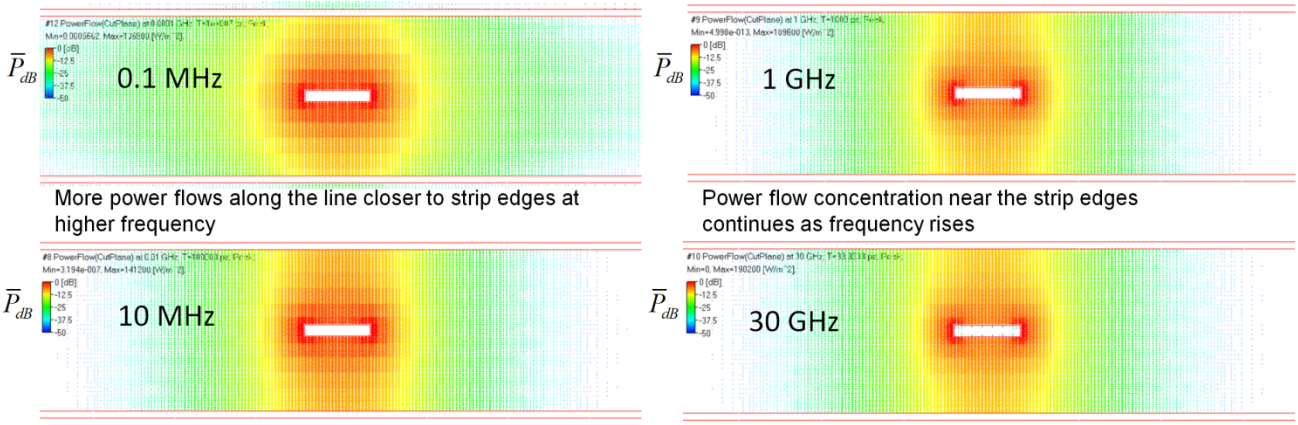
lines (two reference conductors) and for vias (two or more reference conductors). **How to estimate the localization property of a transition?** One way is to run electromagnetic analysis of the structure with different boundary conditions or simply change simulation area size without changing phase reference planes and evaluate the differences in the computed S-parameters - if the difference is small, the structure may be considered localized and suitable for final design (see more at app note #2013_05 at http://www.simberian.com/AppNotes.php). **Alternatively, compute and plot power flow density and literally see the localization of the signal in space as illustrated here.**

First, let's get familiar with the power flow density concept using a simple example and analogy with the circuit theory for a strip line structure:



Voltage in the circuit theory corresponds to the modal electric field intensity E, current corresponds to the modal magnetic field intensity H. Cross-product of the electric field and magnetic field intensities is the vector of power flow density (or Poynting vector), measured in Watt/m^2. It is energy through unit area in space transferred in 1 sec. When we look at the power flow density vectors, we basically see where the energy of the signal is located in space around a trace or via-hole. Total power through a cross section of the strip line corresponds to the power flow in corresponding transmission line model, equal to product of the voltage and current. To understand the localization concept, it is very important to know that the signal energy is actually distributed in space around each element of interconnect structure. For instance, the power flow

density of the dominant quasi-TEM mode in strip line is shown below at 4 frequencies:

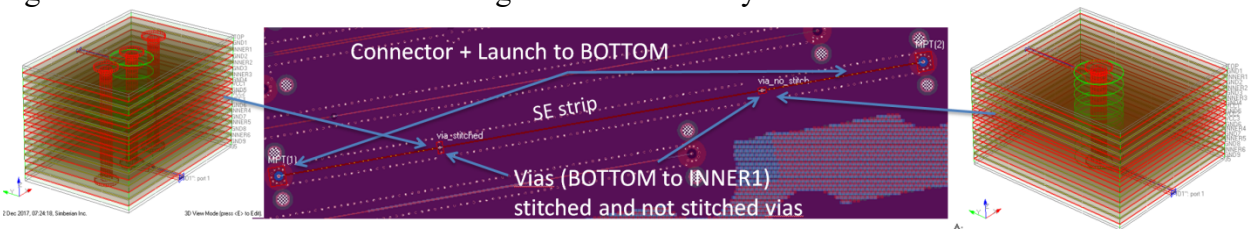


The strip is 1.2 mil thick, 7 mil wide trace, in homogeneous dielectric with Dk=3.76, LT = 0.006 @ 1 GHz, planes 0.77 mil thick and 17.2 mil apart, 1 V excitation and 50 Ohm terminators.

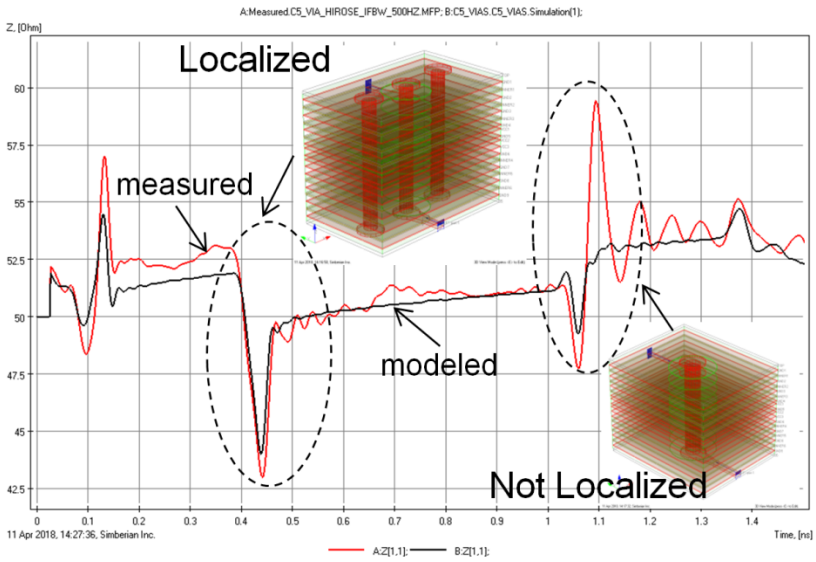
The power flow density is depicted by vectors with the direction along the t-line (into the picture) outside of the conductors. The value of the vectors is expressed with color scale in dB from zero (red color) to -60 dB (blue color). The power flow drop by 0.5 corresponds to -3 dB, by 0.1 to -10 dB, by 0.01 to -20 dB and so on. We can observe that the maximal power density is uniform around the strip at lower frequencies and concentrates around the strip edges at higher frequencies. As we can also see, the power of the signal drops around the strip rather quickly to -50 dB (by 0.00001 times). **We can say that the structure is well localized if there is nothing in the area with the significant power flow (no coupling to the other strips for instance).** However, the localization is conditional on homogeneity of dielectric and uniformity of the strips. If such conditions are not satisfied (and they are usually not satisfied for PCB interconnects – dielectrics are not homogeneous and there are large variations in manufacturing), the energy of the quasi-TEM mode can be transformed into the dominant TEM wave of the parallel plate waveguide formed by the top and bottom plane. To avoid it, the stitching vias connecting the planes should be used along the traces at higher frequencies. The distance between the stitching vias should be less than half of wavelength in dielectric at the highest frequency of interest – that may be a lot of additional vias. **The strip line localization can be easily violated if the equipotentiality of the reference planes is not ensured with the stitching vias.** The result is the signal energy leak along the trace (can be observed on TDR as flat or decreasing impedance). Due to the reciprocity it works both ways – the energy of the power distribution network can be coupled to the trace, if it is not localized with the stitching vias.

Now let's take a look at the power flow density in via-holes. One of the links on EvR-1 board was designed by Marko Marin with two single-ended vias specifically to test the localization importance. One of the vias have two stitching vias at about 30 mil distance from the

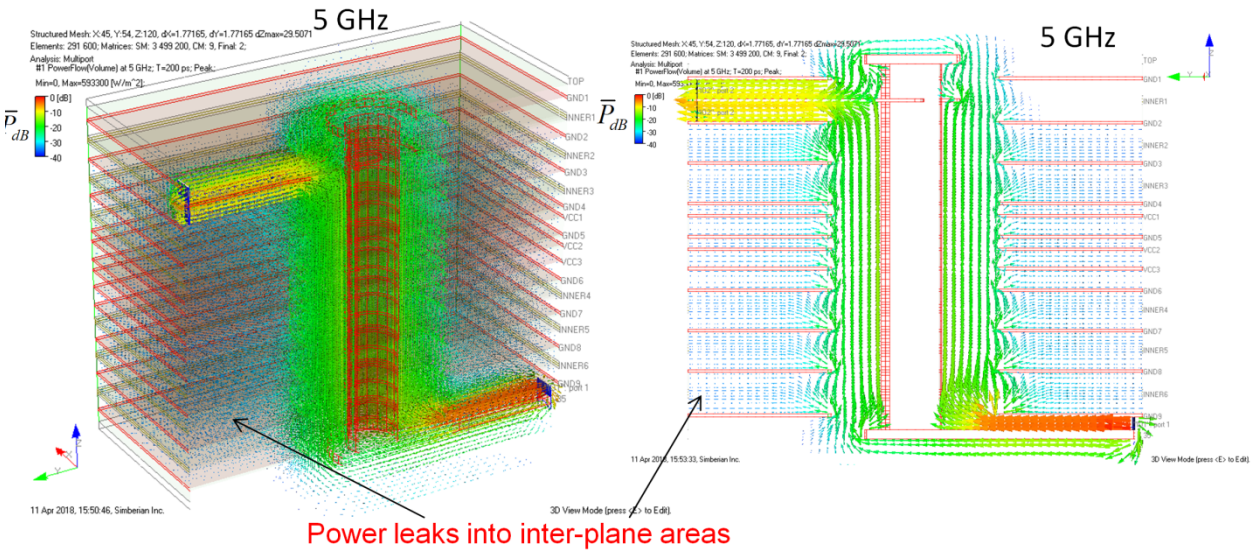
signal via and another have no stitching vias in the vicinity as shown below:



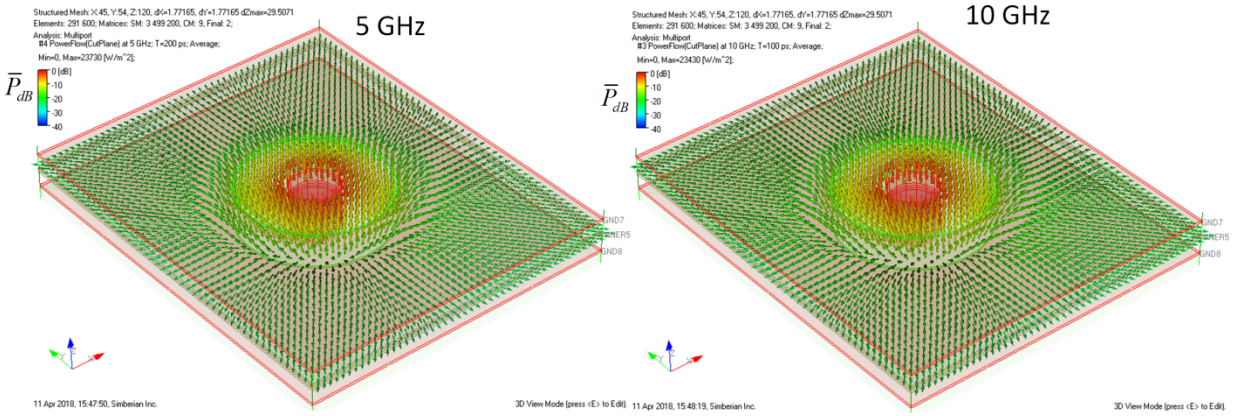
This is example from our award-winning DesignCon2018 paper M. Marin, Y. Shlepnev "40 GHz PCB Interconnect Validation: Expectations vs. Reality" - the paper with all details and complete report are available at [the Simberian web site.](#) We used the "sink or swim" formula for predictable interconnect design that is based on tree components: **interconnect geometry adjustments + identified material models + validated software -> predictable interconnects**. With all three components in place, we were able to reliably predict behavior of most of the interconnect structures on EvR-1 board without additional tuning or calibration for 28-30 Gbps NRZ signal. However, the analysis to measurement correlation was acceptable only up to about 5 GHz for the structure with the non-localized via shown above. It makes it predictable for signals with only about 3-5 Gbps data rate. TDR plot shown below reveals the large discrepancies in the measurements and the model at the location of the single via without the stitching vias. We can see some oscillations at the via location – it means that the via is coupled to a resonating cavity formed by parallel planes and multiple distant vias around the traces.



To see how the coupling happens, let's use the power flow density visualization. The 1 V signal source is connected to the microstrip line port at the bottom of the board. Both microstrip and strip line ports are terminated with 50 Ohm. As we can see, the power from the microstrip line at the bottom does not go all the way to the strip line in the layer INNER1 – some energy is radiated into the inter-plane areas as shown below for 5 GHz (peak values of the power flow density):

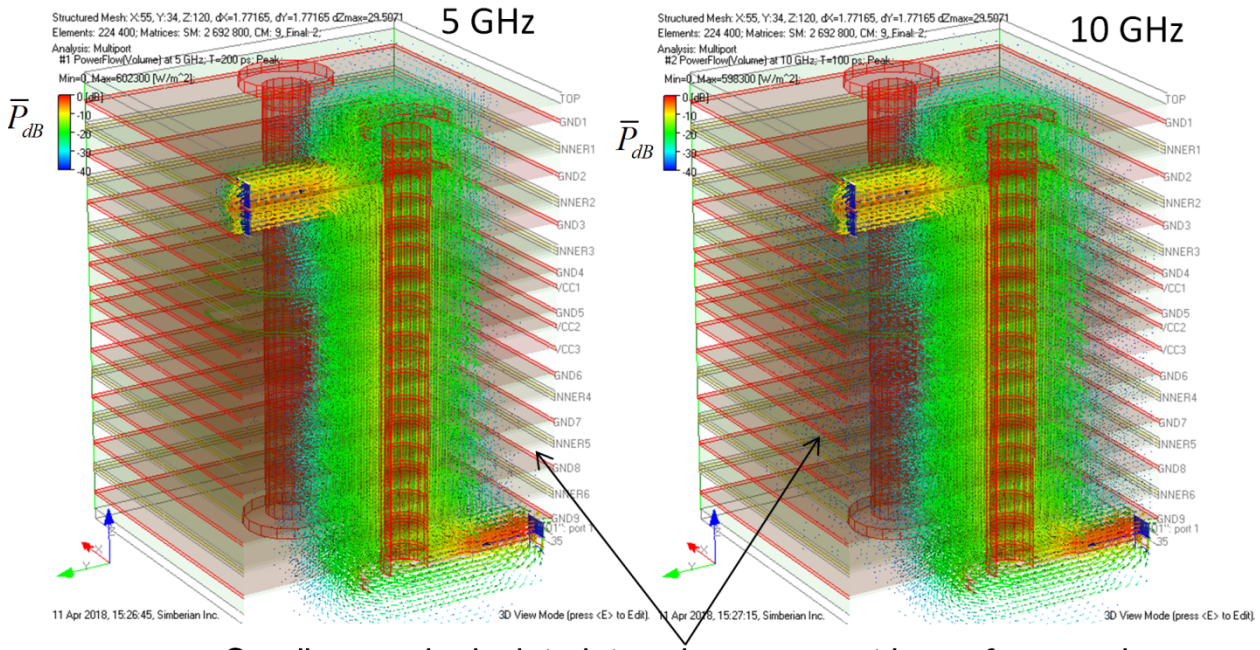


This model uses absorbing boundary conditions on the outside boundaries of the simulation domain – it absorbs the energy of the parallel plane waves going from the via. For instance, here is the close up of what is going on between the reference planes GND7 and GND8 – the power flows along the via in the anti-pad area and flows mostly outward between the parallel planes and is absorbed at the outer boundary:

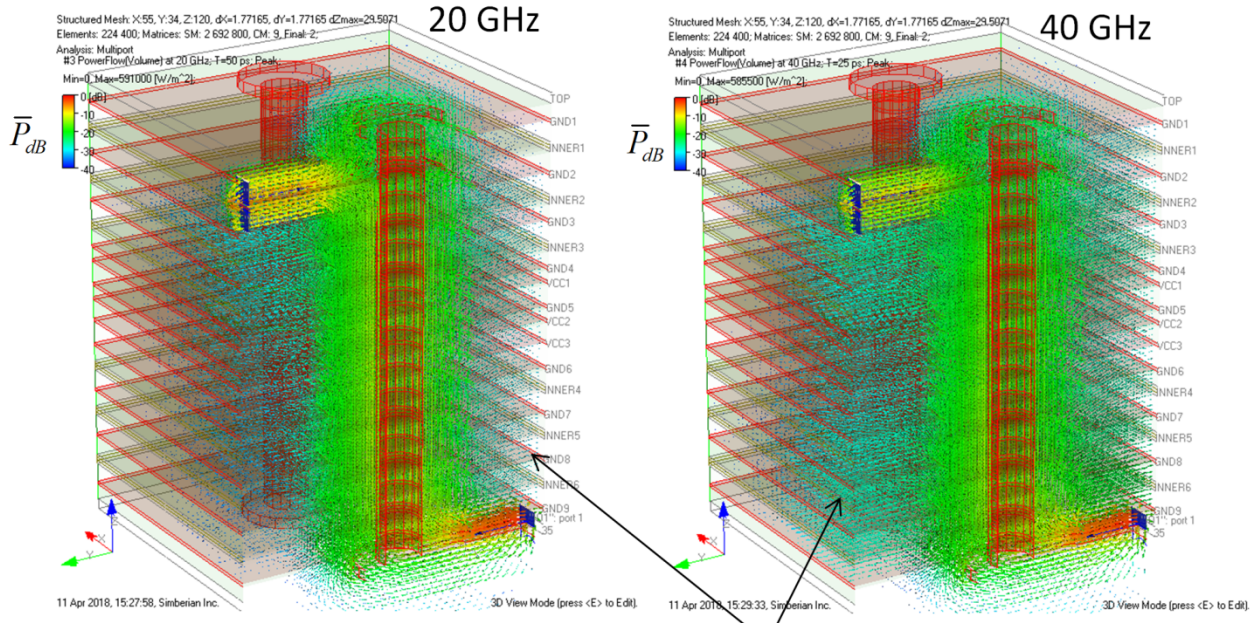


In reality, the energy injected into the inter-plane area does not completely disappear – it may be reflected from the fences formed by vias and returned back to the signal via in form of the oscillations observed on TDR above (coupled to cavities formed by distant stitching vias). Behavior of such vias can be predicted only in the post-layout analysis with either huge computational cost (large simulation area) or with simplified models of the whole board with substantial model accuracy degradation. **The easier alternative is to localize it!**

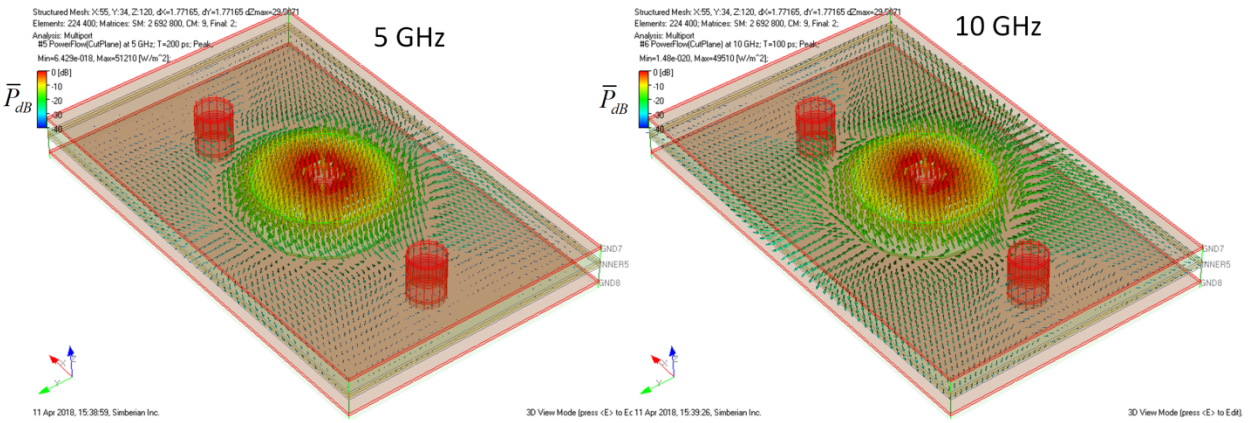
The second via in this link was designed to see how effective would be 2 stitching vias placed at about 30 mil from the signal via. The TDR correlation for this via is acceptable, let's see how the power propagates along that structure at different frequencies:



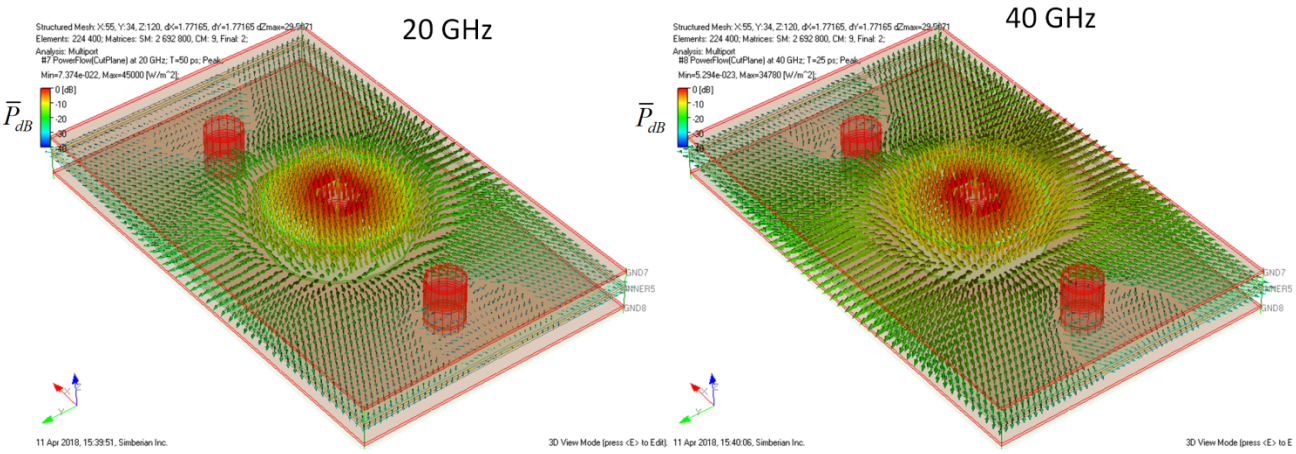
Small power leaks into inter-plane areas at lower frequencies



Power leaks into inter-plane areas increases with the frequency

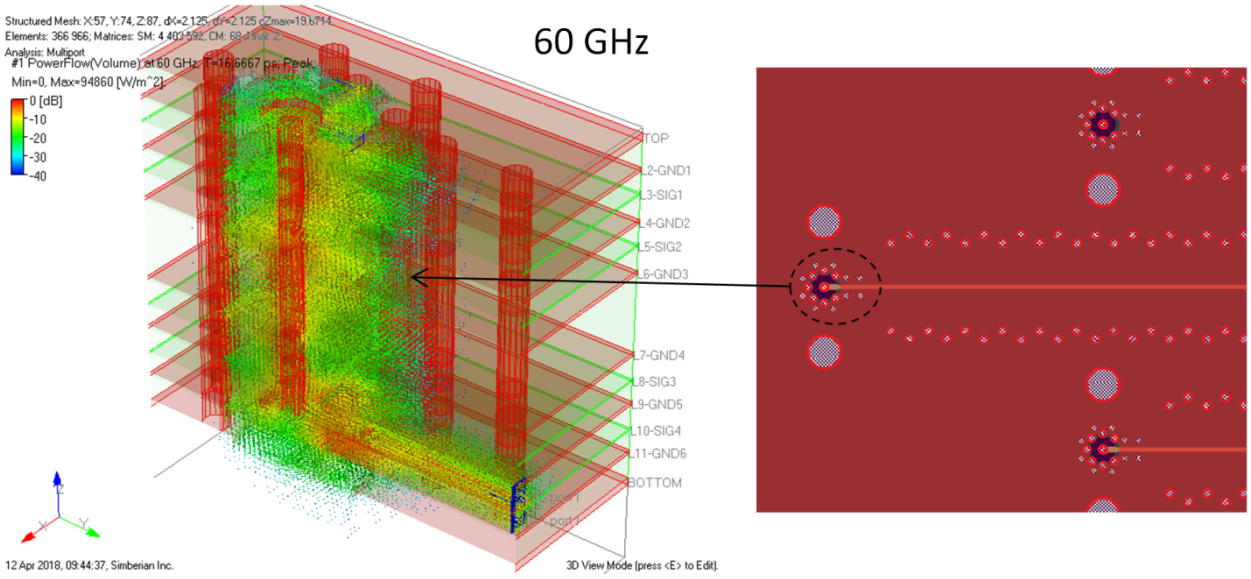


Small power leaks into inter-plane areas at lower frequencies (stitching vias work)



Larger power leaks into inter-plane areas at higher frequencies (stitching vias are not so effective)

What a difference just 2 properly designed stitching vias make! The localization bandwidth of the single via is extended to 15-20 GHz. The localization degrades progressively starting from about 20 GHz in this case – it means that this via becomes coupled to the parallel plane structures with all the unpredictability consequences as we observed for the single via. What if we want to extend the frequency range further up to 50-60 GHz? That is very difficult task for the single-ended through vias in general. Just take a closer look at an example of the single via launch localized up to about 60 GHz with 17 stitching vias as shown below:



This via transition was designed by Scott McMorrow for one of our material model identification projects reported in D. Dunham, J. Lee, S. McMorrow, Y. Shlepnev, 2.4mm Design / Optimization with 50 GHz Material Characterization, DesignCon2011. It is also featured in demo-video #2018_01 at http://www.simberian.com/ScreenCasts.php (demo-videos #2016_01 and #2018_01 use power flow density to illustrate the effect of the stitching via number and positioning).

The bottom line is that the possibility to simulate a link in isolation from the rest of the board or localization is probably the most important condition to design predictable interconnects. Only structures with behavior predictable up to a target frequency should be used to design links for tens of Gbps data rate. The closeness of the stitching vias should be measured relative to the wavelength – the stitching vias can be considered close as long as the distance does not exceed quarter of the wavelength at the target frequency. The number of the stitching vias also matter. Without the localization, the interconnects cannot be accurately simulated in most of the practical cases. **If interconnect behavior cannot be predicted, the outcome is uncertain - it may work or may fail!**