How Interconnects Work: Bandwidth for Modeling and Measurements

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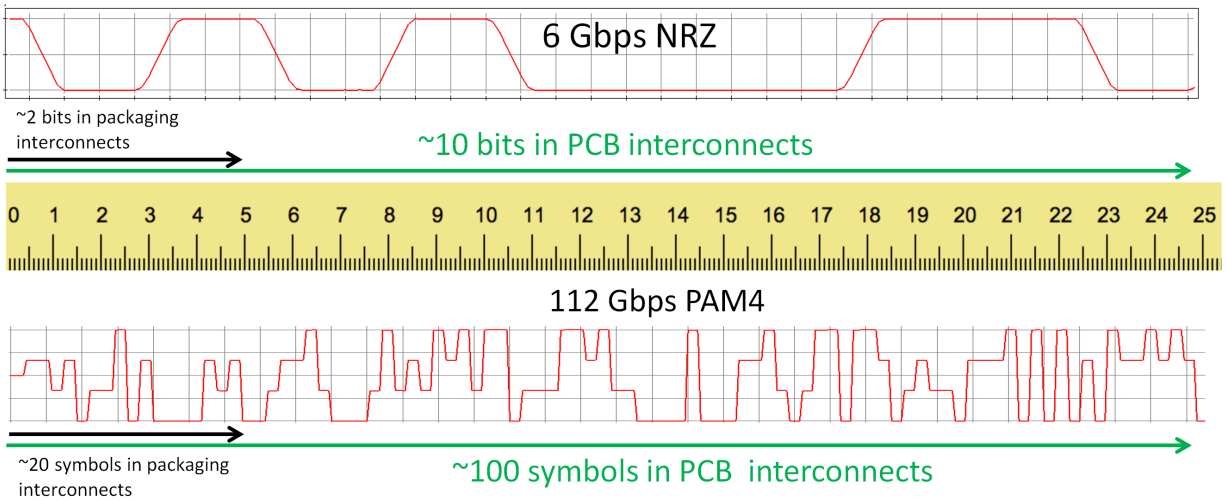
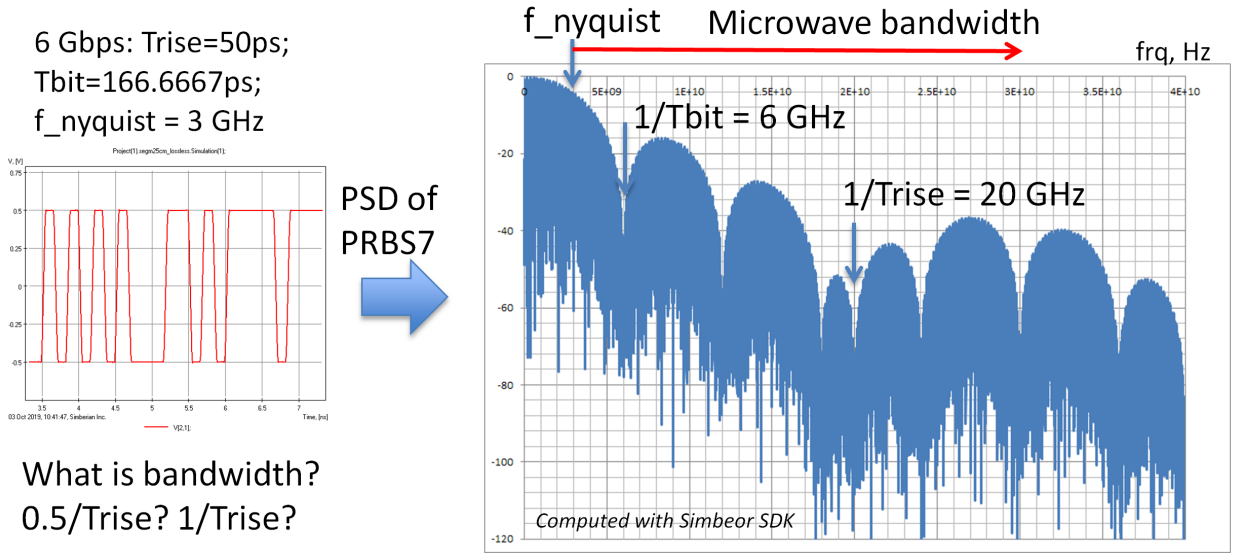
What does it take to design predictable PCB/packaging interconnects operating at 6-112 Gbps? Design interconnects that will behave as expected? Can we use design processes and practices adopted at lower data rates? For instance, can we apply approaches that worked well at 1-3 Gbps for design of interconnects operating at 10-30 Gpbs? Can we achieve the first pass design success at such data rates and, if so, what does it take to do it? What signal degradation factors have to be accurately predicted and at which data rate they become important? We have recently tried to answer those questions at tutorial at DesignCon 2020 [1]. This article is loosely based on the material prepared for the tutorial and addresses the issue of frequency bandwidth required for the analysis and measurements for PCB or packaging interconnects operating at 6-112 Gbps.

Digital signal in a serial link is a sequence of bits transmitted through PCB or packaging interconnects as sequence of pulses modulated by amplitude. The digital interconnect modeling problem is actually the analog problem of modeling propagation of pulses in time domain. Most often a simple two-level pulse amplitude modulation (PAM2) is used. Lower voltage level corresponds to 0 and higher level to 1. Also, because of pulse amplitude does not return to zero, PAM2 is often called non-return-to-zero (NRZ). To transmit data with speed 6 Gbps (Gigabit per second) with NRZ or PAM2 modulation, one bit time should be 166.6667 ps. In space it spreads over about 2.5 cm (about 1 inch) in PCB type dielectric (Dk=4). Four-level pulse amplitude modulation (PAM4) is becoming more popular as the data rates increase and the required link bandwidth for PAM4 is smaller [2]. It uses 4 voltage levels to encode sequences of 2 bits 00, 01, 10 and 11 called symbols. It is also non-return-to-zero modulation. To transmit 112 Gbps or 56 GBd (GigaBoud) with PAM4 modulation, one symbol time should be 17.8571 ps. In PCB dielectric with Dk=4 it spreads in space over just 2.677 mm (about 105 mil). To understand the scale of PCB and packaging interconnects, we can use the number of bits for NRZ or symbols for PAM4 signal spreading over the length of ideal link as shown next in the space domain:



The ruler above provides scale in cm. Slowdown factor 2 is used for the illustration of the spatial spread for typical PCB dielectric with Dk=4. We can see that at 6 Gbps NRZ only a couple of bits are simultaneously in the packaging part of interconnects (about 5 cm or 2 inches) and about 10 bits are in the PCB part (about 25 cm or 10 inches) at the same time. With the data rate increase to 112 Gbps and PAM4 modulation use, we can observe about 20 symbols (would be 40 bits for NRZ) over the package section of interconnects and about 100 symbols (would be 200 bits for NRZ). The illustration provided above is for the ideal link – it would be like that without any kind of the signal degradation. It never happens in the real world. The signals degrade in real interconnects and such degradation can be predicted with the modeling or analysis or measured with scopes or VNAs. Mathematically, it is easier to model the digital signal degradation in the frequency domain, assuming that the time domain signal is a superposition of harmonics. Harmonics are just sinusoidal signals in time domain. At this point the analog problem in time domain becomes the problem for the harmonics or frequency domain problem. **And the first question always is what is the bandwidth of the signal in the frequency domain and over what bandwidth we have to model or measure it?**

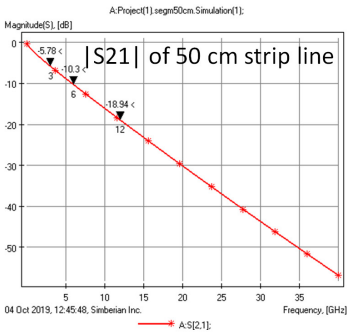
Let's take a closer look at power spectral density (PSD) of 6 Gbps NRZ signal with 50 ps rise time shown next for pseudo-random bit stream PRBS7 (computed with Simbeor SDK):

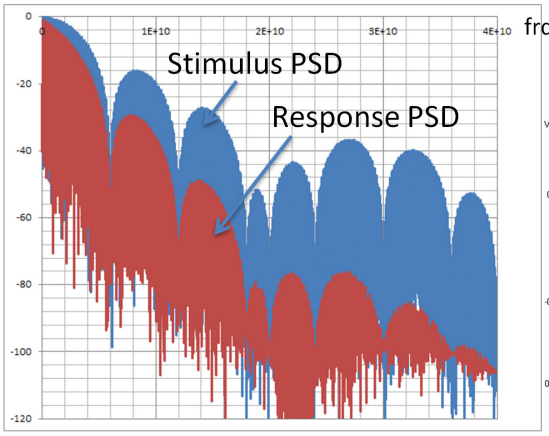


We can see that the signal is a superposition of harmonics with rapidly decreasing magnitudes - the vertical axis on the plot is in dB and starting from about 5 GHz harmonics are below -18 dB. Though, the contribution of such harmonics cannot be considered insignificant. The spectrum has minimum at 1/Tbit or 6 GHz, but rises after that up to -18 dB again. The minimal bandwidth of a link to pass such signal is defined by the Nyquist frequency (0.5/Tbit or 3 GHz in this case) [3]. Obviously, accurate modeling or measurements must include the harmonics above the Nyquist frequency – otherwise the observed or computed signal in time domain would be significantly distorted by the measurements or computations. **Notice that most of the spectrum over the Nyquist frequency is in the microwave bandwidth!** So, what should be the bandwidth for the modeling or measurement for such signal – where to stop the frequency sweep? Should it be 0.5/Trise or 1/Trise? At this point we actually do not have enough data to answer that – we have to consider the problem to be solved.

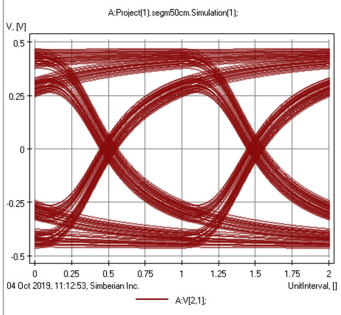
The actual signal does not have exactly linear rise time as used for the spectrum evaluation above. It is not generated like that, and even at the chip IO level the signal is smoothed or filtered by the lossy and dispersive interconnects. The package may be very destructive too. So, let's take a look at the spectrum of the same signal when it passes through 50 cm (about 20 inch) of PCB stripline interconnect just for illustrative purpose. The insertion loss of such link is shown on the left graph below and corresponding response spectrum is shown in the middle graph next (40 GHz bandwidth):

FR408 – Wideband Debye: Dk=3.8,
LT=0.0117 @ 1 GHz
Copper: RR=1.2, Causal Hammerstad
Roughness Model: SR=0.4, RF=2





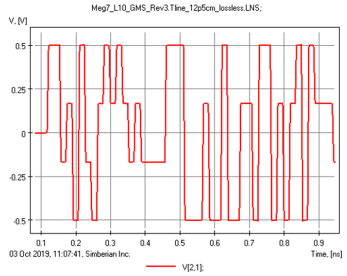
Distorted response



The original PSD is shown in blue (stimulus) and the PSD of the signal passed through is shown in brown. The eye diagram (overlap of the pulses) on the right shows the degradation of the ideal trapezoidal pulses – the rise time increases and there is deterministic (predictable) jitter due to the dispersion (it is actually not jitter, but usually called like that). From the PSD plots we can see considerable attenuation of the high-frequency harmonics. If the analysis or measurements have to be done only for the transmission through the interconnect, it can be done with high accuracy over much smaller bandwidth. **The interconnect reduces the bandwidth for the modeling and measurement for better or worse – this is really important point of this example.**

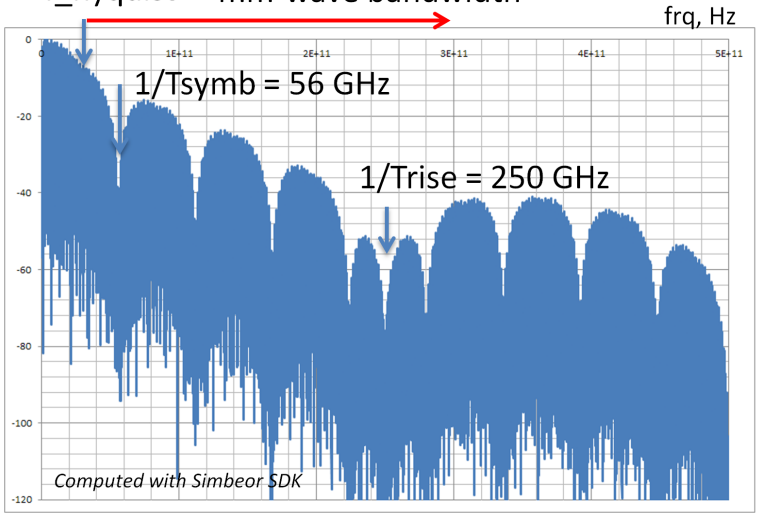
Next, let's take a look at the spectrum of 112 Gbps PAM4 signal with just 4 ps rise time (a little over-optimistic case) – it is computed up to 500 GHz with Simbeor SDK and shown next:

112 Gbps: Trise=4ps;
Tsymb=17.8571ps;
f_nyquist = 28 GHz



PSD of PRBS7

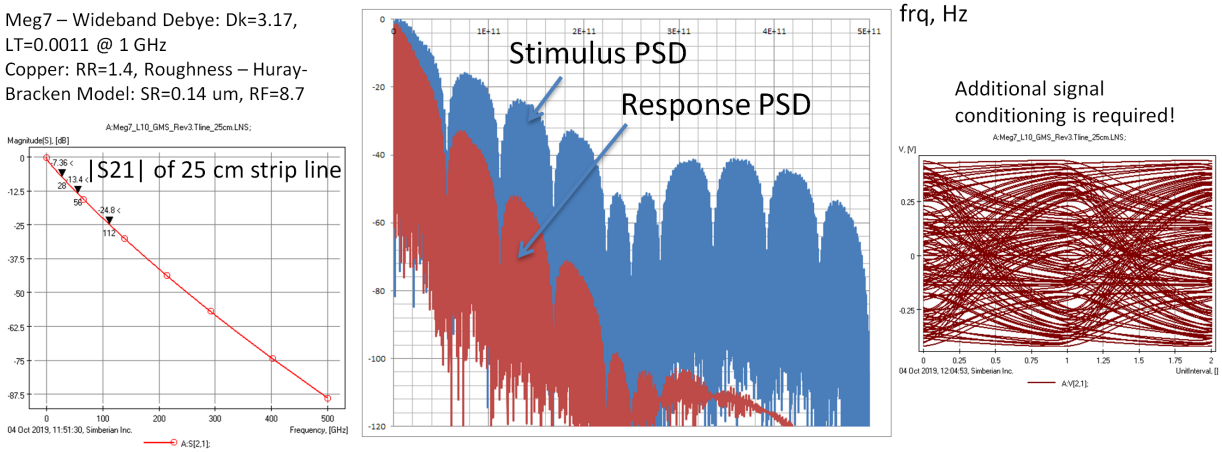
f_nyquist mm-wave bandwidth



What is the bandwidth?
0.5/Trise looks unrealistic…

If the upper frequency estimate 1/Trise looked reasonable in case of 6 Gbps (relatively easy to make models and measurements), it is completely unrealistic in this case – just try to build a model or measure up to 250 GHz. Nyquist frequency 0.5/Tsymb is or 28 GHz in this case – the analysis or measurement up to this frequency will be highly insufficient – most of the spectrum will be unaccounted for. **Notice that the signal spectrum above the Nyquist frequency in this case is in the millimeter-wave bandwidth (over 30 GHz).**

Fortunately, the spectrum changes dramatically when the PRBS signal shown above on the left passes 25 cm (about 10 inch) stripline interconnect as shown next (500 GHz bandwidth):

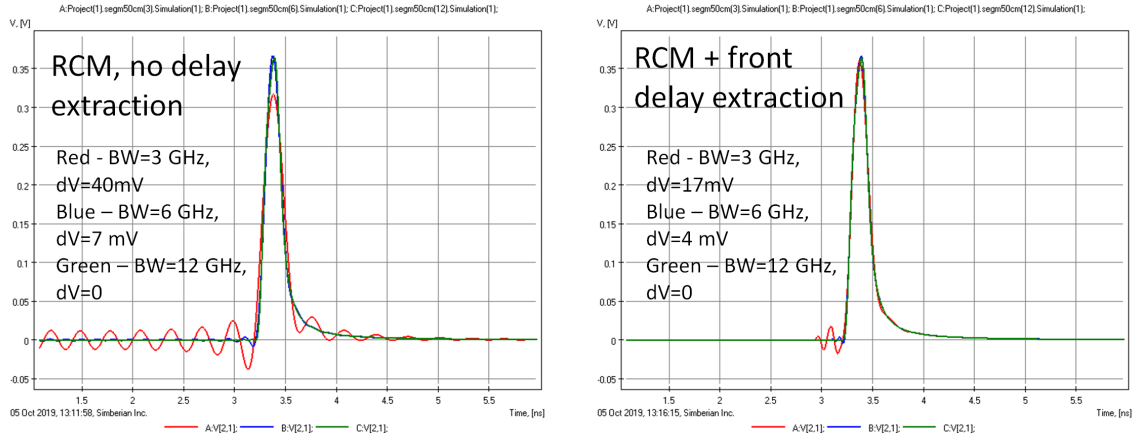


Though, it is actually rather "unfortunately", if you look at the eye diagram on the right – this is how 112 Gbps PAM4 looks when it passes the 25 cm of stripline on a typically designed PCB! It does not look good and requires additional signal conditioning to restore it from such mess. **Can PCB interconnects be designed better than that – absolutely, YES!** But this is beyond of the scope of this paper and will be addressed in [4].

Here is what we learned at this point from a few numerical experiments. The bandwidth required for modeling or measurements is defined by the signal source spectrum (may be computed or measured). It is further reduced by expected channel insertion loss (it includes all kinds of losses - thermal, reflections, leaks – will be discussed in the next article). Such reduction is "unfortunate"- it may degrade the signal up to the point of complete link failure. **In fact, if PCB interconnects are designed following the practices adopted at lower data rates, there will be artificially created "interconnect bottleneck".**
One more thing contributes to the bandwidth. We have not discussed possible coupling or crosstalk here. The model bandwidth must be adjusted to account for the spectrum of the coupled signals that are not attenuated much as the near side (near-end crosstalk or NEXT for instance). **So, is there a universal formula for the bandwidth?** Unfortunately, no – the widely used universal formulas based on rise time or Nyquist frequency that worked at lower data rates may be not usable any more.

Though, there is a universal way to estimate the bandwidth – with numerical experiment! Let's give it a try. First, let's compute the single bit response (SBR) of 50 cm stripline link for 6Gbps NRZ signal used for the spectrum evaluation. We use 40 GHz bandwidth as the benchmark and artificially restrict the modeling bandwidth to 3, 6 and 12 GHz and compare the SBRs as shown below:

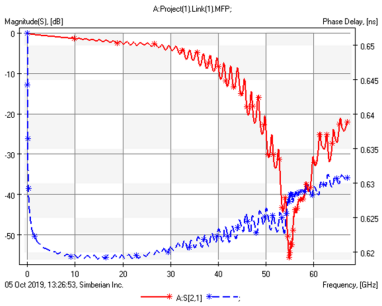
Test case: About 50 Ohm strip line – almost no reflections; FR408 – Wideband Debye: Dk=3.8, LT=0.0117 @ 1 GHz; Copper: RR=1.2, Causal Hammerstad Roughness Model: SR=0.4, RF=2

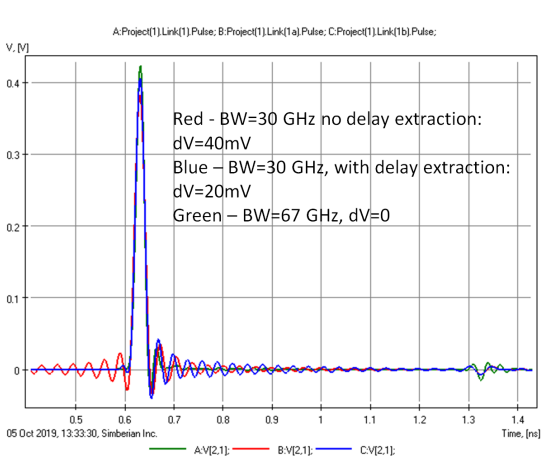


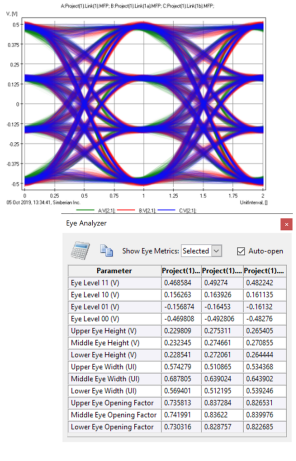
The left plots show SBRs computed in Simbeor software with rational compact model (RCM) without the delay extraction. We can see that if we restrict the bandwidth to just the Nyquist frequency 3 GHz, the SBR will show non causality with peak to peak voltage noise 40 mV – that value may be considered as the error due to the insufficient bandwidth (that is how the insufficient bandwidth usually shows up in time domain). With the extension of the bandwidth up to 6 GHz (1/Tbit), the error is reduced to 7 mV and the error is negligible with the bandwidth 12 GHz. That is what the model or measurement bandwidth should be for this case, ideally. Obviously, one can reduce the "non-causality" by the delay extraction procedure. If RCM is built with the frontal delay extraction (delay is dispersive or changes with frequency), the errors due to the insufficient bandwidth drops as shown on the right graph above. Though, the answer would be still about 12 GHz. Will it work for another type of interconnect? Unfortunately, not – the numerical experiment should be repeated. **Also, the result of such numerical experiment will depend on the software used to compute SBR – validate the software first.**

Single symbol responses (SSR) for 112 Gbps PAM4 signal discussed earlier and computed from S-parameters (shown on the left) measured for a 5 cm (about 2 inch) link are shown below:

Test case: 5 cm of strip line on Meg7 with two vias with stubs;
S-parameters measured up to 67 GHz





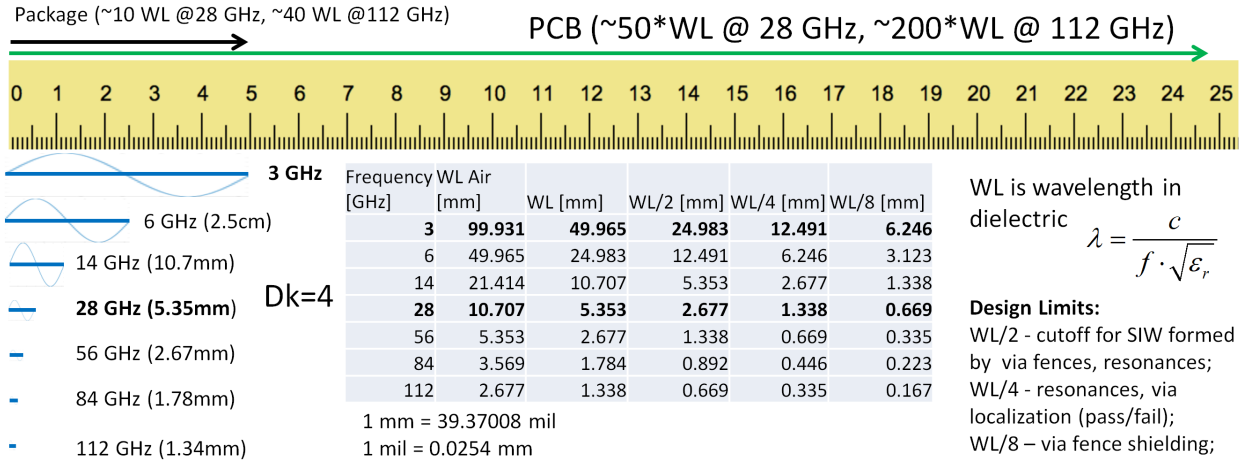


Parameter	Project(1)...	Project(1)...	Project(1)...
Eye Level 11 (V)	0.468584	0.49274	0.482242
Eye Level 10 (V)	0.156263	0.163926	0.161135
Eye Level 01 (V)	-0.156874	-0.16453	-0.16132
Eye Level 00 (V)	-0.469808	-0.492806	-0.48276
Upper Eye Height (V)	0.229809	0.275311	0.265405
Middle Eye Height (V)	0.232345	0.274661	0.270855
Lower Eye Height (V)	0.228541	0.272061	0.264444
Upper Eye Width (UI)	0.574279	0.510865	0.534368
Middle Eye Width (UI)	0.687805	0.639024	0.643902
Lower Eye Width (UI)	0.569401	0.512195	0.539246
Upper Eye Opening Factor	0.735813	0.837284	0.826531
Middle Eye Opening Factor	0.741991	0.83622	0.839976
Lower Eye Opening Factor	0.730316	0.828757	0.822685

67 GHz bandwidth in this case is considered as sufficient for SSR computation and used as the benchmark – it does not produce significant error (no non-causality in the SSR). If the bandwidth is

reduced to 30 GHz (a little over the Nyquist frequency), the error is about 40 mV for the model constructed with RCM and no delay extraction, and about 20 mV with the frontal delay extraction. The eye diagrams for all 3 cases may look very similar – they are shown on the right together with the eye measurements computed with Simbeor Eye Analyzer tool.

This article begins with the illustration of PCB or packaging interconnects scale in terms of bits or symbols in spatial domain. It may be not very practical knowledge, to know how many bits or symbols are in your interconnects at any given moment. Next we learned that for the data rates 6 Gbps substantial part of signal spectrum is in the microwave bandwidth (over 3 GHz) and for higher data rates the spectrum goes into the mm-wave bandwidth (over 30 GHz). The digital interconnects are waveguiding structures at these frequency ranges and should be treated as such. **We are deep in the waveguide analysis territory ruled by the electromagnetic analysis!** Over the microwave and millimeter wave bandwidths it is much more useful to think about the interconnects in terms of wavelengths as the microwave engineers do. Below is the final illustration of PCB and packaging interconnect scale in term of the wavelengths:



Frequency [GHz]	WL Air [mm]	WL [mm]	WL/2 [mm]	WL/4 [mm]	WL/8 [mm]
3	**99.931**	**49.965**	**24.983**	**12.491**	**6.246**
6	49.965	24.983	12.491	6.246	3.123
14	21.414	10.707	5.353	2.677	1.338
28	**10.707**	**5.353**	**2.677**	**1.338**	**0.669**
56	5.353	2.677	1.338	0.669	0.335
84	3.569	1.784	0.892	0.446	0.223
112	2.677	1.338	0.669	0.335	0.167

1 mm = 39.37008 mil
1 mil = 0.0254 mm

WL is wavelength in dielectric $\lambda = \frac{c}{f \cdot \sqrt{\varepsilon_r}}$

Design Limits:
WL/2 - cutoff for SIW formed by via fences, resonances;
WL/4 - resonances, via localization (pass/fail);
WL/8 – via fence shielding;

We can see that the electrical length of 5 cm package is about 1 wavelength at 3 GHz and 10 wavelengths at 28 GHz. The electrical length of 25 cm PCB is about 5 wavelength at 3 GHz and about 50 wavelength at 28 GHz. Though, it is not very important. **More important are the design limits imposed by the wavelengths are also provided on the picture above.** The wavelength in dielectric with Dk=4 at the frequency 3 GHz is about 5 cm (about 2 inch) – that is at the Nyquist frequency for 6 Gbps NRZ signal. It is very easy to follow the design limits set by the wavelength for the reference integrity, via localization and to avoid the resonances. The wavelength in dielectric at 28 GHz (Nyquist frequency for 112 Gbps PAM4 signal) is just 5.353 mm (about 210 mil). It limits the distance to stitching vias to just 1.338 mm or 70 mil, to have the viahole transitions localized. And this is just a bare minimum – to be predictable, the viaholes must stay localized above that frequency.

This article demonstrates importance of numerical experiment in making a decision on the bandwidth for PCB or packaging interconnect modeling and measurements. By building models with the excessive bandwidth (requires only realistic transmission line models) and observing the effect of the bandwidth reduction we can identify the bandwidth for the system investigation.

REFERENCES:

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