Flawless Interconnect Design with Simbeor Software

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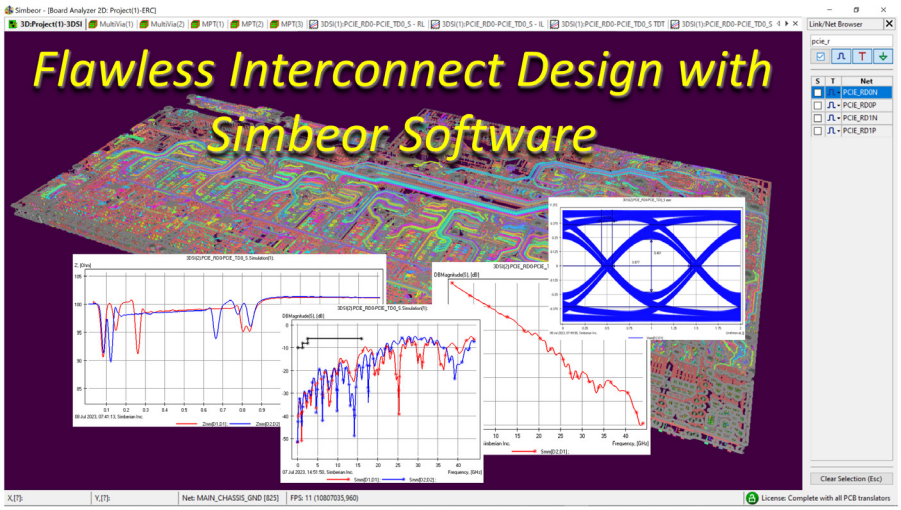


Data rates in PCB interconnects are increasing in all signaling protocols (PCIe, DDR, GDDR, Ethernet, USB, SAS, InfiniBand, CEI, OIF, 5G,…). Most of those high speed signaling standards have one-lane data rates over 6 Gbps (GT/s) and some up to 112 Gbps with signal spectrum in microwave and even millimeter wave bandwidths [1]. Design of compliant interconnects at these data rates cannot simply rely on geometrical rules or rules of a thumb. **Signal distortion by reflections, dissipation and crosstalk can cause interconnect performance degradation or even failure.** To avoid it, signal integrity compliance analysis and possible interconnect optimization is required and Simberian's Simbeor software is the ideal tool for that. This article gives an overview of Simbeor electromagnetic signal integrity software and highlights its new features.

Simbeor is state-of-the-art software for 3D electromagnetic analysis of PCB and packaging interconnects. It can be used for pre-layout design (stackup exploration, viahole design) and post-layout interconnect compliance analysis and optimization. Simbeor ensures the accuracy of the models by using advanced algorithms for 3D full wave analysis, benchmarking and experimental validation. Simbeor and the "sink or swim" interconnect design process [2], [7] remove all uncertainties and guarantee the first pass design success. Most important, Simbeor lets you solve electromagnetic signal integrity problems at a relatively low cost and with extreme ease. You don't need to be an expert in signal integrity or have a PhD in electromagnetics to use it. No other tool can match that.

The first version of Simbeor was introduced in 2007. It was the first electromagnetic tool designed specifically for PCB designers and signal integrity engineers. Since then Simbeor evolution is a chain of innovations in interconnect analysis and validation (see Appendix 1). In the past three years, with the major part of it in "self-isolation", Simberian's team elevated Simbeor to a new level. Simbeor software development kit (Simbeor SDK) was introduced for design exploration and machine learning and for possible integration into other tools [3]. Post-layout geometry processing, visualization and model building were accelerated orders of magnitude. Electromagnetic analysis was also accelerated orders of magnitude with the domain decomposition technique. We had enough time (not much distractions) and sufficient expertise to re-think and re-design the post-layout process – make it suitable

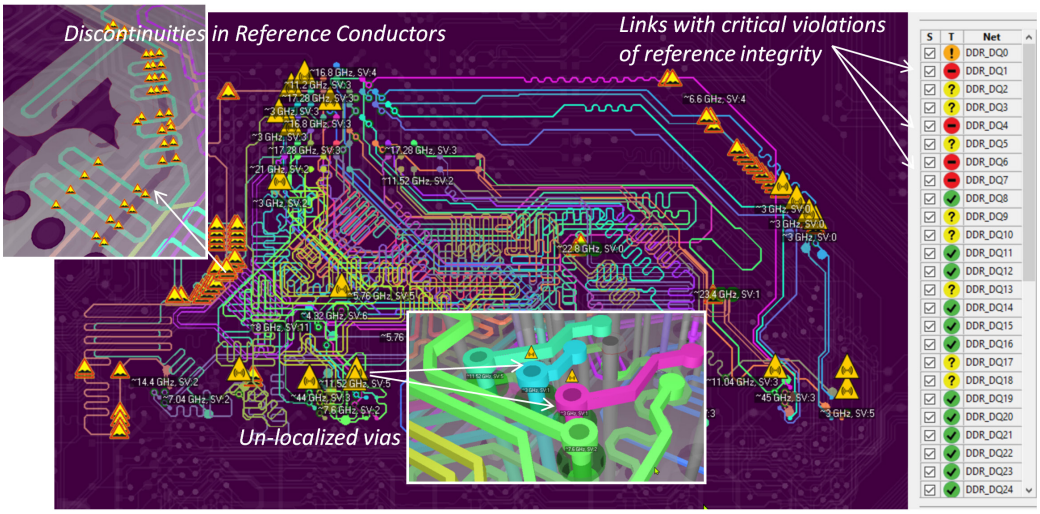
not only for SI engineers, but for any PCB designer. As the result, we have created a tool called SI Compliance Analyzer™ that does not have analogs so far.

SI Compliance Analyzer can be used for fast and consistent post-layout signal integrity verification with simulation-based electrical rule checking (ERC), basic signal integrity analysis (Fast SI), and advanced 3D EM signal integrity analysis (3D SI). Basically, SI Compliance Analyzer should be a one-stop solution for all interconnect validation and compliance analysis tasks with one unified easy-to-use interface and the following operating modes:

- **Electrical Rule Checking (ERC):** uses 2D quasi-static field solver Simbeor SFS solver for traces and component pads and fast EM models of viaholes, to find reference integrity and localization violations, impedance continuity violations and possible crosstalk noise. This mode can be used for interactive analysis of links in fraction of a second or thousands of links with automation. It makes all geometry-based rule checkers obsolete and unnecessary.
- **Fast SI:** uses 2D quasi-static field solver Simbeor SFS for traces and pads, fast EM models of viaholes and precise de-composition for the basic signal integrity analysis of crosstalk noise, losses, delay and skew for relatively slow signals (<10 Gpbs, >100 ps rise time) or preliminary analysis of high-speed links. It enables interactive analysis of links in seconds or hundreds of links with the automation in real time.
- **3D SI:** uses 2D quasi-static field solver Simbeor SFS or a 3D EM solver for traces and 3D EM solver (Simbeor 3DML or 3DTF) for viaholes, component pads and other discontinuities and precise de-composition for advanced signal integrity analysis of PCB/Packaging Interconnects (unlimited data rates, accuracy depends on geometry, materials and link localization). It enables interactive analysis of links in minutes or hundreds of links with the automation in real time.

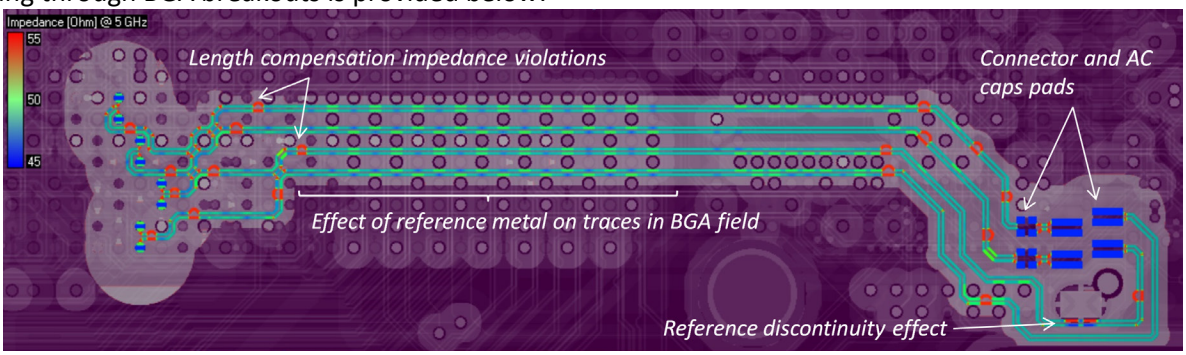
All those modes are designed to verify interconnect compliance with a particular signaling standard and quickly find the reason for failure if a compliance metric is violated. A few examples of interconnects analysis and optimization are provided in this article, to illustrate the process.

A perfect digital interconnect is a lossless transmission line with constant characteristic impedance and phase delay over the signal bandwidth and termination resistors matching the characteristic impedance. In such interconnect bits sent by transmitter would flow smoothly into the receiver with no bit rate limits. Such ideal transmission line is only imaginary and theoretical. The physics of our world does not allow that. To ensure that the digital signal is actually getting through, we have to build interconnect models that include all signal degradation factors important for a specific data rate. But, before building any model, the reference integrity and viahole localization must be verified and fixed if necessary. **Reference integrity analysis** in ERC mode of SI Compliance Analyzer does exactly that. It checks all reference conductors and stitching vias, and viahole localization [4]. Basically, it is the analysis of the current return path. Below is an example of the reference integrity analysis in Simbeor software for all DDR data links on the Open Computing Project (OCP) PCB:



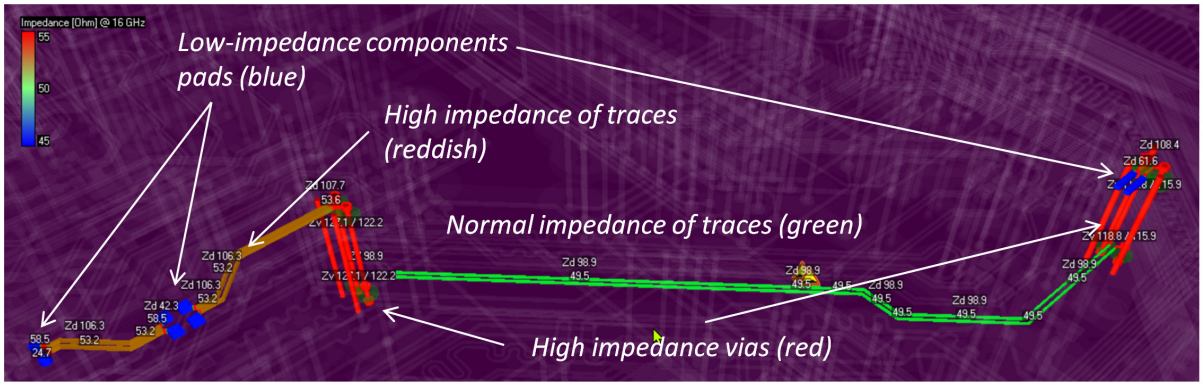
The analysis is done for DDR5 data rate 6.4 GT/s and reveals some problems in the nets marked with the red stop signs on the right (severe reference integrity violations). Some traces go over the splits in the closest reference planes and some viaholes are un-localized (begin leaking the energy at the Nyquist frequency). **The severe reference integrity violations must be fixed in layout before proceeding with any other type of analyses. This is imperative!** The PCB in this case was designed for DDR3 and as we can see cannot be used "as is" for DDR5.

When all reference integrity problems are corrected we can proceed with the other types of compliance analysis. **Impedance continuity analysis** in ERC mode of SI Compliance Analyzer can be used to quickly check the impedance of interconnects, including viaholes and pads (more on the impedance and reflection in [5], [6]). Here is an example demonstrating precision of the impedance analysis in Simbeor and how the reference conductors can change the impedance of traces on a design with traces going through BGA breakouts is provided below:

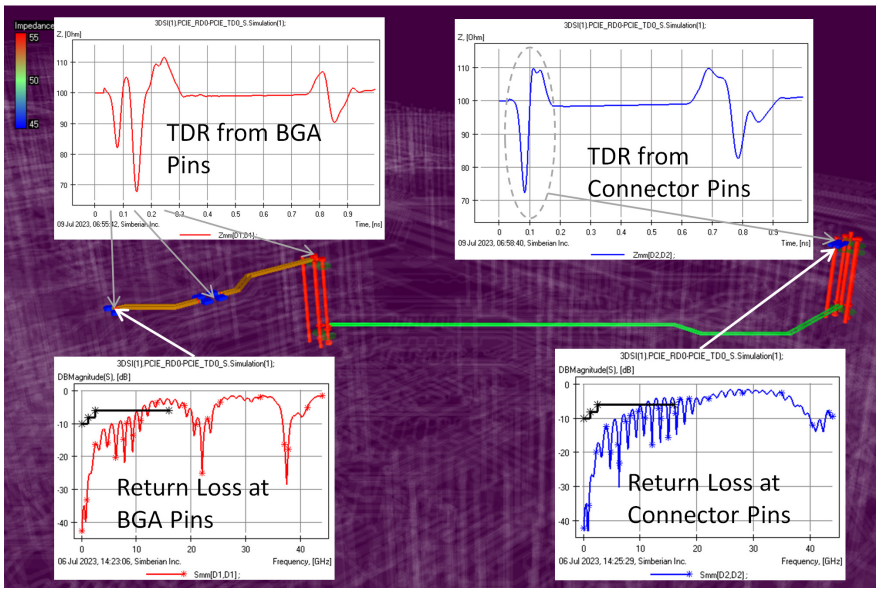


Simbeor evaluated the effect of cut-outs and reference pads on the impedance. We can see that the impedances of connector and AC coupling pads are below the target and the impedance of the length compensation sections is above the target (layout mistake). The discontinuities in the reference conductors also create impedance violations (another layout mistake discovered by Simbeor).

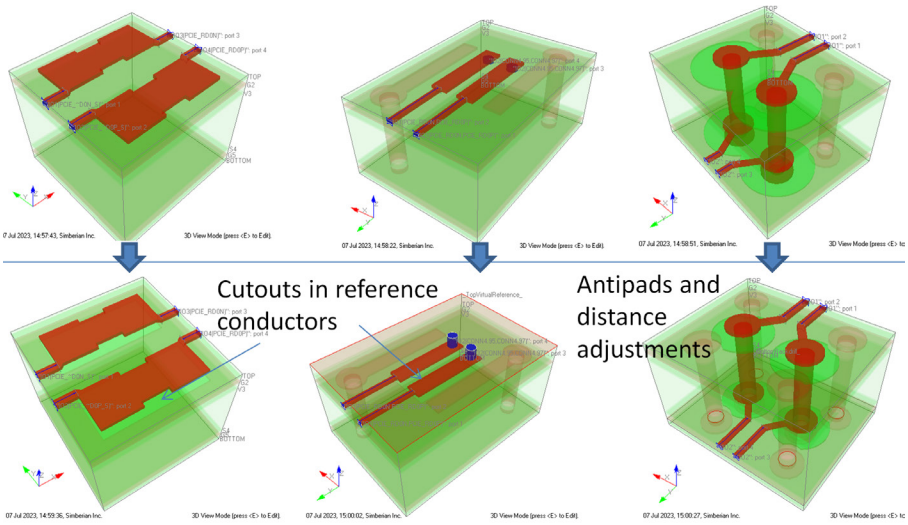
Here is another example of the impedance continuity analysis for properly localized PCIe link on OCP board:



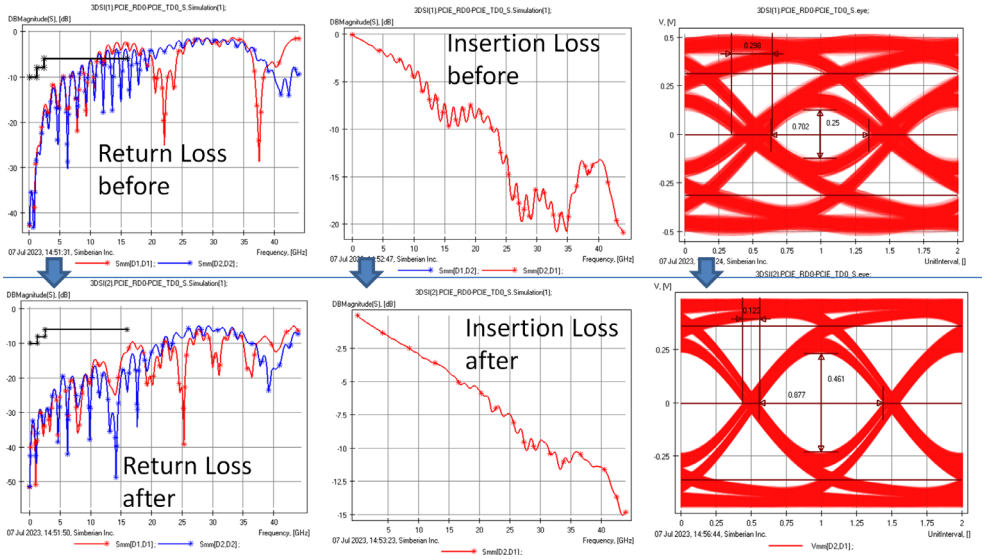
The analysis is done at the Nyquist frequency of PCIe 5.0 signal running at 32 GT/s. The target differential impedance is 100 Ohm and we can see that the link may require some improvements. The question is how the impedance violations affect the signal transmission. **Analysis of reflections in 3D SI analysis mode** (or Fast SI for lower data rates) of SI Compliance Analyzer can be used to answer that. Accurate 3D SI models are used here to compute Return Loss (RL) and do the TDR analysis as illustrated next:



The return loss violates PCIe 5.0 standard mask (black line on the bottom graphs) in this case and the main reasons for that are the reflections from the component pads, viaholes and microstrip traces on the top side of the board (dips and spikes on TDR plots of the top graphs). That was also observed on the preliminary impedance continuity analysis in the ERC mode. The link requires optimization that can be also done in Simbeor. Small cut-outs in the reference conductors below the signal pads can be used to reduce the capacitance of the component pads and adjustments of distance between the signal viaholes and anti-pad size can be used to reduce the inductance of viaholes as illustrated next:

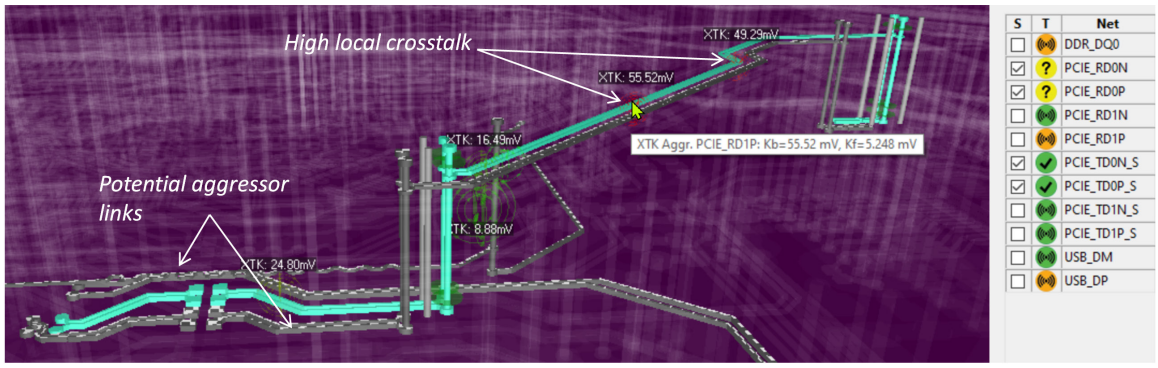


The original geometries of the discontinuities are shown in the top row and the adjusted more optimal or less reflective discontinuities are shown in the bottom row.
The results of such small adjustments are shown next:



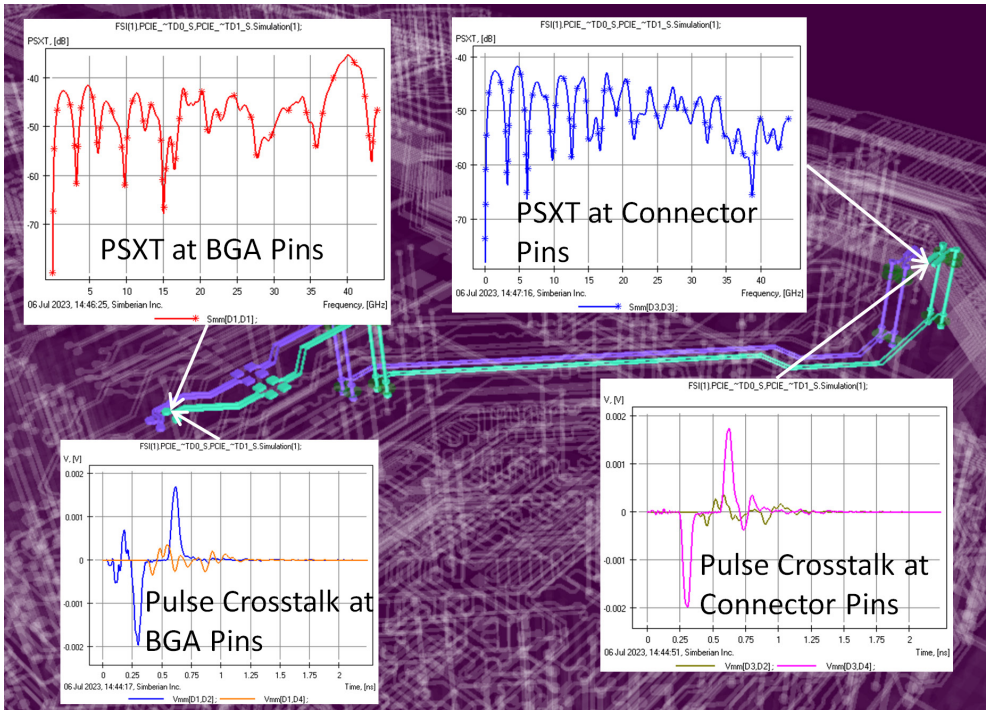
Return and insertion loss and eye diagram of the original link are shown in the top row and corresponding results for the adjusted link are shown in the bottom row. What a difference such small adjustments make! The link passes the return loss mask (black line) and the eye is larger (more margin for possible random unpredictable things).

Simbeor SI Compliance Analyzer can be used for control of all types of standard compliance metrics (RL, IL, Fitted IL, ILD, PSXT, MDXT, ICN, ICR,…). **That includes the crosstalk analysis.** Local crosstalk evaluation can be done in ERC mode of SI Compliance Analyzer as illustrated below:



For a selected link Simbeor finds all possible aggressor links and evaluates trace to trace and pad to pad coupling in mV (can be dB or %), assuming 1 V excitation with the rise time specified for the signal. It eliminates all types of geometrical proximity rules.

To evaluate the **system-level impact of the crosstalk**, Fast SI or 3D SI analysis modes of SI Compliance Analyzer can be used. Fast SI mode includes crosstalk between the traces and pads and 3D SI optionally adds crosstalk evaluation between the vias. The analysis can be done in frequency domain (PSXT, ICR, ICN, MDXT,…) as well as in time domain (step, pulse crosstalk or eye diagram with crosstalk) as illustrated next:



The top graphs show Power Sum Crosstalk (PSXT) at the BGA and connector pads and the bottom graphs show the pulse crosstalk for 32 GT/s signal with 25 ps rise time and 0.5 V excitation. 3D SI analysis is used for this example.

Overview of Simbeor electromagnetic signal integrity software with focus on the recently added SI Compliance Analyzer™ is provided in this article. All type of the signal integrity analyses demonstrated here can be done in Simbeor with just a couple of button clicks (see how it can be done at https://www.youtube.com/@simbeor/videos). That enables seamless and easy to setup **post-layout analysis automation with scripting** for the whole board with optional **comparison of the results with the previous iteration of the same design**. All critical links on a board can be either checked in minutes

with simulation-based ERC analysis (all applications), or simulated in tens of minutes with Fast SI analysis (DDRx), or simulated in a few hours with the measurement-validated 3D SI analysis (SerDes). Note that the accuracy of all types of analyses, except the reference integrity, depends on the accuracy of the material models and the accuracy of PCB manufacturing [7], [8]. Broadband dielectric and conductor roughness models have to be identified before the analysis and Simbeor is ideal tool for that too. Four methods are available in Simbeor for the broadband dielectric and conductor roughness model identification. That can be done manually or automated with Simbeor SDK. The upcoming release of Simbeor 2023 further pushes the boundary of possibilities with the extensions in EM solvers, to build accurate models at frequencies over 50 GHz, and new capabilities in SI Compliance Analyzer, to increase productivity of PCB designers.

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Appendix 1: Simbeor Technology Evolution (see details at https://www.simberian.com/News.php)

- 2007: The first Method of Lines electromagnetic solver for PCB interconnects (Simbeor 3DML);
- 2009: New material model identification method with GMS-parameters (DesignCon best paper award winner);
- 2010: The first de-compositional electromagnetic analysis of PCB interconnects (IEC Design Vision award winner);
- 2011: The first S-parameters quality assurance and macro modeling tool Touchstone Analyzer (UBM Design Vision award winner, metrics are standardized in IEEE P370);
- 2012-2014: The first electrical viahole design tool Via Analyzer, easy-to-use post-layout analysis tool Board Analyzer, quasi-static MoM solver Simbeor SFS, new “sink or swim” approach for design of predictable interconnects (UBM Best in Design and Test finalist, 2015);
- 2015: The first 3D EM solver based on Trefftz finite elements (Simbeor 3DTF);
- 2017: The first easy-to-use cloud accelerator for electromagnetic analysis (Simbeor Agent);
- 2018: The first version of automatic post-layout EM analysis in Board Analyzer;
- 2018: Systematic approach to analysis to measurement validation (DesignCon best paper award winner);

- 2019: The first interconnect analysis toolkit for design automation and machine learning (Simbeor SDK);
- 2020-2021: Acceleration of EM solvers with domain decomposition, acceleration of geometry processing;
- 2022-2023: The first completely automatic post-layout 3D EM analysis with easy-to-do analysis and comparison automation (SI Compliance Analyzer);