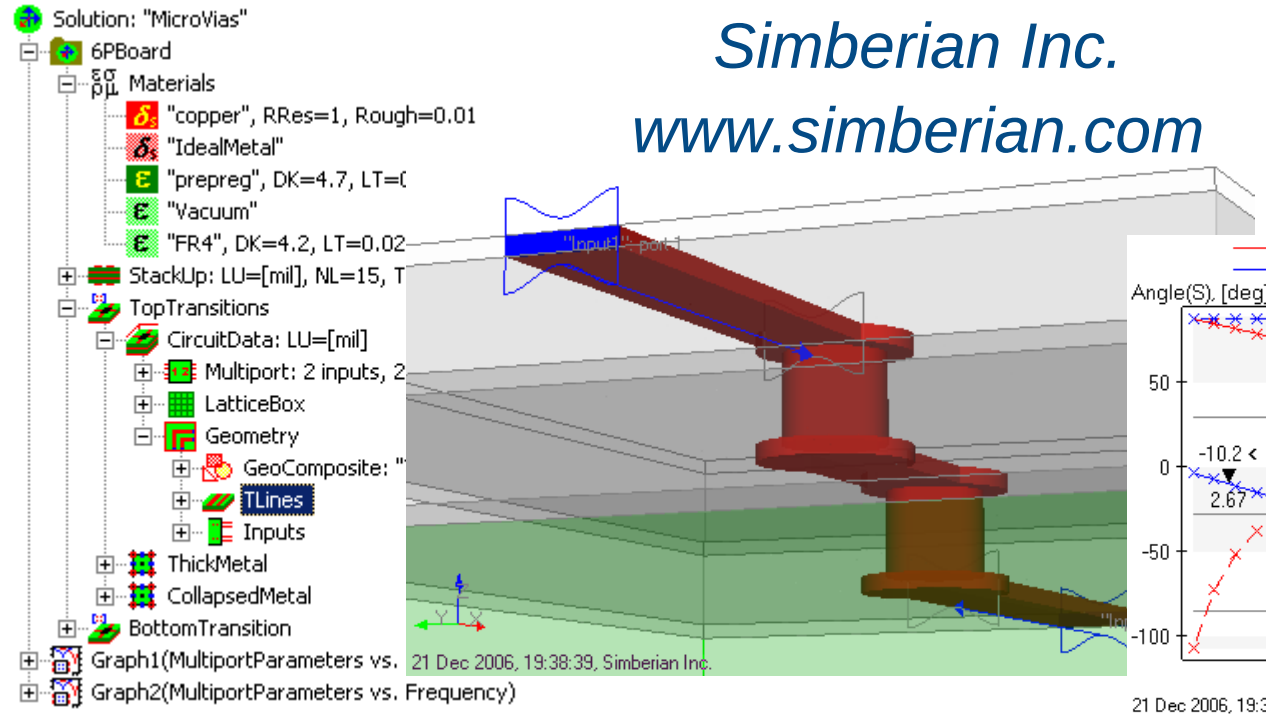
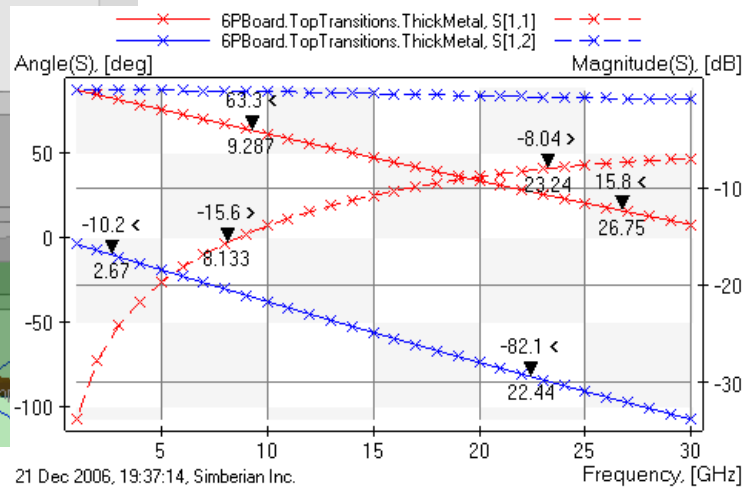
Simberian Electromagnetic Solutions

Designing localizable minimal-reflection via-holes for multi-gigabit interconnects

Simberian Inc.

www.simberian.com





Property of Simberian Inc.

- Copyright © 2009 by Simberian Inc., All rights reserved.
  - THIS DOCUMENT IS CONFIDENTIAL AND PROPRIETARY TO SIMBERIAN INC. AND MAY NOT BE REPRODUCED, PUBLISHED OR DISCLOSED TO OTHERS WITHOUT PERMISSION OF SIMBERIAN INC.
- Simberian® and Simbeor® are registered trademarks of Simberian Inc.
  - Other product and company names mentioned in this presentation may be the trademarks of their respective owners.

Overview

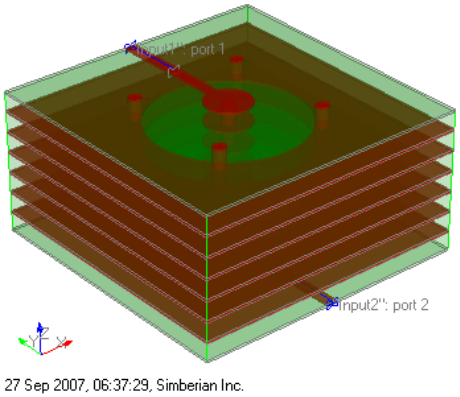
- Introduction
- Localization of single via-holes
- Localization of differential via-holes
- Electromagnetic analysis of via-holes
- Multiport parameters
- Designing optimal via-holes with experimental validation
- Conclusion
- Solutions and contacts

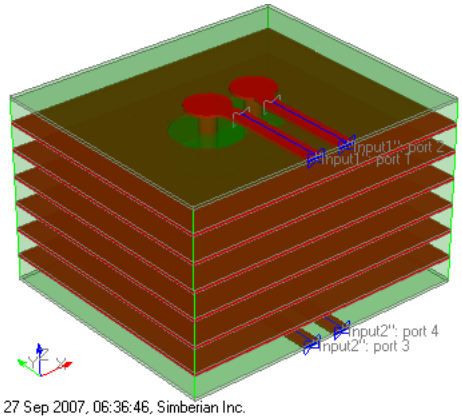
Introduction

- Via-holes are structures connecting components and traces in different layers of multi-layered printed circuit boards (PCBs) or packages
- They are relatively small comparing to the traces and behave almost like ideal connections at low frequencies (below 1-3 GHz) due to small electrical length and small impedance of the current return path
  - A lumped inductance and/or with a lumped capacitance, calculated with approximate equations may be sufficient to model the via effect at these frequencies
- This was working fine until recently, when the spectrum of the signals transmitted through the interconnects reached the microwave range (above 3 GHz for 6 Gb/s signals)
  - The via-holes behave as distributed structures starting from 3 GHz and must be simulated as the distributed structures
- Unfortunately, not all vias are identical from the analysis point of view
  - Some via-holes can be simulated in isolation from the rest of the board and some may require the analysis of the whole board with all reference and power distribution structures included
- **This app note explains how to distinguish different cases and to build localizable minimal-reflection via-holes with Simbeor 2008**

Via-hole types and common traits

- Via-hole types
  - Single-ended and differential
  - Through, blind, buried and back-drilled vias
  - Signal vias and stitching vias
  - Micro-vias
  - …
- Common traits
  - There are no simple models for analysis of multi-gigabit signal propagation (especially if vias are going through multiple parallel planes)
  - Electromagnetic analysis is required at microwave frequencies
  - All types of vias can be characterized with multiport parameters



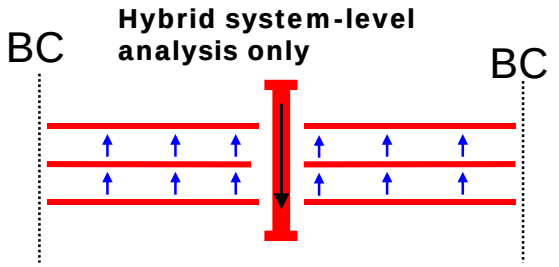


Localizable and non-localizable vias

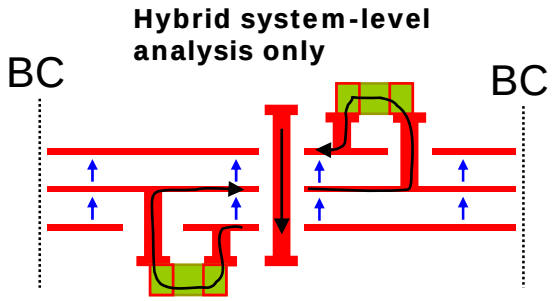
- Via-hole current return path localization may be used to separate all via-holes in two groups for analysis purpose
  - **Via-holes with the current return path in a small area around a via can be called localizable**
  - **Otherwise, if the current return path is spread over the board, the via can be called non-localizable**
- Via-holes that connect traces with the same reference planes can be always analyzed in isolation (though they may radiate)
- It is not the case for the vias connecting traces with different reference planes (via-holes crossing one or more reference planes)
- Let's investigate the return current localization separately for **single-ended and differential via-holes**

Analysis of single vias going through multiple parallel planes

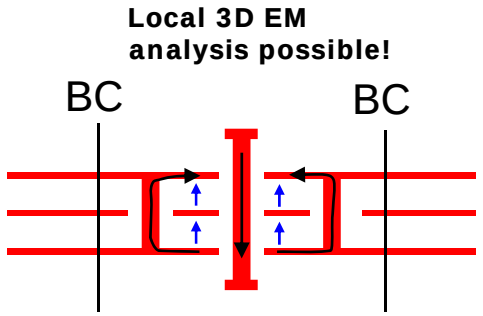
- Planes are not terminated and the return current is the “displacement” current between the planes
  - The problem is non-localizable – requires analysis of the whole board



- Planes are terminated with the decoupling capacitors and the return current is a combination of the “displacement” currents through capacitors and planes
  - Decaps have low impedance only in a narrow band – thus the problem again is non-localizable for broadband EM analysis



- Stitching vias are used to connect the reference planes for the connected layers and the return current is mostly conductive
  - Problem can be localized (localizable) and solved with any boundary conditions (frequency band is limited)



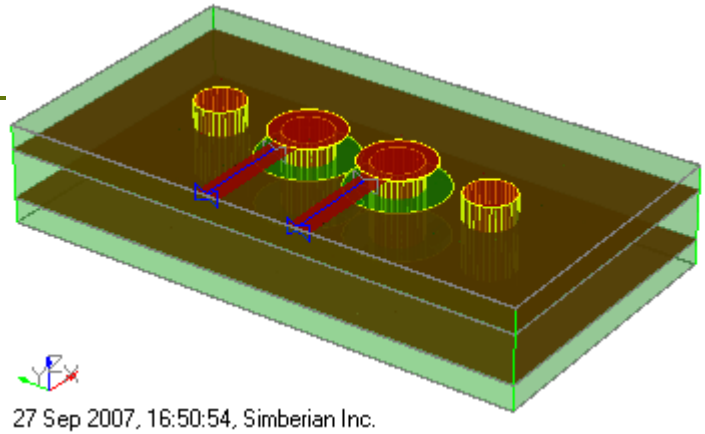
How to model the non-localizable cases (without stitching vias)

- S-parameter models become dependent on the simulation area and boundary conditions
  - Independence of the boundary conditions indicates that the problem is localizable
- Any type of locally enforced boundary conditions is not correct for non-localizable problem
  - PEC (electric walls) are equivalent to short-circuiting the planes at a distance from vias – preferable
  - PMC (magnetic walls) are equivalent to open-circuiting the planes at a distance from vias – incorrect low frequency asymptotic of S-parameters
  - PML (perfectly matched layer) or ABC (absorbing boundary conditions) – absorbs energy at a distance from vias
    - Not equivalent to the infinite planes (infinite planes or radial waveguides reflect energy at any location)
    - Absorbed energy is completely lost for the system level analysis (it will appear somewhere on the real board)
- Possible way to solve a non-localizable problem is either put the whole board into 3D solver or to use a hybrid simulation technique with transmission plane solver

Alternative - use stitching vias

- For multi-gigabit signals single-ended vias always require electrically close stitching via-holes connecting all reference conductors of the connected transmission lines
- Localized vias can be locally simulated with any boundary conditions at a sufficient distance (though PEC are asymptotically correct and preferable)
- The number of stitching via-holes to keep the localization may be up to 4-6 stitching vias or more per signal via for localization up to 20 GHz on a typical PCB
- Localizable via-holes are relatively independent of the simulation area or board shape and size and can be simulated in the isolation from the rest of the board and reliably reused as a design component

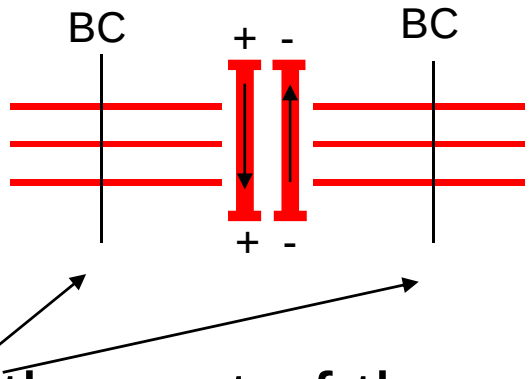
Differential via-holes



- Differential vias are two-via transitions through multiple parallel planes with possible stitching vias nearby
- Two modes propagate independently trough a **symmetrical** pair
  - Differential (+-) – two vias are two conductors: $Id=0.5(I1-I2)$, $Vd=V1-V2$
  - Common (++) – two vias one conductor and parallel planes with decoupling is another conductor: $Ic=I1+I2$, $Vc=0.5(V1+V2)$
- Signal in differential pair always contain differential mode (useful) and may contain common mode induced by asymmetries in driver and discontinuities

S-parameter model for differential mode (differential model)

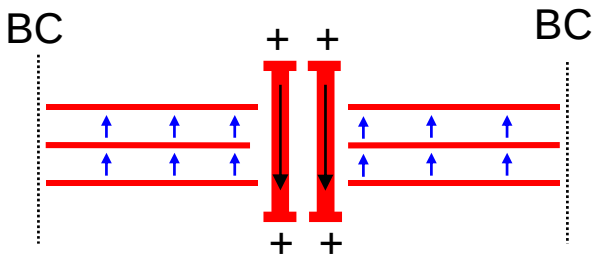
- Differential mode has two identical currents on the via barrels (vias have to be electrically close)



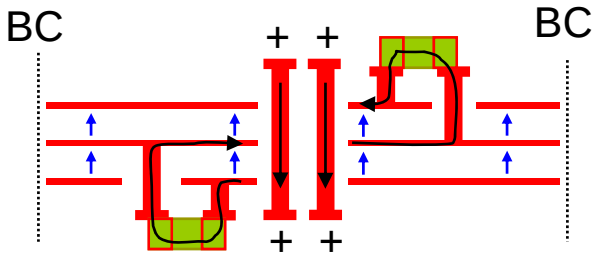
- The vias can be isolated from the rest of the board for the electromagnetic analysis with any boundary conditions (PEC, PMC, PML, ABC)
  - Distance from the vias to the simulation area boundaries should be larger then the largest distance between the planes to reduce the effect of sidewalls
  - In that case, the differential mode S-parameters are practically independent of the boundary conditions

Analysis of common mode in differential vias going through multiple parallel planes

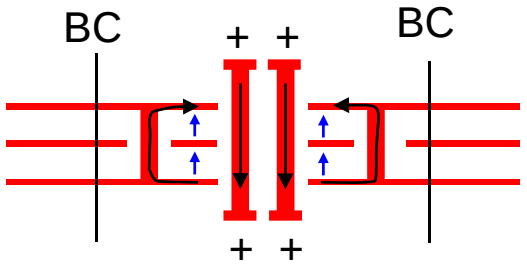
- Planes are not terminated and the return current for common mode is the "displacement" current between the planes
  - The problem is non-localizable – may require analysis of the whole board



- Planes are terminated with the decoupling capacitors and the return current is a combination of the "displacement" currents through capacitors and planes
  - Decaps have low impedance only in a narrow band – thus the problem again is non-localizable for broadband EM analysis



- Stitching vias are used to connect the reference planes for the connected layers and the return current is mostly conductive
  - Problem can be localized (localizable) and solved with any boundary conditions (frequency band is limited)



How to simulate differential vias with the common mode?

- Simulate the whole board in a 3D full-wave solver with all plane terminations
  - Hardly ever possible and not practical
- Use a hybrid solver with 2D parallel-plane models
  - Practical, but accurate only if such solvers include 3D full-wave models for differential mode (no such solvers available so far)
- Localize the problem with asymptotically correct PEC boundary conditions
  - Influence of the boundary conditions on the performance at the system level may be insignificant in many cases
  - May work if no common mode or it is very small at the connections to the vias

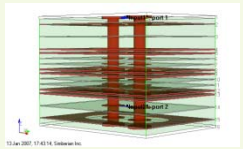
Electromagnetic analysis of via-holes

3D Static and Magneto-Quasi-Static Solvers

$$\vec{E} = -\nabla\varphi - j\omega\vec{A}$$
$$\vec{H} = \frac{1}{\mu}\nabla\times\vec{A}$$

3D Full-Wave Solver

$$\nabla\times\vec{E} = -i\omega\mu\vec{H}$$
$$\nabla\times\vec{H} = i\omega\varepsilon\vec{E} + \sigma\vec{E} + \vec{J}$$

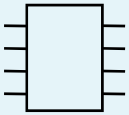


Transmission Plane Solvers

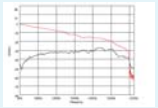
$$\frac{\partial J_{sx}}{\partial x} + \frac{\partial J_{sy}}{\partial y} = -Y_{\square}(\omega)\cdot V + J_z$$
$$\frac{\partial V}{\partial x} = -Z_{\square}(\omega)\cdot J_{sx}$$
$$\frac{\partial V}{\partial y} = -Z_{\square}(\omega)\cdot J_{sy}$$

Simple lumped or distributed LC models

Multiport S-parameters



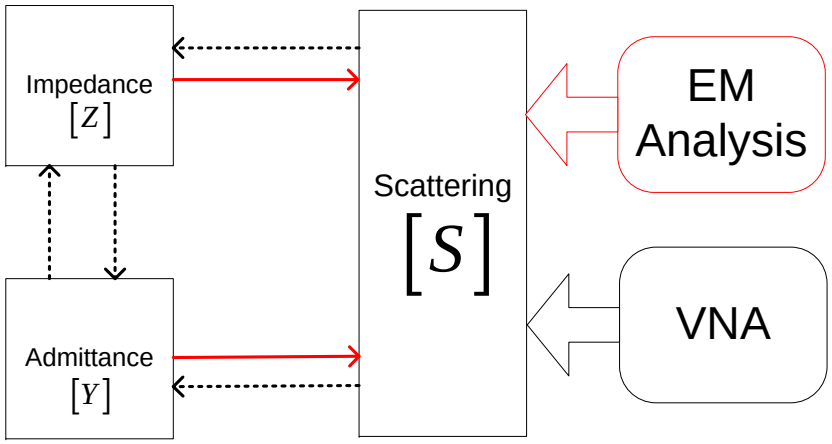
Hybrid 2D transmission plane + circuit solvers



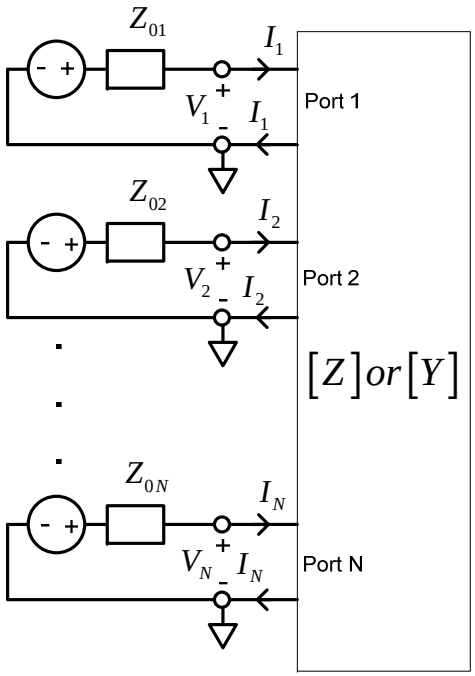
System-level simulator

Multiport parameters

- Multiport is a natural and scalable black-box description of linear structures smaller, comparable with, or larger than wavelength
- Multiport parameters of via-holes and other components are usually united and simulated with non-linear drivers and receivers in time domain
- Multiport parameters are output of electromagnetic simulators as well as Vector Network Analyzers (VNA)



Impedance and admittance parameters



Equivalent currents and voltages at ports: $\bar{I} \in C^{N\times 1}$, $\bar{V} \in C^{N\times 1}$

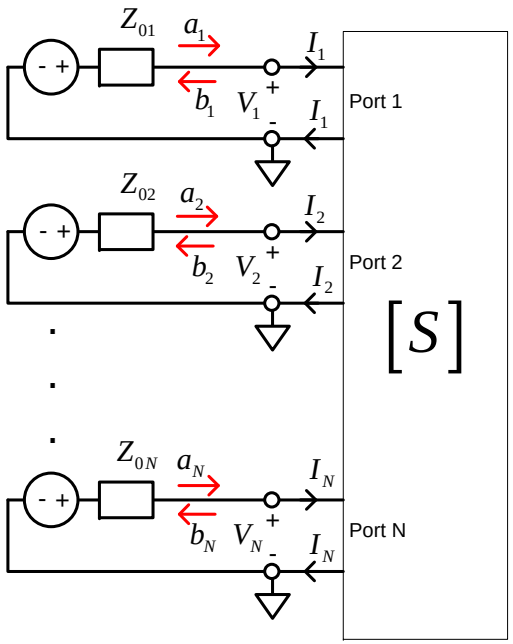
Impedance parameters: $\bar{V} = Z \cdot \bar{I}$, $Z \in C^{N\times N}$, $Z_{i,j} = \left.\frac{V_i}{I_j}\right|_{I_k=0\ k\neq j}$

Admittance parameters: $\bar{I} = Y \cdot \bar{V}$, $Y \in C^{N\times N}$, $Y_{i,j} = \left.\frac{I_i}{V_j}\right|_{V_k=0\ k\neq j}$

Conversion: $Y = Z^{-1}$, $Z = Y^{-1}$

- Immitance parameters are convenient for circuit analysis
- Matrix elements may have large dynamic range and singularities
- Can not be measured directly at high frequencies when structure size is comparable with wavelength

Scattering parameters definition



Incident and reflected waves:

$$\bar{a} = \frac{1}{2\sqrt{Z_0}}\left(\bar{V} + Z_0 \cdot \bar{I}\right), \quad \bar{b} = \frac{1}{2\sqrt{Z_0}}\left(\bar{V} - Z_0 \cdot \bar{I}\right), \quad \bar{a}, \bar{b} \in C^{N\times 1}$$

$$Z_0 = diag\{Z_{0i}, i = 1, ..., N\} \in C^{N\times N}$$

Scattering parameters:

$$\bar{b} = S \cdot \bar{a}, \qquad S \in C^{N\times N}, \qquad S_{i,j} = \left.\frac{b_i}{a_j}\right|_{a_k = 0 \; k \neq j}$$

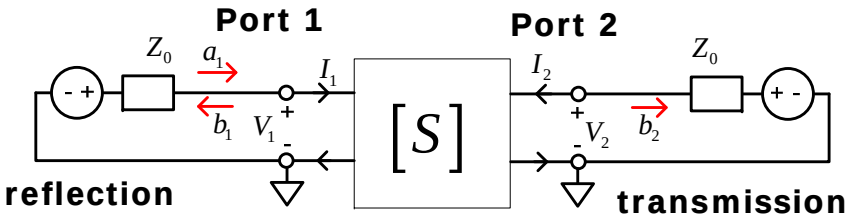
$$S = \left(U - Y_N\right) \cdot \left(U + Y_N\right)^{-1}, \; Y_N = Z_0^{1/2} \cdot Y \cdot Z_0^{1/2}$$

$$S = \left(Z_N - U\right) \cdot \left(U + Z_N\right)^{-1}, \; Z_N = Z_0^{-1/2} \cdot Z \cdot Z_0^{-1/2}$$

- S-parameters can be directly extracted from electromagnetic simulation or measured at any frequency including DC
- S-parameters are free from singularities
- S-parameters can be directly used in a SPICE simulators

S-parameters definitions for 2-port model

$$\begin{bmatrix} b_1 \\ b_2 \end{bmatrix} = \begin{bmatrix} S_{1,1} & S_{1,2} \\ S_{2,1} & S_{2,2} \end{bmatrix} \cdot \begin{bmatrix} a_1 \\ a_2 \end{bmatrix}$$



reflection coefficient

$$S_{1,1} = \left.\frac{b_1}{a_1}\right|_{a_2=0}$$

transmission coefficient

$$S_{2,1} = \left.\frac{b_2}{a_1}\right|_{a_2=0}$$

$$V_i^+ = \sqrt{Z_0} \cdot a_i$$ **voltage of incident wave**

$$V_i^- = \sqrt{Z_0} \cdot b_i$$ **voltage of reflected wave**

$$V_i = V_i^+ + V_i^-$$ **total voltage**

$$I_i = \frac{1}{Z_0}\left(V_i^+ - V_i^-\right)$$ **total current**

$$P_i^+ = \left|a_i\right|^2$$ **power of incident wave**

$$P_i^- = \left|b_i\right|^2$$ **power of reflected wave**

$$\left|S_{1,1}\right|^2 = \frac{\left|b_1\right|^2}{\left|a_1\right|^2} = \frac{P_1^-}{P_1^+}$$

$$\left|S_{2,1}\right|^2 = \frac{\left|b_2\right|^2}{\left|a_1\right|^2} = \frac{P_2^-}{P_1^+}$$

$$\left|S_{i,j}\right| = \sqrt{\mathrm{Re}\left(S_{i,j}\right)^2 + \mathrm{Im}\left(S_{i,j}\right)^2}$$ **magnitude**

$$\left|S_{i,j}\right|_{dB} = 20 \cdot \log\left(\left|S_{i,j}\right|\right)$$ **magnitude in dB**

$$\angle S_{i,j} = \arctan\left(\mathrm{Im}\left(S_{i,j}\right) / \mathrm{Re}\left(S_{i,j}\right)\right)$$ **phase**

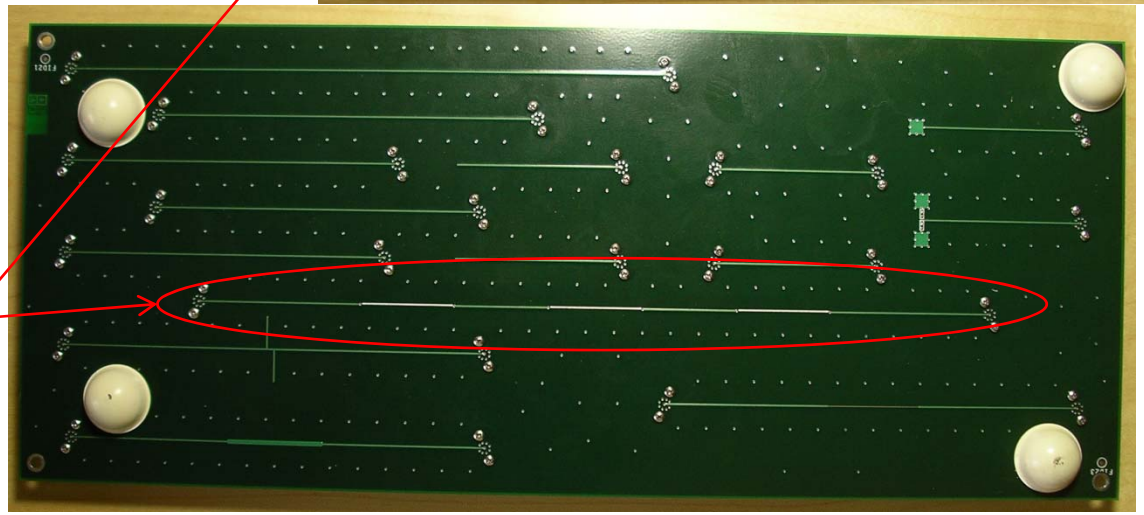
$$i = 1, 2; \quad j = 1, 2;$$

Minimal-reflection via-holes

- Minimal-reflection and maximal transmission and no resonances in the frequency band of interests
- Single-ended via-hole:
  - Reflection loss or S[1,1] is close to zero (below -20 dB)
  - Transmission coefficient S[2,1] is close to unit (close to 0 dB)
- Differential via-hole:
  - Reflection loss or S[D1,D1] via is close to zero (below -20 dB)
  - Transmission coefficient S[D2,D1] is close to unit (close the 0 dB)
- No via-hole stubs
- Distance between barrels and pads and anti-pads optimized to minimize the reflection – the result is the impedance controlled via

Small test board with non-localized vias

- SetB
  - Materials
    - "Copper", RR=1, SR=0.5
    - "FR4", Dk=4.1, LT=0.019, PLM=WD
    - "Vacuum"
    - "SolderMask", Dk=3.3, LT=0.02, PLM=WD
  - StackUp: LU=[mil], NL=4, T=63[mil]
    - 1| Medium: T=0.4, Ins="SolderMask"
    - 2| Signal: "Signal1", T=1.35, Ins="SolderMask"
    - 3| Medium: T=8.9, Ins="FR4"
    - 4| Plane: "Plane1", Mat="Copper", T=1.35, Ins="FR4"
    - 5| Medium: T=39, Ins="FR4"
    - 6| Plane: "Plane2", Mat="Copper", T=1.35, Ins="FR4"
    - 7| Medium: T=8.9, Ins="FR4"
    - 8| Signal: "Signal2", T=1.35, Ins="SolderMask"
    - 9| Medium: T=0.4, Ins="SolderMask"

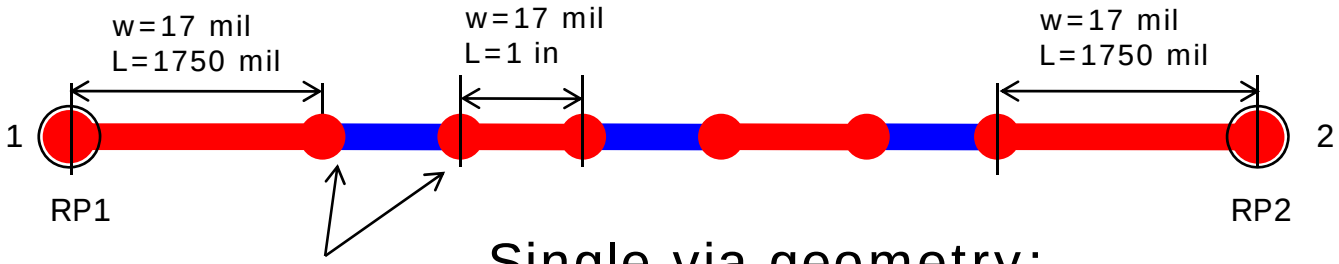


Channel with 6 single vias

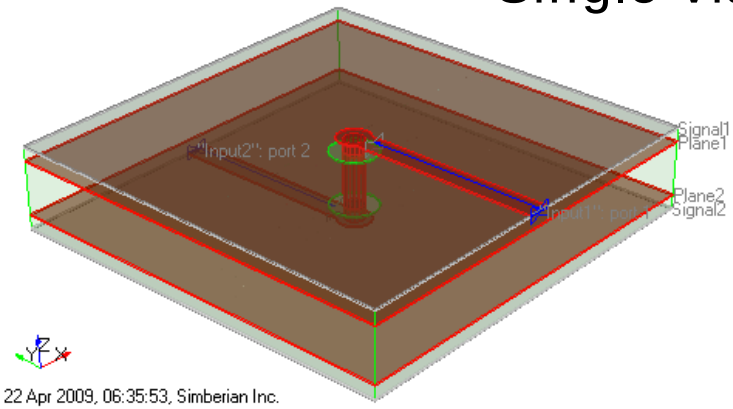
Designed and investigated by Teraspeed Consulting Group

Geometry of micro-strip channel with 6 vias without stitching vias

- 6 through via-holes without stitching vias, separated by 1 inch segments of 17 mil micro-strip line, de-embedded to reference planes RP1 and RP2



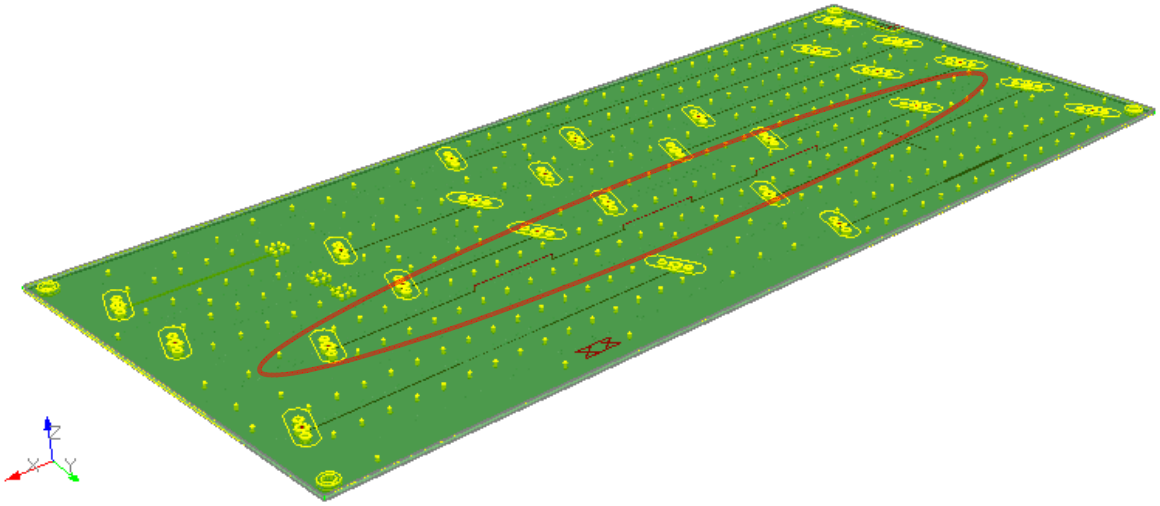
Single via geometry:

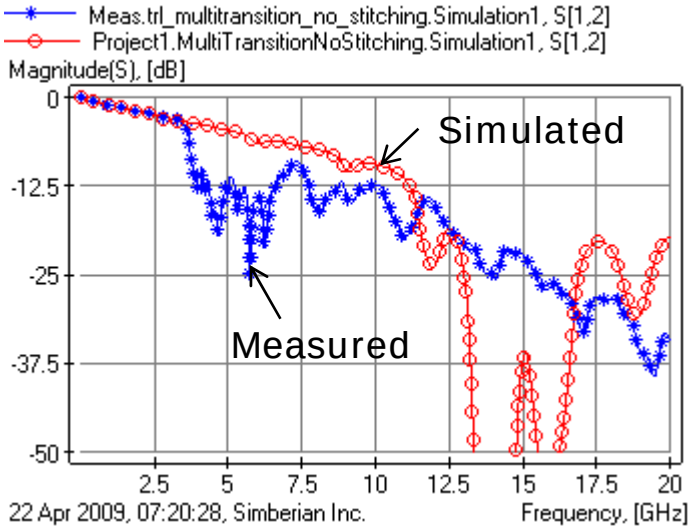


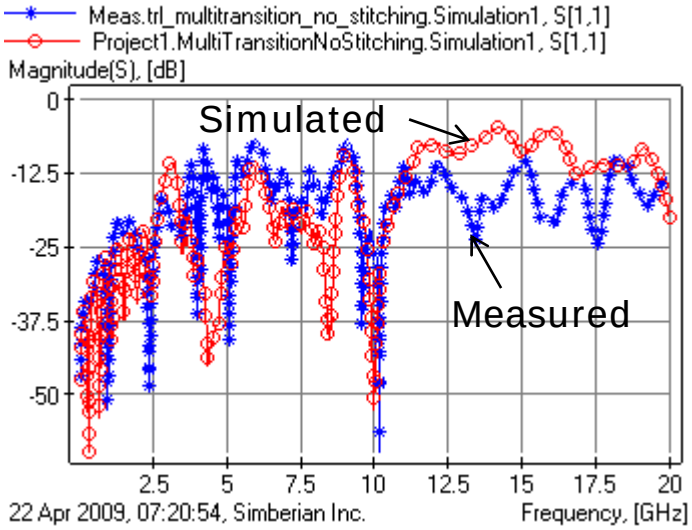
Top and bottom substrate: DK=4.1, LT=0.02 @ 1 GHz, T=8.9 mil
Core: DK=4.7, LT=0.02, T=39 mil
Diameter of all vias are 15 mil
Pad diameter for all via is 25 mil
Antipad diameter is 35 mil

S-parameters of micro-strip channel with 6 vias without stitching vias

The structure is not localizable and no correspondence at frequencies above 3 GHz (whole board must be simulated)



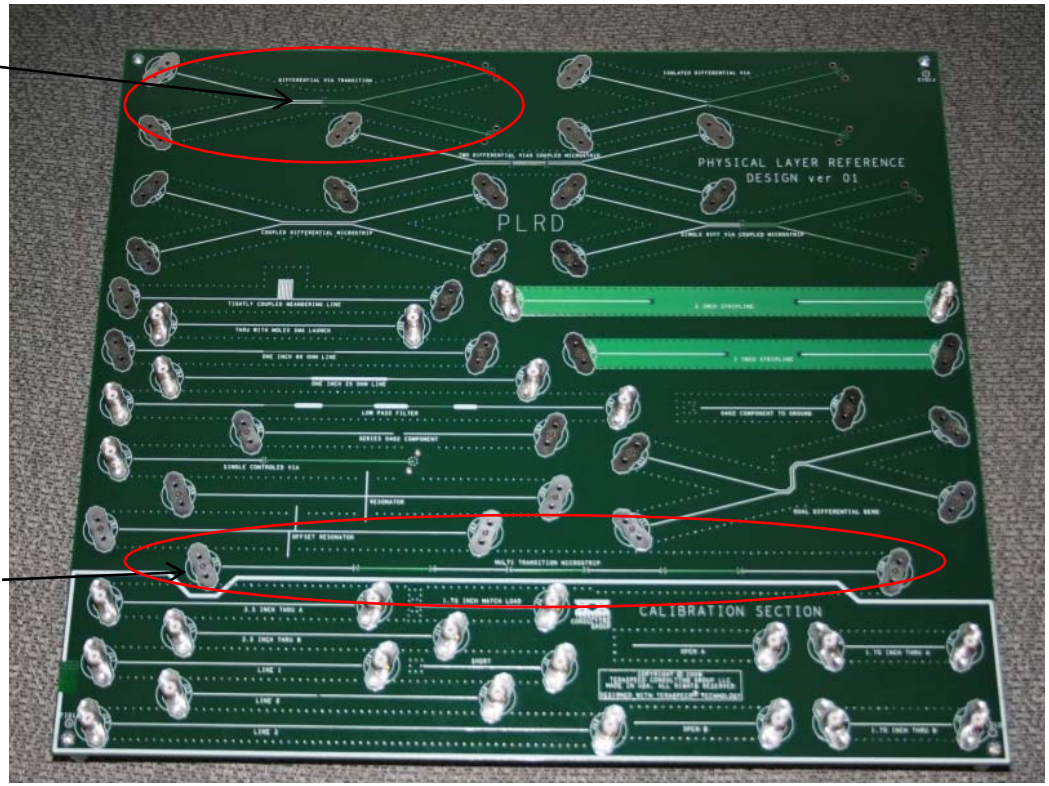




PLRD-1 Physical Layer Test Vehicle

- Micro-strip channel with 6 single-ended vias with stitching vias and differential vias are used as examples here

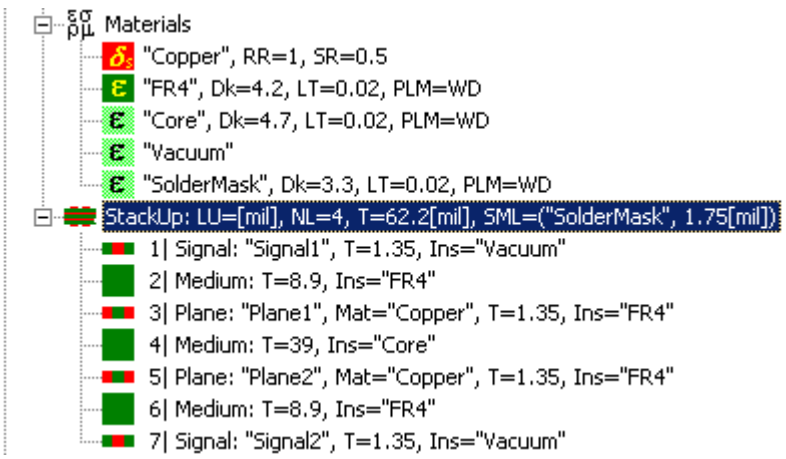
Differential vias

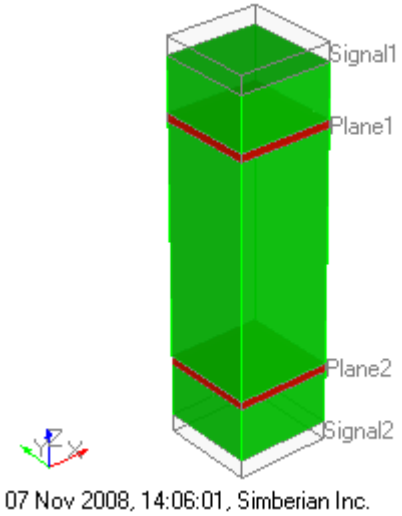


Channel with 6 single vias

Designed and investigated by Teraspeed Consulting Group – available for independent evaluation

Step 1: Materials and Stackup

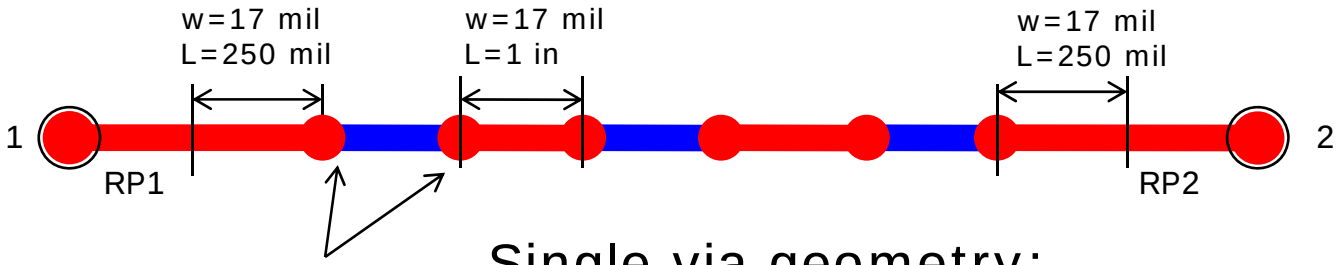




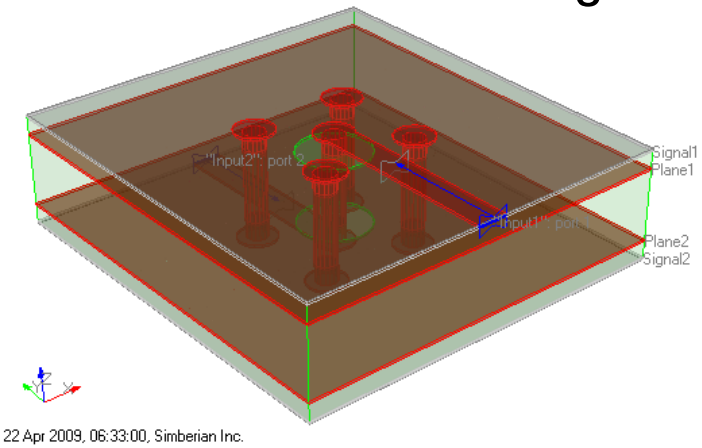
- **Start with properties provided by board vendor**:
  - Copper bulk resistivity 1.724e-8 Ohm meters, roughness 0.5 um (roughness factor 2 is guessed)
  - Solder mask: DK=3.3, LT=0.02
  - FR-4 core dielectric: DK=4.7, LT=0.02
  - **FR-4 dielectric between signal and plane layers: DK=4.0 – 4.25, LT=0.02 – extracted on the base of measurements and simulations**
  - Measurement frequency for all dielectrics is guessed to be 1 GHz

Geometry of micro-strip channel with 6 localized vias (with stitching vias)

- 6 through via-holes with 4 stitching vias, separated by 1 inch segments of 17 mil micro-strip line, de-embedded to reference planes RP1 and RP2



Single via geometry:

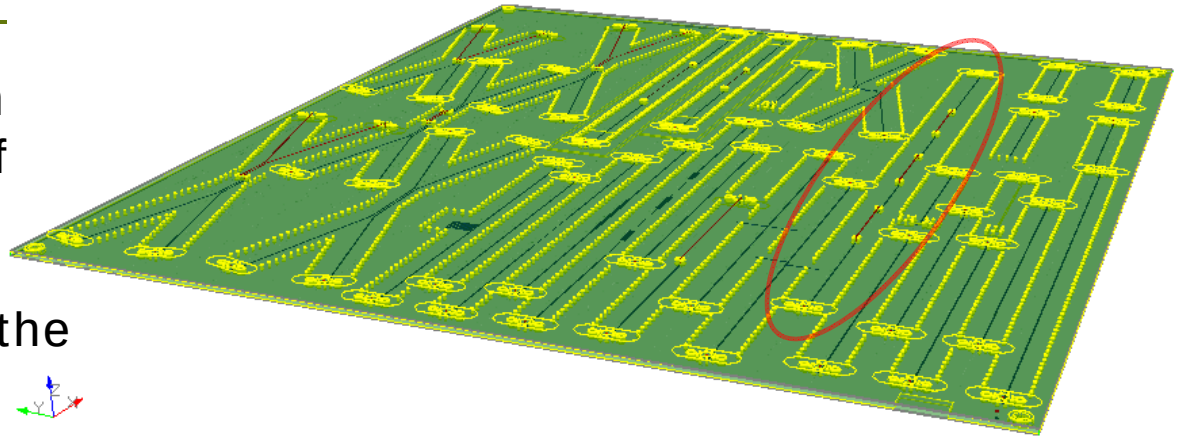


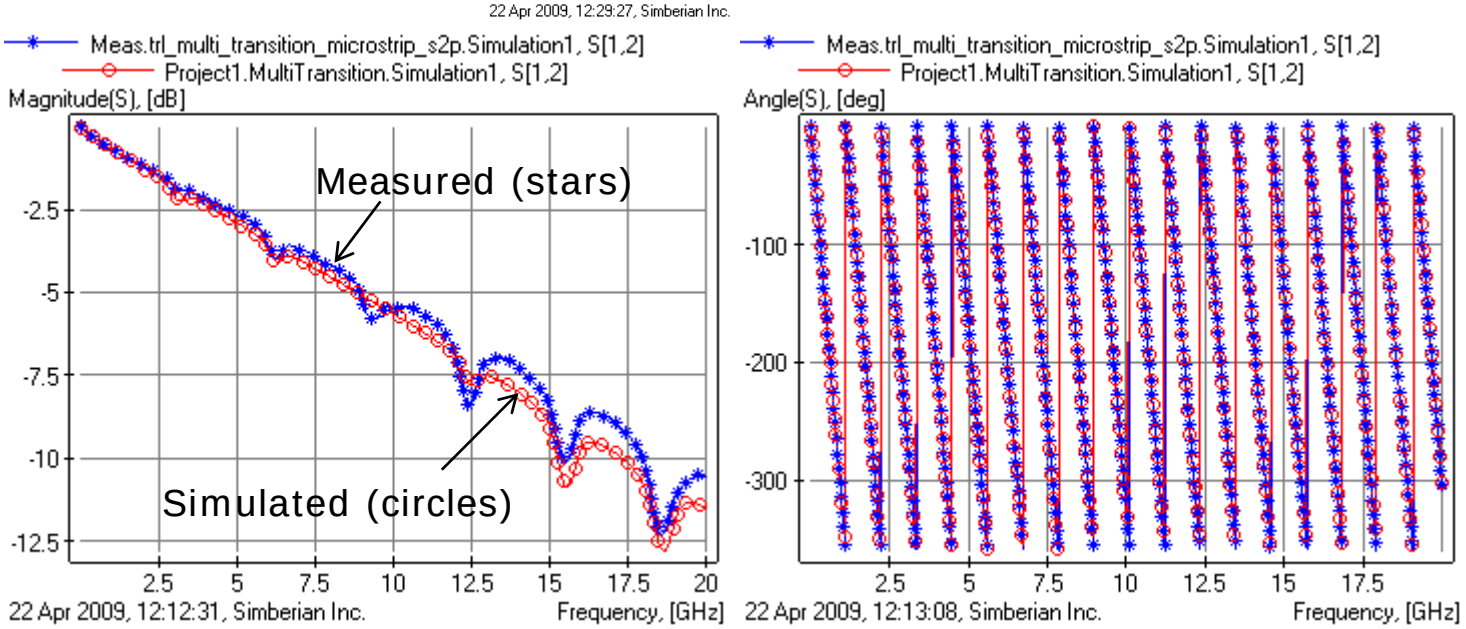
Top and bottom substrate: DK=4.0, LT=0.02 @ 1 GHz, T=8.9 mil
Core: DK=4.7, LT=0.02, T=39 mil
Diameter of all vias are 12 mil
Pad diameter for all via is 22 mil
Antipad diameter is 40 mil
Distances between signal and stitching vias are 40 mil

Geometry is synthesized with Simbeor 2008 to minimize the reflection

S-parameters of micro-strip channel with 6 localized vias

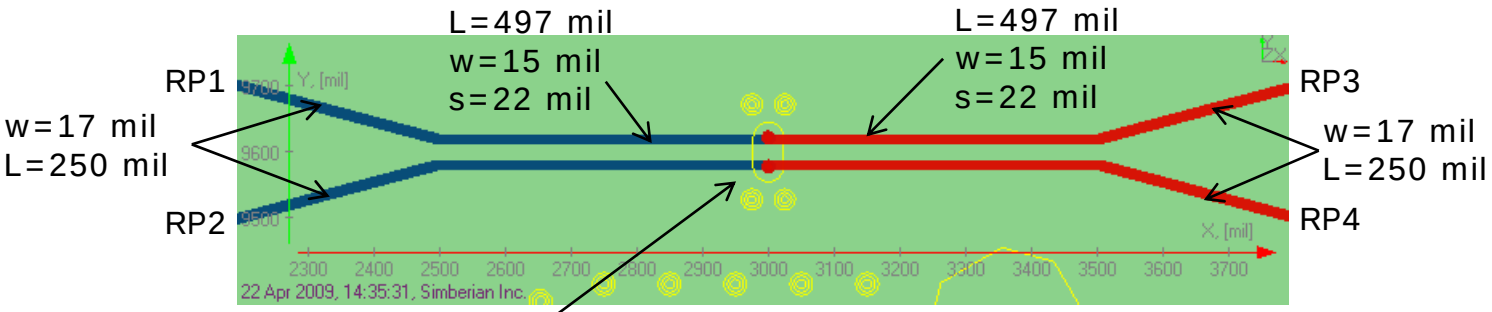
Good correspondence in magnitude and phase of the transmission coefficient (though reflection was larger in the experiment)

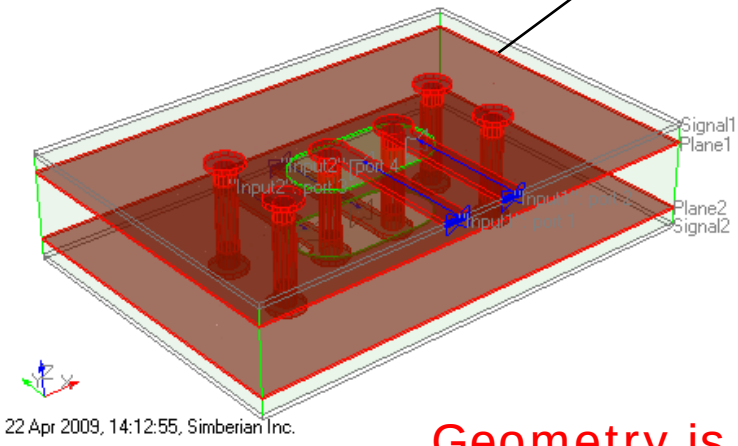




Differential via-holes

- Differential via-holes with 4 stitching vias connecting two differential micro-strip lines, de-embedded to reference planes RP1-RP4



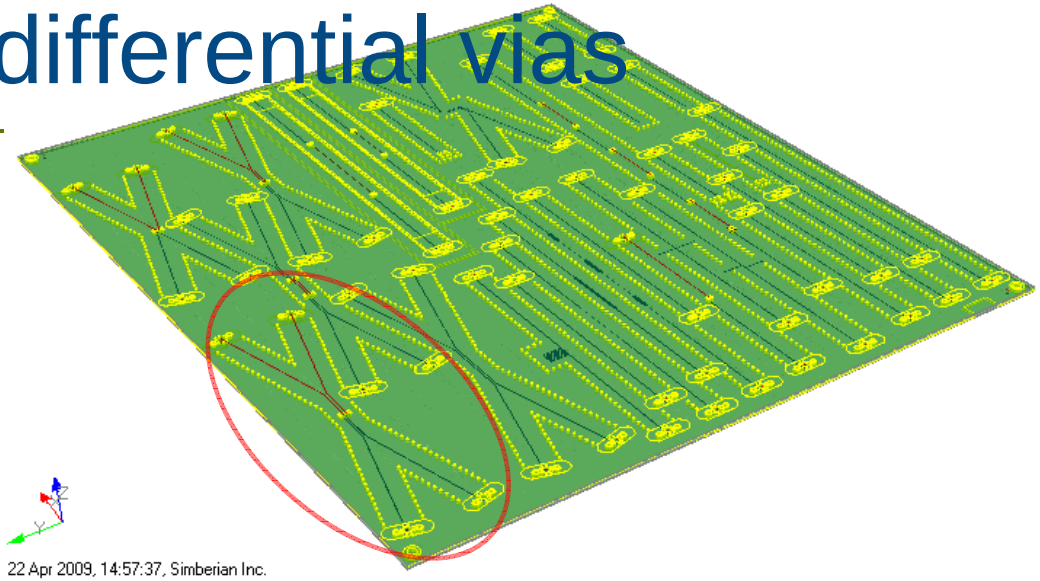


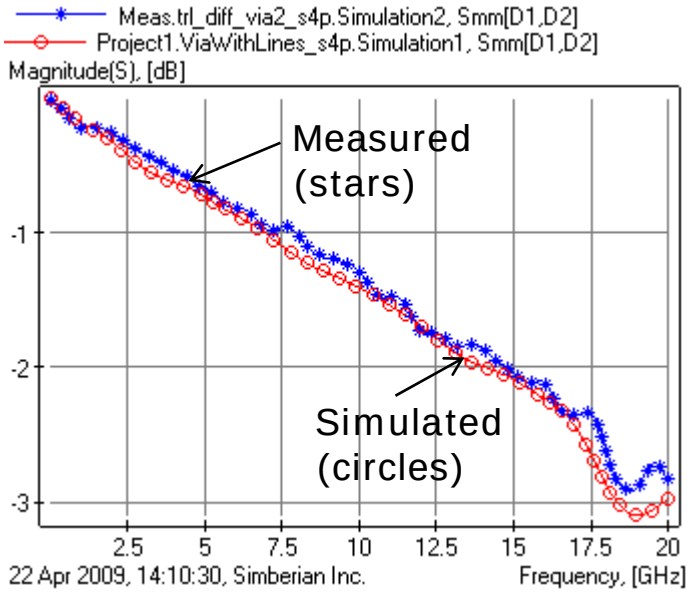
Substrate DK=4.25, core DK=4.7,
LT=0.02 @ 1 GHz
15 mil strips separated by 22 mil
Diameter of vias is 12 mil
Diameter of pads is 22 mil
Distance between vias 44 mil
Oblong anti-pad 46 by 90 mil

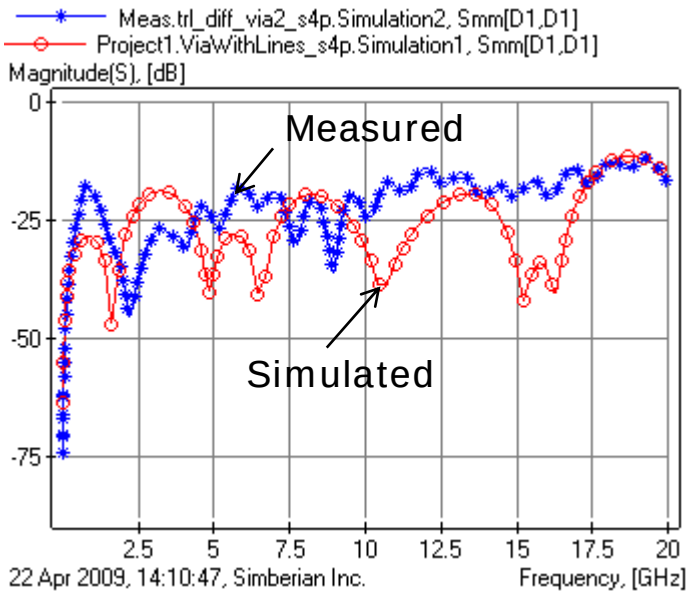
Geometry is synthesized with Simbeor 2008 to minimize the reflection

S-parameters of differential vias

Good correspondence in magnitude of the transmission and reflection coefficients between Simbeor model and measurements







Conclusion – Select the right tools to optimize and build via-hole models

- Distinguish localizable and non-localizable cases
  - Dependence of S-parameters from the boundary conditions usually shows that the problem is non-localizable
- Only localizable cases can be analyzed with a 3D full-wave solver such as Simbeor 2008
  - Single-ended via or differential vias with stitching vias nearby
  - Differential mode propagation in differential vias without stitching vias
- **Only localizable via-holes can be safely used as components of multi-gigabit data channels**
- Complete board analysis is required to build accurate models for non-localizable cases – possible but not practical

Solutions and contact

- Setting up all simulations and analysis took about 2 hours
- Simbeor solution file used to illustrate these notes is available for download from Simberian web site
  - http://www.simberian.com/AppNotes/Solutions/DesigningLocalizableMinimalReflectionVias_2009_05.zip
- Send questions and comments to
  - General: info@simberian.com
  - Sales: sales@simberian.com
  - Support: support@simberian.com
- Web site www.simberian.com