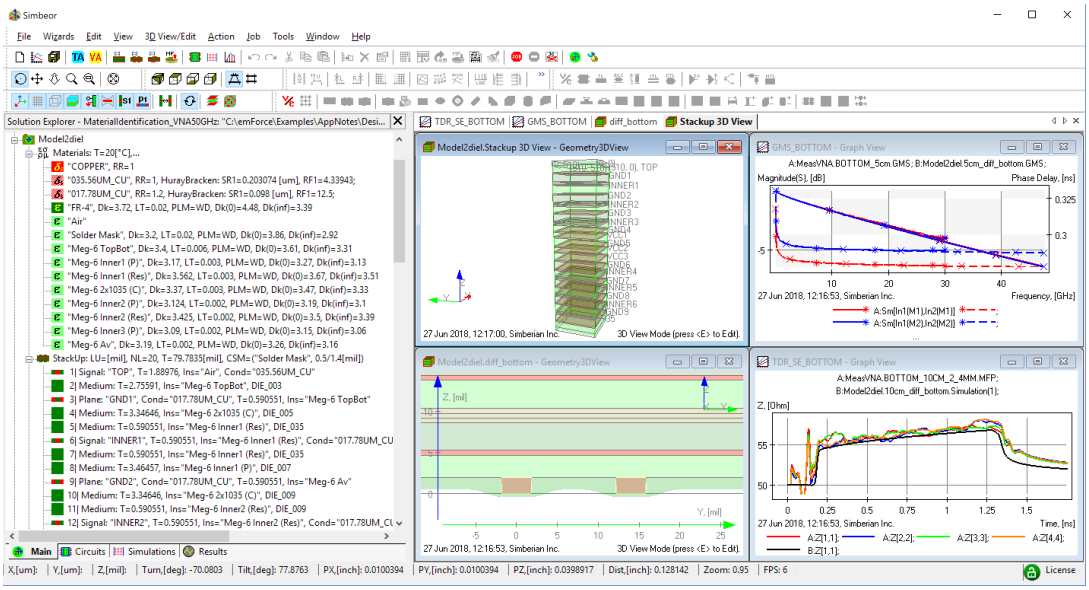
Advanced stackup planning with impedance, delay and loss validation

Yuriy Shlepnev, Simberian Inc.
First published at LinkedIn on June 28, 2018



A typical printed circuit board (PCB) design usually starts from the material selection and stackup definition – this is the stackup planning or design exploration stage. **How reliable are the data provided by the material vendors and PCB manufacturers? Can we use these data to predict trace width and spacing for the target trace impedance or to calculate delays or evaluate the loss budget?** PCB routing is usually done with these preliminary data. The actual stackup may be further adjusted by the PCB manufacturer together with the trace widths and spacing, to have the target impedances. This is typical impedance controlled process that is well established and usually produces acceptable outcome. **But, what about the losses? Can we use preliminary data to evaluate the losses and loss-related compliance metrics? Or can we just specify the target losses and rely on the manufacturers as it is done for the impedance?** Let's try to answer these questions. As an example with the preliminary and final data, EvR-1 validation board is used here – all data for this board are provided by Marko Marin from Infinera. This board was featured in our award-winning "Expectation vs. Reality" paper [1]. We will use Simbeor software as the stackup exploration tool here, to evaluate the accuracy of the characteristic impedance, delay and losses. **Simbeor is selected for the stackup exploration because of it is systematically validated with the measurements up to 50 GHz [2].**

When it comes to the stackup planning, the first step is to select a PCB manufacturer, have possible selection of the materials and define the stackup structure. In our case, the validation board has 20 layers with 8 layers assigned for the high-speed signals as shown in Fig. 1. Low-loss Panasonic Megtron6 laminate is selected to rout the high-speed interconnects. The target impedance has been specified for

the PCB manufacturer and the manufacturer provided expected stackup structure and trace widths and spacing adjustments to fulfil the target impedances [1]. This is the usual case for a production board. According to the manufacturer, the expected impedance variations should be within 8%. That is too large to expect excellent correlation up to 30 GHz for 28 Gbps NRZ links, but may be acceptable. The board manufacturer provided stackup geometry as shown in Fig. 1 on the left and corresponding stackup entered for the pre-layout analysis into Simbeor software is shown in Fig. 1 on the right side. Megtron6 specs provide dielectric constant and loss tangent at multiple frequencies – just one frequency data can be used to define causal wideband Debye model. The values for Dk in the Fig. 1 are slightly different from the Megtron6 specs and are provided by the PCB manufacturer based upon their experience with this material.

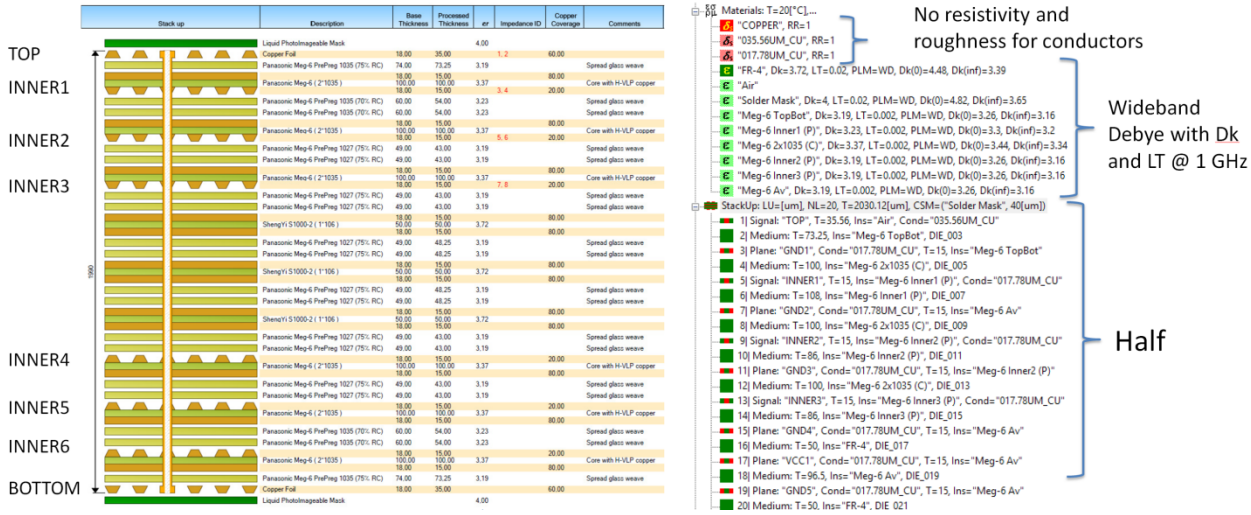


Fig. 1. EvR-1 validation board stackup from PCB manufacturr (left) and the initial material models and exactly the same stackup in Simbeor software defined for pre-manufacturing analysis (right).

The major problem here is with the conductor roughness models – all we know that the copper foil roughness is specified as H-VLP and no other data. PCB manufacturer also roughens the shiny side of the copper foil during the board manufacturing, without any parameters for the electrical modeling. **Even if we would have data for the mate side of the copper foil from the copper foil manufacturer, the PCB manufacturer treatment of the shiny side makes it practically useless.** Thus, we start the stackup exploration without the conductor roughness model and with the trace adjustments provided by the PCB manufacturer. The rest of the EvR-1 validation board design is covered in details in [1]. To validate the preliminary data we will use 10 cm differential links in strip layer INNER1 and microstrip layer BOTTOM (see Fig. 1). The results of the first experiment are shown in Fig. 2. Left graphs show measured TDRs – the response is computed with S-parameters measured up to 50 GHz. TDRs for 10 cm segments of the transmission line model computed in Simbeor are also shown on the same graphs for comparison.

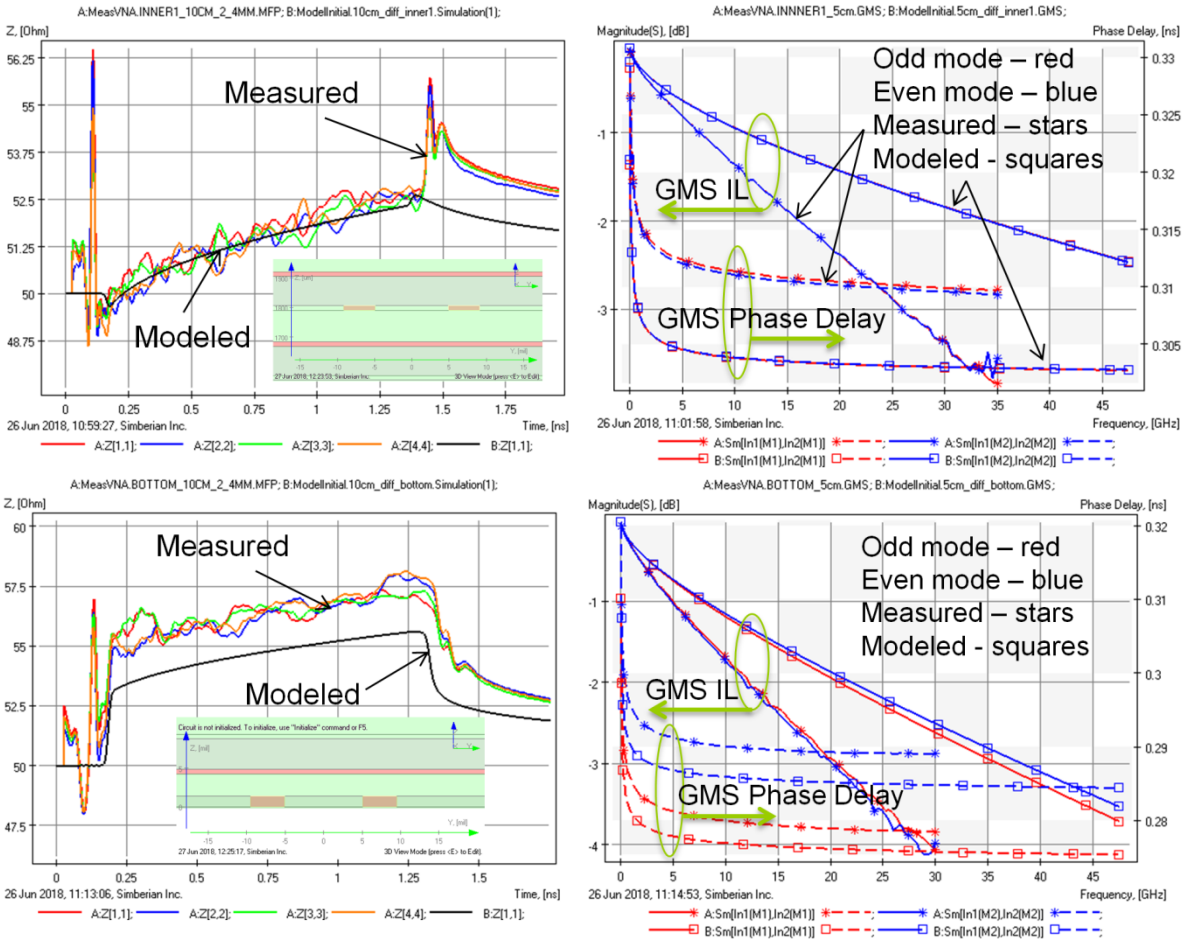


Fig. 2. TDR of 10 cm differential links measured and computed (left graphs) and GMS insertion loss (IL) and phase delay for 5 cm differential line segments measured and computed (right graphs) with the stackup structure and material parameters from the PCB manufacturer for layer INNER 1(top graphs) and for layer BOTTOM (bottom graphs).

We can see acceptable TDR correlation for the strip line, **but computed impedance of the microstrip line is substantially lower.** The models for these preliminary comparisons do not have the launches. Right graphs in Fig. 2 show correlation between the Generalized Modal S-parameters (GMS-parameters) measured and computed for 5 cm segment of the differential lines. GMS-parameters are reflection-less transmission parameters – the reflection losses are completely removed in Simbeor software. **That makes this type of S-parameters ideal for precise material parameters identification and model quality evaluation.** From GMS-parameters we can observe that the model delays are off by less than 2 ps/inch. **The most important is the obvious difference in the losses** – the difference is already substantial at 5 GHz (about 20%) and may be totally un-acceptable at 30 GHz (about 50%).

So, why do we see such discrepancies between the measurements and models? For the losses, it is quite obvious **- we do not have any data at the stackup exploration stage to specify a conductor roughness models. If such models are used to compute compliance metrics, this can lead to complete design failure!** Note that this is not just the problem with the losses – it also affects such metric as the insertion

loss to power sum cross-talk metric (ICR). Considering differences in the impedances and delays, it is either differences in geometry of the cross-sections or in the parameters of the dielectrics or both – we will find out soon. To make it more complicated, note that the conductor roughness increases the inductance of the traces and can substantially change both the impedance and phase delay in addition to the losses [3]. All that must to be included in the transmission line model. Also, simple adjustment of the model parameters (geometry or dielectric properties) will not work - too many parameters to play with and a systematic approach is needed. Fortunately, with Simbeor software the parameters of the dielectric and conductor roughness models can be separately identified in the systematic way. It can be done with the S-parameters measured for two line segments and converted into either GMS-parameters, or into complex propagation constants (Gamma). Both GMS-parameters and Gamma can be used in Simbeor to identify the material properties with the separation of the losses between the dielectric and conductor roughness [4]. **For the accurate and unique identification, the geometry of the transmission lines in the test structures must be measured from the cross-sections.** EvR-1 board was cross-sectioned and investigated. The final trace widths and separations with an example of the cross-sections are shown in Fig. 3.

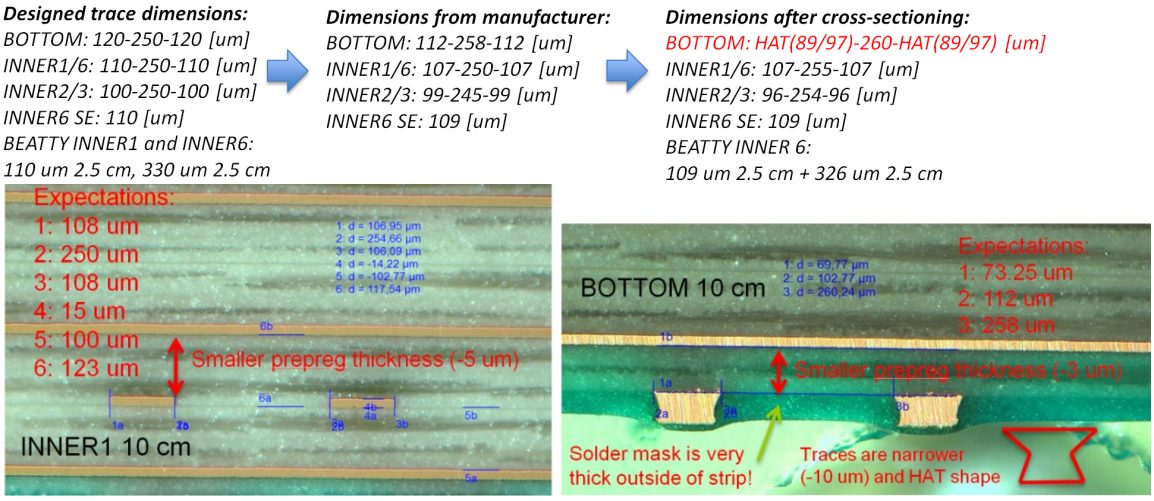


Fig. 3. Final trace geometry adjustments and example of the cross-sections of differential test links in INNER1 and BOTTOM layers (expectations are data from PCB manufacturer).

What we can learn from this is that the trace widths and space adjustments from this particular PCB manufacturer were acceptable only for the strip lines. However, the geometry of the microstrip traces in the BOTTOM or TOP layers are completely different from the data provided by the manufacturer. That is why we observe more differences in TDR of the microstrips in Fig. 2. See more observations and the material identification step details and references in [1].

The final stackup with all geometry adjustments from the microphotographs and dielectric and conductor roughness models identified with Simbeor software is shown in Fig. 4. To ensure the accuracy, we have 8 dielectric models - one for the core dielectric, four for the prepreg layers, one for solder mask dielectric and two optional for the resin-reach layers surrounding the strips in the interior layers. The resin-reach layers are required only in cases when test structures have some far end crosstalk (FEXT) and it has to be accounted for in the model. Dielectric constants and loss tangents from

the PCB manufacturer are shown in brackets in Fig. 4 for comparison. In addition to the dielectrics, two conductor roughness models are identified – there is nothing to compare it with. The analysis to measurement correlation with all that adjustments and material models are shown in Fig. 5. Comparing to the results with the data from PCB manufacturer shown in Fig. 2, the correlation is much better. Though, it is not perfect due to the expected manufacturing variation and possibly other unknown reasons that we may further discover. With this new stackup, both pre- and post-layout analysis can be done with high confidence as demonstrated in [1] and [2].

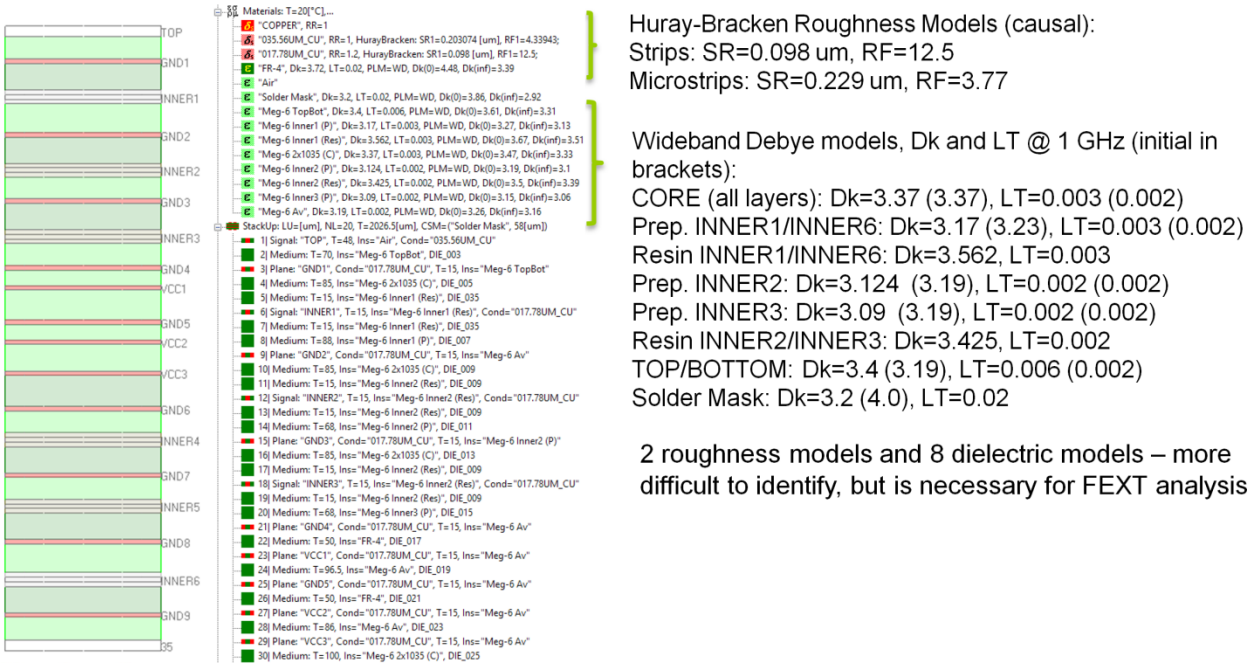


Fig. 4. The final stackup structure and dielectric and conductor roughness models.

The bottom line is that the stackup data provided by a PCB manufacturer must be validated. Data for strip line layers from this particular manufacturer were basically acceptable for the preliminary analysis of the impedances and delays in the strip lines. Though, data for the traces in the surface layers (microstrips) were not acceptable to do any analysis. **The most troubling was absence of models or any useful data to build conductor roughness models – any investigation of the losses would be completely useless without such models.** Thus, any stackup exploration or planning stage must include building small validation boards or test coupons to verify the data obtained from the PCB manufacturer and to identify actual geometry adjustments and the conductor roughness models. The coupons should have two segments of transmission line (single-ended or differential) with different lengths per each layer with unique dielectric. The coupons must be cross-sectioned after S-parameters of the line segments are measured. **This is the most important step of the systematic approach to design predictable interconnects.**

Simbeor software was used for all computations provided in this paper. All corresponding Simbeor solutions are available upon request to learn the “sink or swim” process. Moreover, Simberian team can help you to establish all elements of the systematic approach to design predictable interconnects.

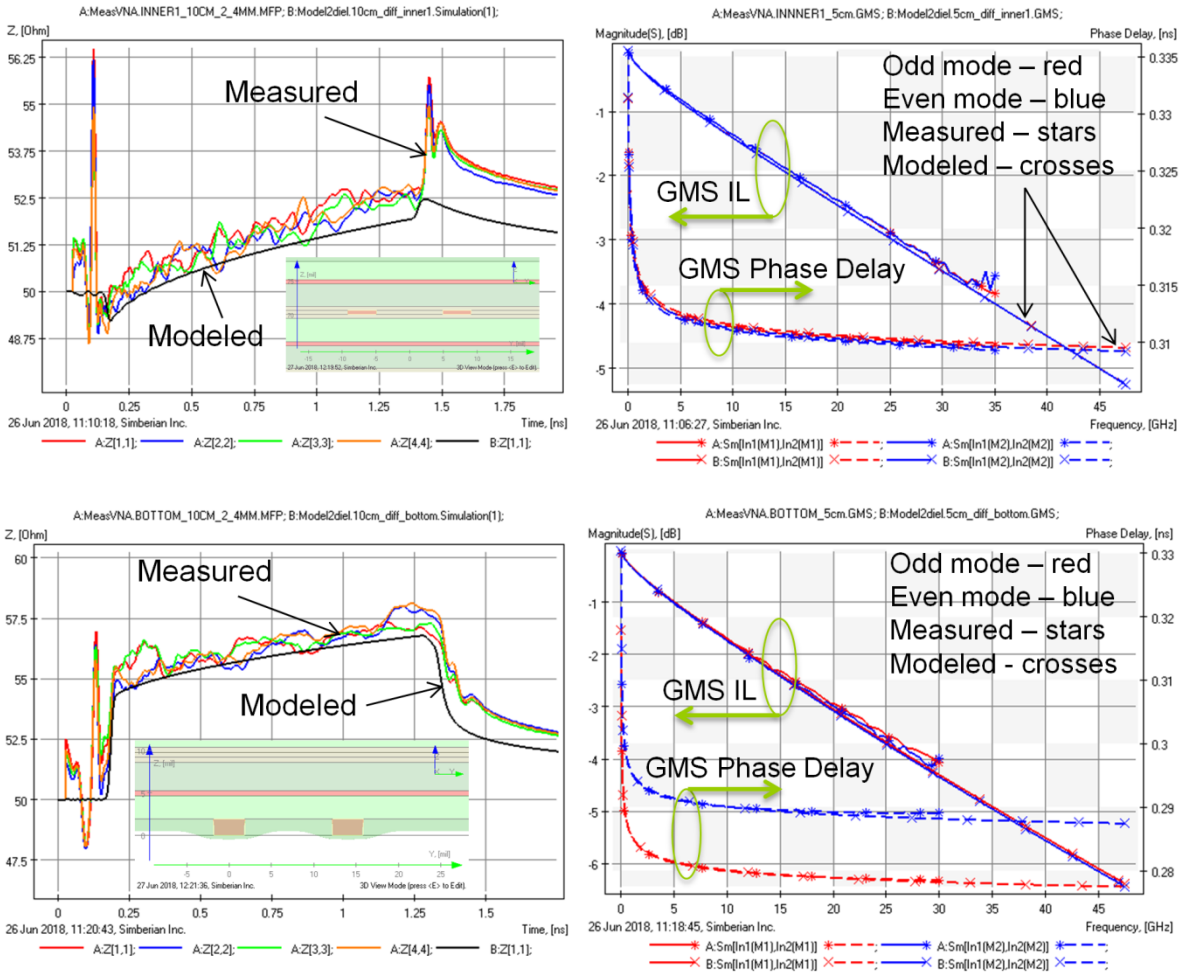


Fig. 5. TDR of 10 cm differential links measured and computed (left graphs) and GMS insertion loss (IL) and phase delay for 5 cm differential line segments measured and computed (right graphs) with the identified stackup structure and material models for layer INNER 1(top graphs) and for layer BOTTOM (bottom graphs).

1. M. Marin, Y. Shlepnev, 40 GHz PCB Interconnect Validation: Expectation vs. Reality, DesignCon2018, January 31, 2018, Santa Clara, CA. - **the award-winning paper from DesignCon2018**. Presentation with complete report **is also available here.**
2. Y. Shlepnev, **Sink or swim at 28 Gbps**, The PCB Design Magazine, October 2014, p. 12-23.
3. Y. Shlepnev, Unified approach to interconnect conductor surface roughness modelling, 2017 IEEE 26st Conference on Electrical Performance of Electronic Packaging and Systems (EPEPS2017), October 15-18, 2017, San Jose, CA.
4. Y. Shlepnev, Broadband material model identification with GMS-parameters, 2015 IEEE 24st Conference on Electrical Performance of Electronic Packaging and Systems, October 25-28, 2015, San Jose, CA.