DesignCon 2014

Lessons learned: How to Make Predictable PCB Interconnects for Data Rates of 50 Gbps and Beyond

Wendem Beyene, Rambus Inc.
wbeyene@rambus.com

Yeon-Chang Hahm, Rambus Inc.

Jihong Ren, Rambus Inc.

Dave Secker, Rambus Inc.

Don Mullen, Rambus Inc

Dr. Yuriy Shlepnev
shlepnev@simberian.com

Abstract

Design of PCB interconnects for data channels running at bitrate *50 Gbps* and beyond is a very challenging problem that requires analyses and measurements over extremely broad frequency bandwidth from *DC* to *50 GHz* and above. This paper shares our experience in building a practical methodology to make predictable *50 Gbps* interconnects models. Substantial part of interconnects can be simulated with transmission line models that require identification of causal broadband dielectric and conductor roughness models. It is shown that separation of losses between the conductor roughness and dielectric models is essential element of such identification. Examples of proper and improper material models identification and consequences are provided in the paper. Accurate prediction of interconnect behavior also requires localization and *3D EM* analysis for all transitions or discontinuities. Examples of optimized interconnects designed for *50 Gbps* channels and the validation with measurements are also provided.

Author(s) Biography

Wendemagegnehu (Wendem) T. Beyene received his B.S. and M.S. degrees in Electrical Engineering from Columbia University, in 1988 and 1991 respectively, and his Ph.D. degree in Electrical and Computer Engineering from University of Illinois at Urbana-Champaign, in 1997. In the past, he was employed by IBM, Hewlett-Packard, and Agilent Technologies. He is currently a technical director at Rambus Inc. where he is responsible for signal and power integrity of multi-gigabit serial and parallel interfaces.

Yeon-Chang Hahm received his M.S. and Ph.D. degrees in Electrical and Computer Engineering from Oregon State University in 1997 and 2000 respectively. His academic research area focuses on computing distributed elements of on-chip interconnects and modeling. After receiving his degree, he joined IBM, AMD consecutively and worked on SI/PI area for 12 years. He is currently a Principal Engineer at Rambus Inc. responsible for electrical modeling of on-board & on-package passives as well as SI simulations of high-speed serial and parallel signals.

Jihong Ren received her PhD degree in Computer Science from University of British Columbia, Vancouver, Canada in 2006, where she worked on optimal equalization for chip-to-chip high-speed buses. She is currently a Senior Manager at Altera, managing the SerDes IO architecture group. Prior to Altera, she was with Rambus Inc., managing the Signal Integrity and Power Integrity team. She authored and co-authored more than thirty papers, four book chapters and filed 14 patent applications in high-speed communications area. She was awarded the silver Distinguished Inventor award from Rambus in 2010.

Dave Secker is currently a Technical Director in Systems Engineering at Rambus Inc., where he has been for the past 17 years. His responsibilities include physical design, modeling and optimization of high-speed signal interconnect and power delivery

networks at the IC package and system board levels. Previously he worked at Los Alamos National Laboratory as a research assistant. Mr. Secker received his M.S. degree in Electrical and Computer Engineering from The University of Arizona in 1996.

Don Mullen is currently a Senior Principal Engineer at Rambus Inc., focusing on systems packaging, mechanical, and thermal design; he has been at Rambus for the past 15 years. Prior to Rambus, he held various engineering positions involving electronic packaging, thermal design, biomedical engineering, and mechanical systems engineering design. He has a BSME (’70) and is a registered professional engineer in California..

Dr. Yuriy Shlepnev is President and Founder of Simberian Inc., where he develops Simbeor electromagnetic signal integrity software. He received M.S. degree in radio engineering from Novosibirsk State Technical University in 1983, and the Ph.D. degree in computational electromagnetics from Siberian State University of Telecommunications and Informatics in 1990. He was principal developer of electromagnetic simulator for Eagleware Corporation and leading developer of electromagnetic software for simulation of signal and power distribution networks at Mentor Graphics. The results of his research are published in multiple papers and conference proceedings.

Introduction

The need for high bandwidth links continue to grow to meet the demand of high performance computing, data centers, servers and storages driven by internet in general and multi-core memory and processors architectures in particular [1]. The high bandwidth necessitates a large increase in the interface data rate and width.

In the past, the growth of data rate has been sustained by increasing the performance of the input/output (I/O) circuits and the use of more complex equalization, complicated coding and modulation and other signal processing techniques. Subsequently, the electronic and I/O power consumption significantly increases with increasing the interface speed. Thus, the link data rate increase cannot only come from circuit design and performance improvements.

The passive channel, printed circuit board (PCB) on which the electronic components are based on, impose limitation on the supported speed. In today's backplane, the maximum capability of the copper backplane determines the performance of the system. Starting with high-end systems, the transfer from copper backplane to an optoelectronic backplane has been anticipated for a while. Even though, the gap between optical and electrical interconnects are reducing in terms of component cost, and manufacturability, electrical interconnect have still been cost and power efficient solutions for backplane links at present time. To improve and extend the reach of copper-based interconnects, several improvement have been suggested to high-speed channel using low-loss dielectric, smooth copper surfaces, improved connectors and packages [2]-[3].

The viability of a copper based interconnect systems utilizing advanced connectors, packages, and boards with low-loss laminates are not anymore in doubt for data rate of *25 Gbps* [4]. In order to enable higher data rate links, for *100 Gb/s* Ethernet routers and switches and other high-end systems, backplane serial links with data rates beyond *25 Gbps* are been standardized using copper-based interconnects using low-loss boards [5]. There are proposals for the next generation standards of electrical signaling to run at several data rates beyond *50 Gbps* across low-loss board over *0.5 m* long and cables over *1 m* long.

The design of interconnect that support data rate exceeding *50 Gbps* is necessary to support Terabit backplane systems. In order to predict and optimize the performance of high-speed links operating at *50 Gbps* and beyond, it is essential to accurately model and characterize the interconnect systems. The models of interconnects have to be broadband and include high frequency effects that were not critical at that data rates in the range of *10* to *20 Gbps* [6]. For higher data rates, very careful modeling of signal propagation in PCB and package traces requires proper identification of the conductor and dielectric frequency-dependent properties over extremely wide frequency band. In addition, 3D modeling and characterization of transition structures are essential to understand and optimize the wave propagation and minimize mismatch across various transition structures such as via and BGA at the interface between package and PCB.

Low-loss laminates such Megtron 6 from Panasonic, FR408HR from Isola Group, and Nelco 4000-13 EPSI from Park Electrochemical Corp. are expected to be key enablers to design boards to run at higher data rates. These laminates offer much more stable dielectric characteristics and have considerably less loss at high frequencies. To investigate the effect of low-loss laminates and see the impact of surface roughness, dielectric properties, glass weave effects, several boards with Megtron 6 with Hyper Very Low Profile (HVLP) finish and Reverse-Treated Foil (RTF) finish, Nelco 4000-13 EPSI with RTF copper foil and standard glass weave, Isola FR408HR with RTF copper foil and standard glass weave. Table I shows typical electric properties of these low-pass laminates that are studied in this paper and of typical FR-4 board for comparison. Figure 1 shows the photo of some of the boards designed to characterize the traces and the dielectrics.

Table I: Electrical properties (dielectric constant, loss tangent or dissipation factor, and amplitude of surface roughness of laminates studied.

Laminate Types	Dielectric Constant	Dissipation Factor	Amplitude of Surface Roughness
Megtron 6 HVLP	3.6	0.004	1.5 – 2.0 um
Megtron 6 RTF	3.6	0.004	7.0 – 8.0 um
Nelco N4000-13 EPSI	3.2	0.008	7.0 – 8.0 um
FR408HR	3.65	0.0095	7.0 – 8.0 um
Typical FR-4	4.3	0.02	7.0 – 8.0 um

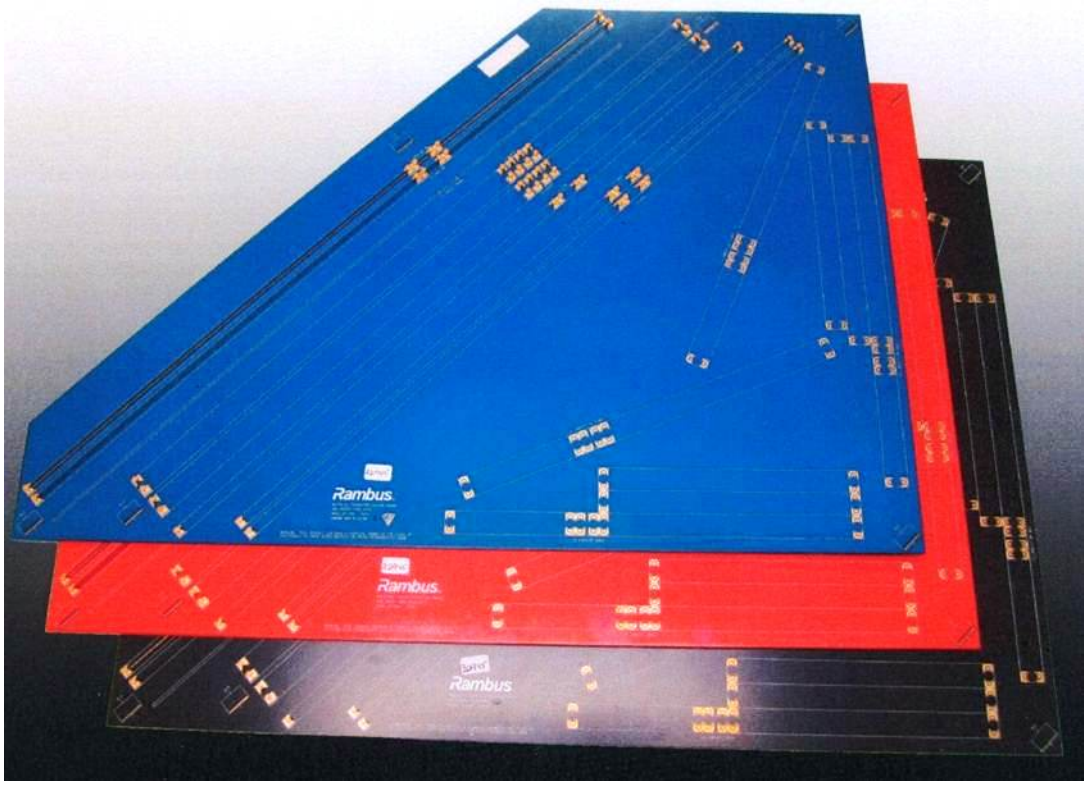


Figure 1: Some of the boards designed for material characterization showing locations of probe pads and MMPX connectors.

Several structures including microstrips and striplines of various lengths with probe pads and connectors were designed. Additional structures were also included on the board to improve and minimize de-embedding procedures. The pad to pad links of two set of differential nets of *6-in.* and *12-in*. long striplines, shown in Figure 2, are used to characterize the low-loss materials and traces.

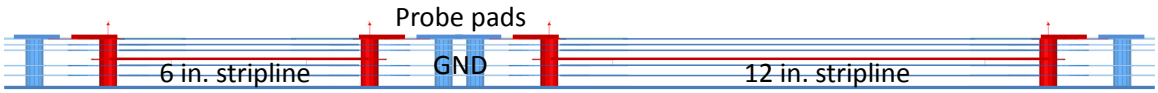


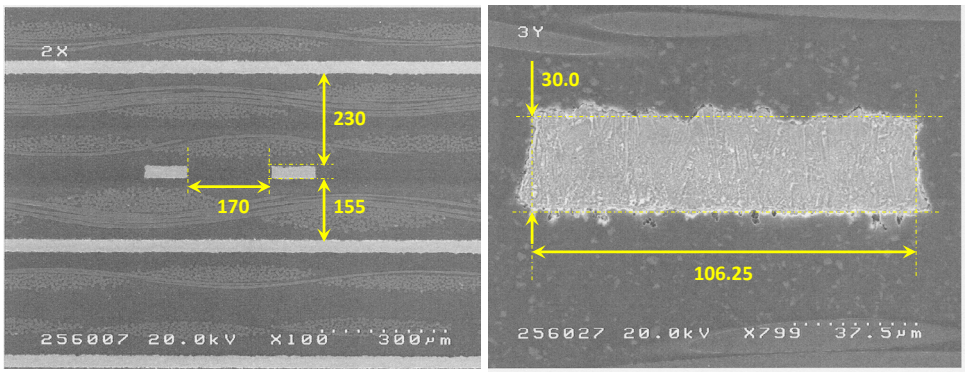
Figure 2: The cross-section of the 8-layer board with *6 in.* and *12 in.* striplines designed on the 4th layer and the launch structures.

The stackup of the boards, the glass type, the material family, the dielectric constant at *1 GHz* and the thickness of the layers are summarized in Table II. The material properties and dimensions are provided by the manufacturer as typical values and need to be verified for the specific boards manufactured for these experiments.

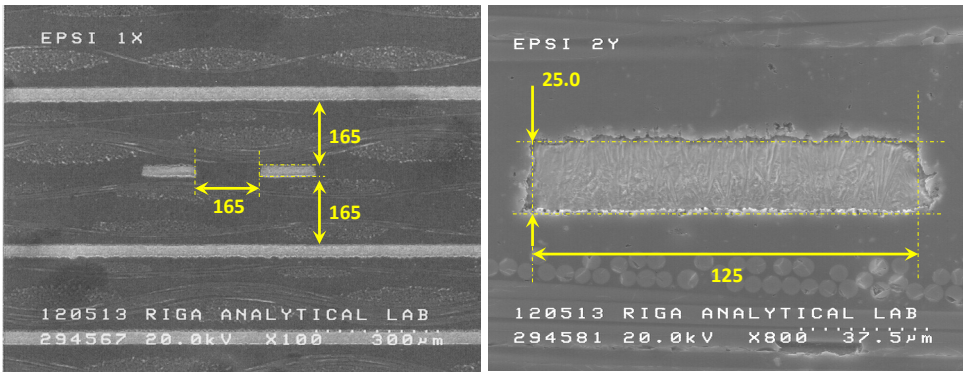
Table II: Layer stackup, glass types, dielectric constant at 1 GHz, and thickness for Megtron 6, Nelco N4000-13EPSI, and FR408HR boards.

Stackup	Segment	Glass type			Dielectric Constant			Thickness (mil)		
		MEG 6	EPSI	FR408HR	MEG 6	EPSI	FR408HR	MEG 6	EPSI	FR408HR
	Mask							0.8	0.8	0.8
L1	Foil							1.6	1.6	1.6
	Prepreg	1035(70)	1080(65)	1080(65)	3.35	3.2	3.46	5.37	5.12	5.52
		1078(72)	1080(65)	1080(65)	3.3	3.2	3.46			
L2								1.2	1.2	1.2
	Core	1-3313	1-2116	1-2116	3.71	3.38	3.7	3.9	5.00	5.00
L3								1.2	1.2	1.2
	Prepreg	3313(54)	106(75)	2116(55)	3.71	3.11	3.68	6.56	5.88	9.08
		3313(54)	2116(55)	2116(55)	3.71	3.31	3.68			
L4								1.2	1.2	1.2
	Core	2-3313	2-1080	1-1652	3.71	3.25	3.8	7.8	6.0	6.0
L5								1.2	1.2	1.2
	Prepreg	3313(54)	2116(55)	2116(55)	3.71	3.31	3.68	7.4	6.72	9.92
		3313(54)	106(75)	2116(55)	3.71	3.11	3.68			
L6								1.2	1.2	1.2
	Core	1-3313	1-2116	1-2116	3.71	3.38	3.7	3.9	5.0	5.0
L7								1.2	1.2	1.2
	Prepreg	1078(72)	1080(65)	1080(65)	3.30	3.2	3.46	5.37	5.12	5.52
		1035(70)	1080(65)	1080(65)	3.35	3.2	3.46			
L8	Foil							1.6	1.6	1.6
	Mask							0.8	0.8	0.8

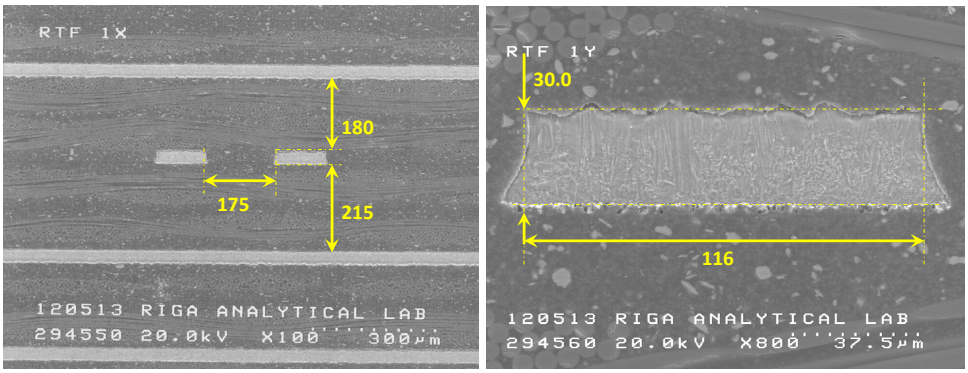
First, the manufactured boards were cross-sectioned to accurately verify all the dimensions of the transmission lines. Figure 3 shows the cross-section of the board with Isola's FR408HR, Nelco N4000-13 EPSI, Megtron 6 with RTF and HVLP finishes. The dimensions for the conductor thickness, width, the trace spacing, and the top and bottom layer heights are all marked in *microns (μm)*.



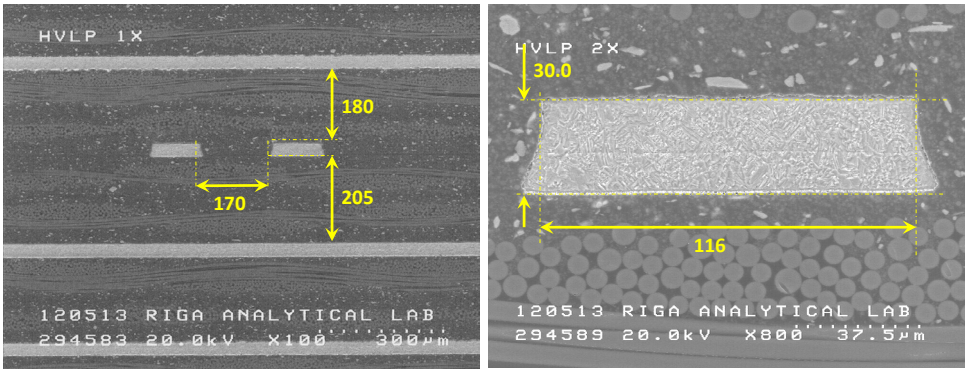
(a)



(b)



(c)



(d)

Figure 3: Micro-photographs of cross-sections of the traces showing copper roughness, (a) FR408H, (b) Nelco N4000-13EPSI, (c) Megtron 6 RTF, (d) Megtron 6 HVLP boards (dimensions are in *µm*).

Scattering parameter measurements are taken with a 4-port *67-GHz* vector network analyzer (VNA) using high-frequency probes with *200 um*-pitch GSSG configuration and high-frequency snap-on connectors. The two set of differential nets with *6-in.* and *12-in.* long traces for FR408HR, Nelco N4000-13 EPSI, Megtron 6 with RTF, and HVLP finish are measured. The measured differential and common mode insertion loss for the *12 in.* traces of the four boards are show in Figure 4. The simulated insertion losses of similar structures using FR4 boards are also plotted for comparisons. The plots show attenuations that agree with the electrical properties of these laminates given in Table I. The measured differential insertion loss of the Megtron 6 with HVLP finish shows about *2 dB* improvement over that of the Megtron 6 with RTF finish at *25 GHz*. The Megtron 6 with HVLP finish also shows about *4 dB* and *6 dB* improvements over Nelco N4000-13 EPSI and FR408HR, respectively. The *12-in.* trace in Megtron 6 with HVLP laminate shows about *20 dB* less loss when compared to similar trace in FR-4 board.

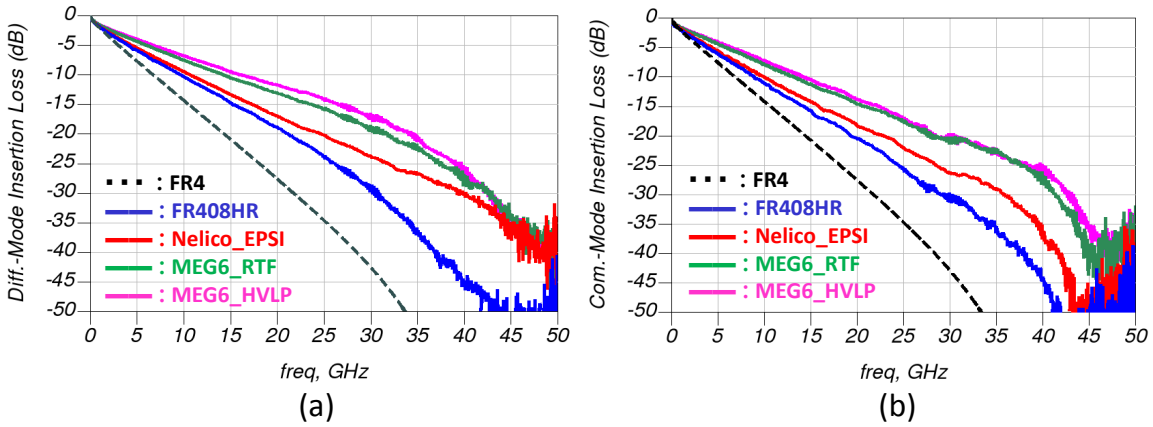


Figure 4: Magnitude of the measured (a) differential and (b) common-mode insertion losses are shown for the four boards: Megtron 6 HVLP (pink), Megtron 6 RTF (Green), Nelco N4000-13 EPSI (red), and FR408HR (blue). The insertion loss of typical FR-4 board is also shown from simulation (black dashed line).

The differential group delays of the *12-in.* traces are calculated from the measured four-port S-parameters. The delays per inch of the four boards are plotted as functions of frequency in Figure 5 (a). The simulated group delay for FR-4 board is also included in the plots. The Nelco N4000-13 EPSI shows the smallest delay as expected from the dielectric constant value of this laminate given in Table I. The typical FR-4 shows the longest delay as predicted from its higher dielectric constant.

Time-domain simulations are also performed using the measured S-parameters to calculate the single-bit response for an excitation of a pulse with amplitude of *1 V* and width of *20 ps* (corresponding to a data rate of *50 Gbps*) and rise and fall time of *8 ps*. Figure 5(b) shows that the single-bit responses of the Megtron 6 board experienced the least attenuations as predicted by glancing at the differential insertion loss shown in Figure 4(a). On the other hand, the single-bit responses for FR-4 suffered the larger attenuation and edge degradation closely followed by FR408HR when compared to the Megtron 6 boards. Although the single-bit response of the Nelco N4000-13 EPSI suffered

similar attenuation and dispersion as FR408HR, it experienced the least delay due to its low dielectric constant.

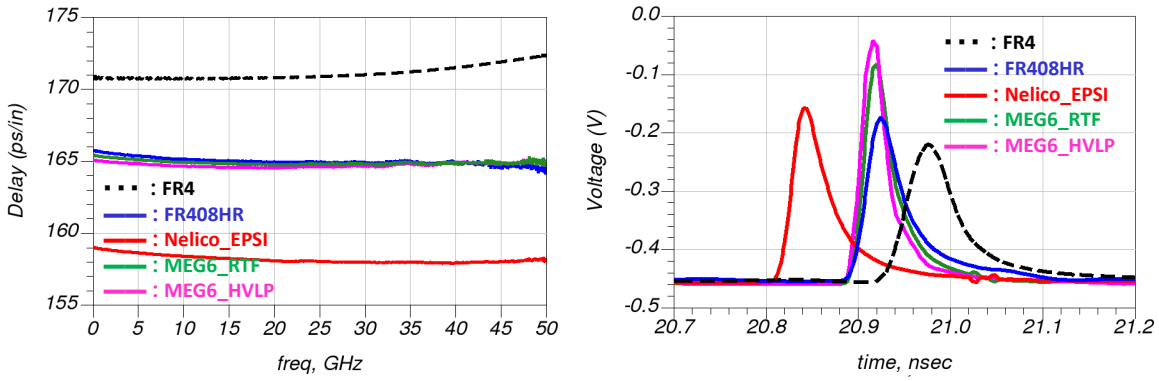


Figure 5: (a) The delays per inch and (b) the single-bit responses (*at 50 Gbps*) of the 12-in. long traces are shown for the four boards: Megtron 6 HVLP (pink), Megtron 6 RTF (Green), Nelco N4000-13 EPSI (red), and FR408HR (blue) and FR-4 (black). The group delay and pulse response of FR4 board are from simulation.

Next, we used the measured S-parameters measured of the two stripline of length of *6 in.* and *12 in.* to identify broadband dielectric and conductor roughness models using the generalized modal S-parameters [7]-[8]. The detail of the method is explained in the next section. The ability to properly separate conductor and dielectric losses for a wide range cross-section and low-loss dielectric is very critical to construct models that agree with measured data for wide-range cross-section used in board design. The accurate transmission line and transition models are then used for performing analysis and optimization of high-speed interconnects operating at *50 Gbps*.

Broadband Material Models

The longest interconnects, commonly found in backplanes and cables, can be formally defined and simulated as transmission line segments. Models for transmission lines are usually constructed with a static or electromagnetic field solvers. Transmission lines with homogeneous dielectrics (striplines) can be effectively analysed with quasi-static field solvers and lines with inhomogeneous dielectric may require analysis with a full-wave solver to account for the high-frequency dispersion [7], [8]. **Accuracy of transmission line models are mostly defined by availability of broadband dielectric and conductor roughness models.** Wideband Debye (Djordjevic-Sarkar) and multi-pole Debye models [8] are examples of causal dispersive dielectric models suitable for accurate analysis of PCB and packaging interconnects. **Parameters for such models are usually not available from manufacturers and have to be identified.** To simulate effect of conductor roughness, Huray's snowball [9] and modified Hammerstad [10] conductor roughness models can be effectively used. **Parameters for these roughness models are also not readily available from the PCB manufacturers.** Manufacturers of dielectric laminates usually provide dielectric parameters at 1-3 frequency points in the best cases. Those frequency points may be acceptable to define the wideband Debye model. Manufacturers of copper foils typically do not have parameters for the electrical

roughness models. Thus, meaningful interconnect design and compliance analysis must start with the identification or validation of dielectric and conductor roughness models over the frequency band of interest. **Availability of accurate broadband material models is the most important element for design success.** Validation or identification of dielectric and conductor models can be performed with generalized modal S-parameters (GMS-parameters) [11]-[12].

Before identification of the conductor roughness model, it is important to verify all dimensions of the test structures on the board. In particular, cross-sections of the transmission lines and length difference between two line pairs have to be accurately measured before the identification. Quality of measured S-parameters has to be estimated and TDR has to be used to verify consistency of the test fixtures.

The basic procedure for the dielectric and conductors surface roughness models identification is illustrated in Figure 6 can be performed as follows (implemented in Simbeor software [14]):

1. Measure scattering parameters (S-parameters) for at least two transmission line segments of different length (L1 and L2) and substantially identical cross-section.
2. Compute generalized modal S-parameters of the transmission line segment difference L=|L2-L1| from the measured S-parameters following procedure described in [13] and [14].
3. Compute GMS-parameters of line segment difference L:
    a. Guess material models and model parameters.
    b. Compute generalized modal S-parameter of line segment difference L by solving Maxwell's equations for line cross-section as described in [11], [12].
4. Compare GMS-parameters and adjust model to minimize the difference or finish.
    a. Compare the measured and computed generalized modal S-parameters.
    b. If the difference is larger than a threshold, change model parameters (or model type) and repeat steps (3b)-(4).
    c. If the difference is less or equal to threshold, the conductor roughness model is found.

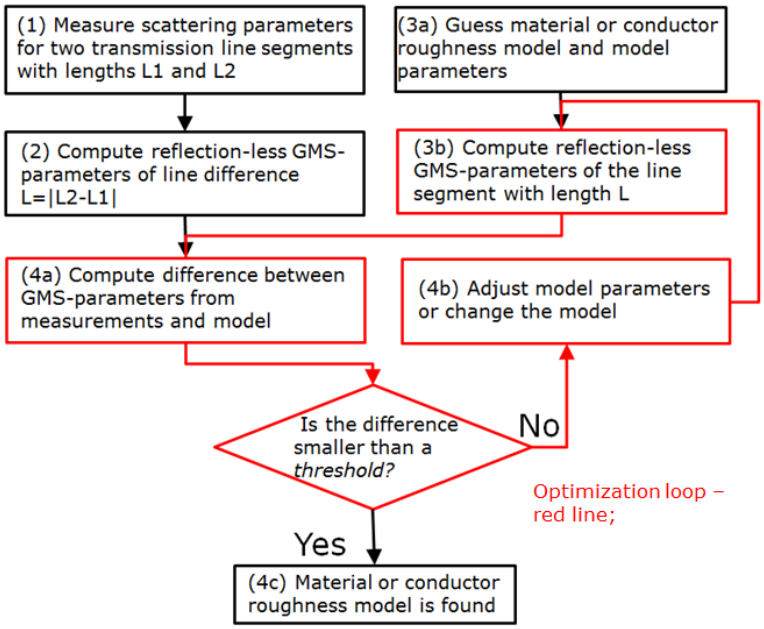


Figure 6: Dielectric material and conductor surface roughness model identification procedure.

As an example of material parameters identification, we first use board made with FR408HR. The first step is to measure the S-parameters with high quality for *6 in.* and *12 in.* differential strip line segments with the differential probe launches. Magnitude of the single-ended reflection and transmission parameters for *6 in.* and *12 in.* lines are shown on the Figure 7:

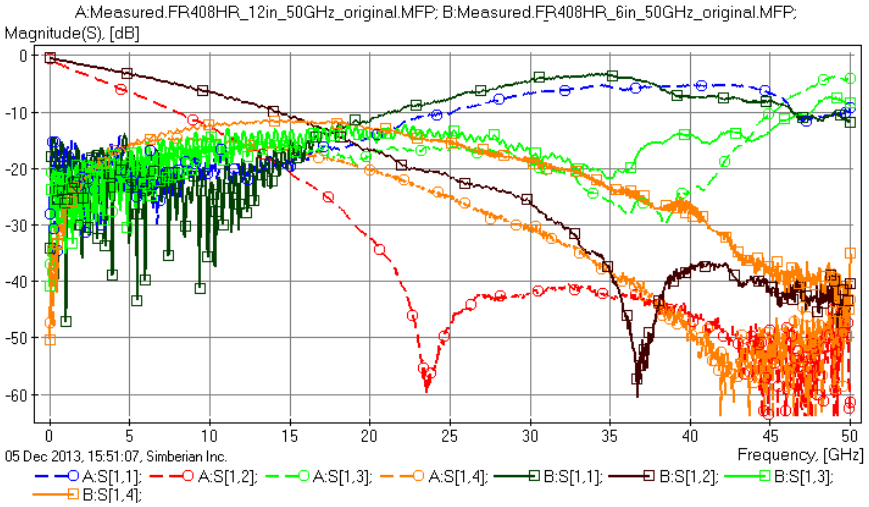


Figure 7: Elements of one row of measured single-ended S-matrix for 6-inch (solid lines) and 12-inch (dashed lines) differential line segments.

Quality of the measured S-parameters is estimated with metrics describe in [15] (implemented in Simbeor software [14]). For *12-in.* segment passivity metric is *100%,* reciprocity is *96.7%* and the final quality of S-parameters estimated with the rational approximation is *95.6%.* S-parameters for *6-in.* segment have passivity *100%,* reciprocity *94%* and final quality *94.6%.* Some metrics are not perfect (reciprocity and final quality), but may be acceptable for the material parameters identification. Additional inspection was performed to reveal non-symmetry of the test fixtures. Figure 8 shows four reflection parameters for *6-in.* segment. If the structure would have geometrical symmetry as designed, all *4* reflection parameters would be identical, but they are not. The reason is explained later.

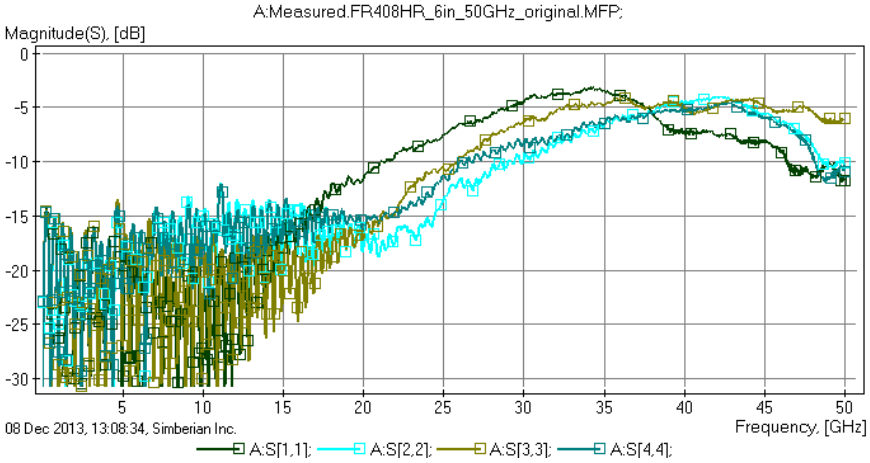


Figure 8: Magnitude of single-ended reflection parameters for *6-in.* differential line segments. Reflections from all 4 ports are expected to be close, but they are not.

To further pre-qualify the test fixtures, TDR is computed with the rational approximation of S-parameters and bandwidth-limited *20 ps* Gaussian step. From the single-ended TDR plots shown on the Figure 9, we can observe relatively large variations of the impedance (more than *4 Ohm*) between conductors in pairs as well as along the same conductor.

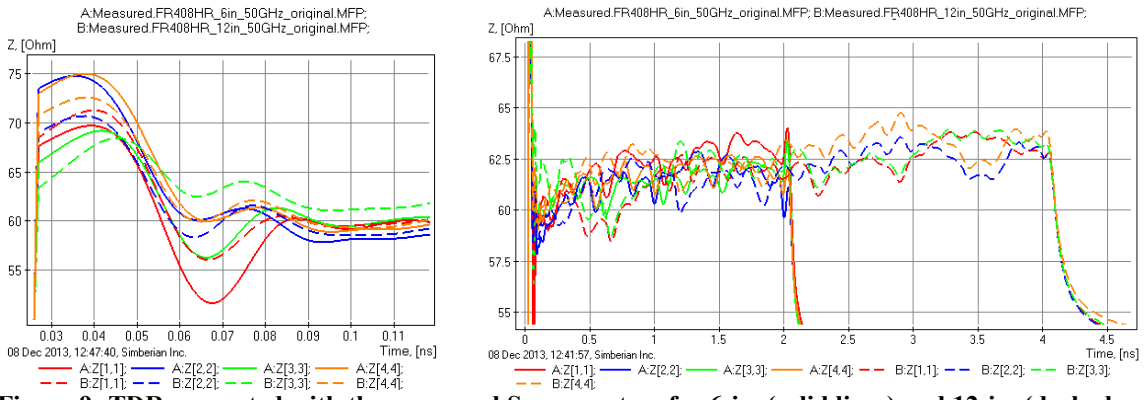


Figure 9: TDR computed with the measured S-parameters for 6-in. (solid lines) and 12-in. (dashed lines) differential segments (20 ps Gaussian step excitation from all 4 ports). Large variations of the impedance can be observed at the launches and along the traces.

The fiber weave effect caused by difference in dielectric properties of glass fiber and fill resin may be possible problem here. Another explanation of the large impedance variation is differences in the manufactured stripline width and distance along the lines. The line segments are not uniform as required for the material identification procedure. This problem was observed only on FR408HR board and has to be investigated further. In addition to the impedance variations along the lines, we can see even larger impedance variation at the launches (about *10 Ohm*) on the right TDR graph on Figure 9. Differences in the geometry of the launches may explain this – it will be further investigated. Overall the observed impedance variations is just another form of the problem with the differences in the reflection parameters observed earlier in Figure 8. To identify the dielectric model, we compute reflectionless GMS-parameters of *6 in.* differential line shown in Figure 10 from the measured S-parameters of *6 in*. and *12 in.* segments.

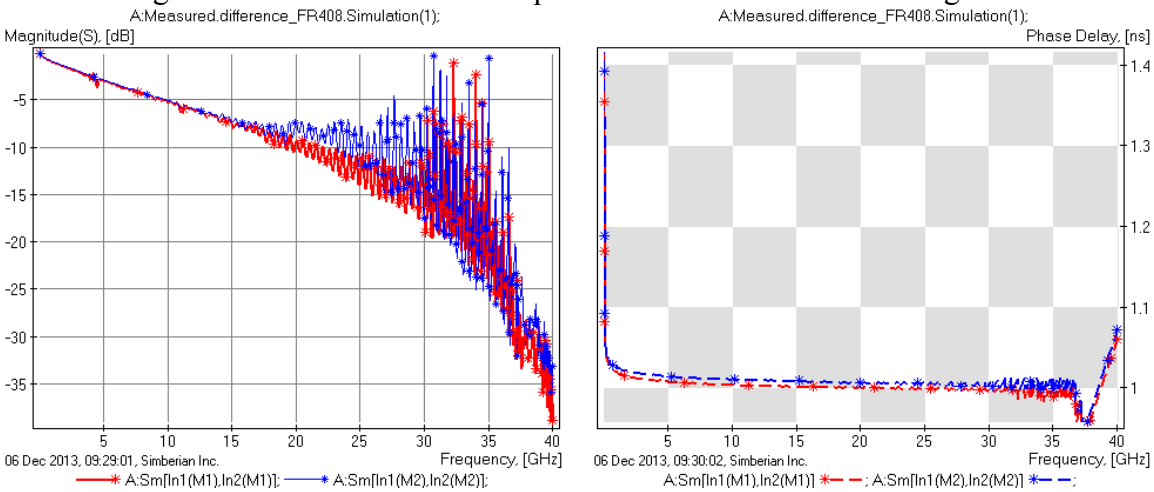


Figure 10: Generalized modal S-parameters: insertion loss (left graph) and phase delay (right graph) for odd mode (red line) and for even mode (blue lines).

Generalized insertion loss is becoming noisy above *15-20 GHz* and phase delay above *30-35 GHz*. The inhomogeneity of line segments and non identities of the launches reduced the frequency range of the extracted GMS-parameters. GMS-parameters are sensitive to non-idealness of the test fixtures was investigated in [16]. Though, insertion loss values at frequencies below *20 GHz* and phase delay values at frequencies below *30-35 GHz* can be still used to build a frequency-continuous homogenized dielectric model such as wideband Debye model [8], [11], [12]. First, we identify dielectric constant as one homogeneous wideband Debye model with dielectric constant of *3.76* and loss tangent of *0.012* at *1 GHz*. GMS-parameters of *6.15* in. differential line model are used to match the measured GMS-parameters as shown on Figure 11.

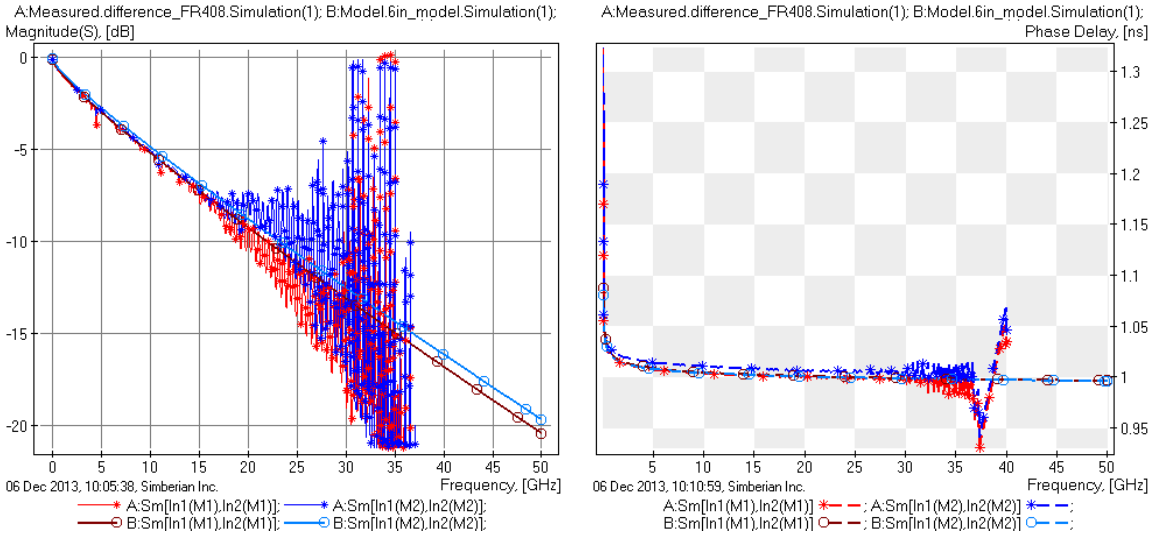


Figure 11: Measured (lines with *) and modeled (lines with o, cross-section from Figure 2(a), homogeneous dielectric model) generalized modal S-parameter for FR408: insertion loss (left graph) and phase delay (right graph) for odd mode (red and brown lines) and for even mode (blue lines).

After additional inspection we have found that the difference of line length between *12* and *6 in*. test fixtures was actually *6.15 in.* With exactly 6 in. line the extracted dielectric constant is *3.96* that is considerably high than *3.66* that in the specification for FR408HR. The priority during the dielectric mode fitting procedure was for the odd or differential mode at frequencies below *15 GHz*. With the homogeneous dielectric model the phase and group velocities of both modes are almost identical as we can see from the graphs. Though, measured phase delay of the even mode is slightly larger than for the odd mode. It indicates that the dielectric behaves as inhomogeneous. Resonances in the measured single-ended transmission parameters S_{12} visible at about *23* and *36 GHz* on Figure 7 also indicate that the propagation velocities of two modes are different. In addition, it is clearly visible on Figure 2(a) that dielectric between and around the strips is mostly resin (no glass). This can be modelled as differential stripline with two dielectrics – resin around the strips and composite dielectric elsewhere as shown on Figure 12.

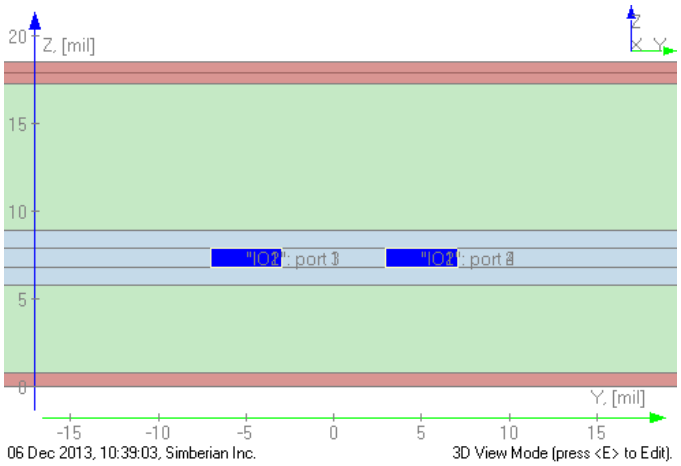


Figure 12: Model of cross-section with inhomogeneous dielectric – blue layers are filled with resin and green with composite dielectric.

Properties of two dielectrics are identified as wideband Debye models by matching generalized phase delay and insertion loss as illustrated on Figure 13.

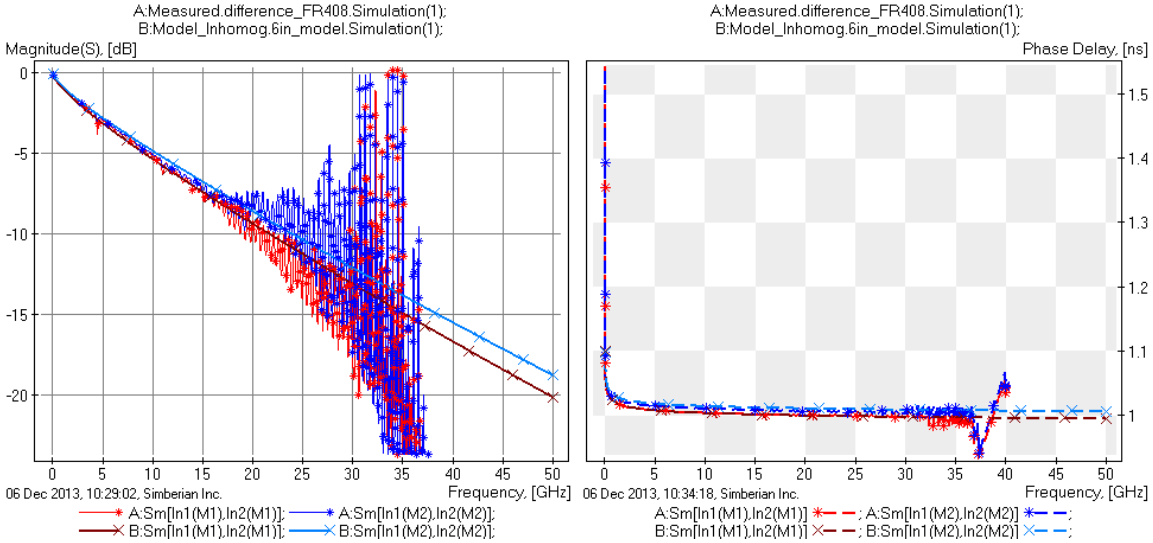


Figure 13: Measured (lines with *) and modelled (lines with o, cross-section from Figure 2(a), inhomogeneous dielectric model) generalized modal S-parameter: insertion loss (left graph) and phase delay (right graph) for odd mode (red and brown lines) and for even *mode (blue lines).*

The composite dielectric (green layers on the Figure 12) has dielectric constant of *3.95* and loss tangent of *0.01* and resin (blue layers) has dielectric constant of 3.5 and loss tangent of *0.012*, both at *1 GHz*. Larger dielectric constant of and lower loss tangent for the composite material can be explained by the higher content of glass in the regions above and below the strips. Now we can clearly see that phase delays for the odd and even modes in the model are different as in the measured data.

Finally, for preliminary verification of the constructed dielectric model, we simulate probe to probe link path. Two launch models are, shown in Figure 14, investigated. The signal vias on the manufactured board were back-drilled, but as we do this analysis and

write the paper there are no data on how exactly the back-drilling was performed. In fact, it looks like the back-drilling was not done with high accuracy and that caused substantial differences in the reflection parameters observed in Figure 8 and 9. To investigate possible boundaries, two structures have been simulated for the preliminary analysis – one with the maximal length of the stubs and another with the minimal via stub as shown in Figure 14. Two lanch models were concatenated with about *5.88 in.* differential transmission line model with in-homogeneous dielectric. Computed mixed-mode S-parameters are compared with the measured one in Figure 15.

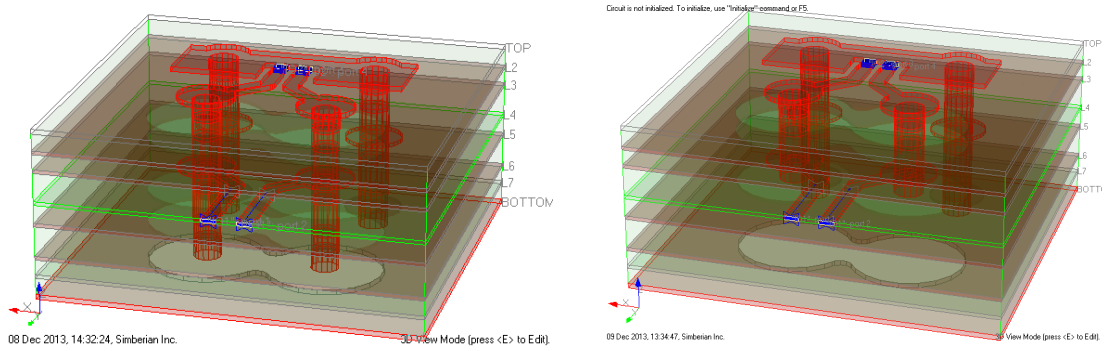


Figure 14: 3D model of the probe launch with and without via stub. Distance between signal vias is about *40 mil*, distance from signal vias to stitching vias is also about *40 mil*. That localizes the structure only up to about *20 GHz*.

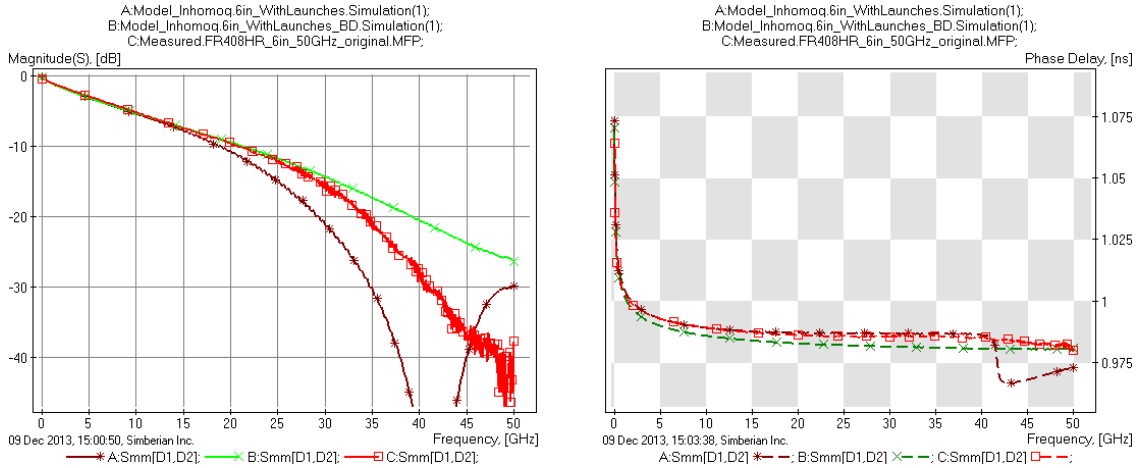


Figure 15: Measured (red lines) and modeled with long launch via stubs (brown lines) and short via stubs (green lines) differential mode insertion losses (left graph) and phase delay (right graph) of *6 in*. probe-to-probe link path.

Two models predict two possible boundary situations on manufactured board. We can observe good correlation of differential insertion losses in both models below *20 GHz*. Phase delays for differential mode is almost on top of the measured data up to *40 GHz* for the case with long via stubs, and just *4 ps* off for the case with short via stubs. The model with long launch via stubs predicts resonance in the differential mode around *41 GHz* and causes substantial increase in the insertion loss in the model at frequencies above *20 GHz*. On the other hand, if stubs are almost completely removed, the model exhibits smaller than measured insertion losses at frequencies above *30 GHz*. Measured structure

did not show the effect of stub resonance below *50 GHz*, but probably still has some via stubs with unknown lengths. The structure has to be cross-sectioned for further investigation. Though, the usefulness of this may be questionable – as we can see from TDR on Figure 9, all launches have substantial differences and it would be difficult to reproduce it in the analysis. Gradual loss of the localization property of the launch vias above *20 GHz* may also contribute into the large impedance variation – non-localized launches become dependent on the position on the board. Another source of the impedance differences may be de-embedding and slight difference in positioning of the probes.

The two boards made of Megtron 6 had smaller variation in the impedance along the line (within *2 Ohm*), but had similar problem with the large impedance variations at the launches. Though, magnitudes of GMS-parameters were good for the identification up to *22-25 GHz* and phase delay up to *45 GHz*. Board made of Nelco N4000-13EPSI also had large impedance variation at the launches and, in addition, variation of the impedance along the traces up to *4-5 Ohm* with even larger variations in the middle of the *12 in.* test fixture (a discontinuity). Useful frequency range of GMS-parameters was reduced to *15-17 GHz* for insertion loss and about *30 GHz* for phase delay. For all three boards we have identified two models, one with all losses included into dielectric model and shown in Table III. To construct another model we followed algorithm of the loss effect separation suggested in [13]. Loss tangent in dielectric model was set equal to the value provided in the material specifications. Then, modified Hammerstad model for conductor roughness [10] was identified by matching generalized insertion loss. The results are listed in Table IV. The surface roughness (rms of the peak-to-value height), and the surface roughness factor are the parameters as defined in the modified Hammerstad formula suggested in [10].

Table III. Identified wideband Debye dielectric model, include conductor roughness effect.

Model Parameters Board Types	Dielectric Constant @ 1 GHz	Loss Tangent @ 1 GHz
FR408HR with RTF copper	3.76	0.012
FR408HR with RTF copper, inhomogeneous	3.95, 3.5	0.01, 0.012
Megtron-6 with HVLP copper	3.69	0.0065
Megtron-6 with RTF copper	3.75	0.0083
Nelco N4000-13EPSI with RTF copper	3.425	0.011

Table IV. Identified wideband Debye dielectric model (dielectric constant and loss tangent) from material specification, and modified Hammerstad model for conductor roughness.

Model Parameters Board Types	Dielectric Constant @ 1 GHz	Loss Tangent @ 1 GHz	Surface Roughness, rms (um)	Surface Roughness Factor
Megtron-6 with HVLP copper	3.64	0.002	0.38	3.15
Megtron-6 with RTF copper	3.72	0.002	0.37	4
Nelco N4000-13EPSI with RTF copper	3.425	0.008	0.49	2.3

Lessons learned from the material identification:

During the project it took a few iterations to measure S-parameters with high quality metrics up to *50 GHz*. Manufactured test structures showed un-expectedly large impedance variations in the launches on all 4 boards and in transmission line impedances on 2 boards. It reduced the bandwidth of extracted GMS-parameters. Though, the extracted GMS-parameters were effectively used to build frequency-continuous dielectric and conductor roughness models up to *50 GHz*. Conductor roughness effect can be either accounted in the dielectric model or separated in the modified Hammerstad model as it is demonstrated for two Megtron 6 and Nelco boards. Both models are nearly identical if used for the cross-sections with same strip widths. Megtron 6 board with HVLP copper had just marginally smaller losses comparing to the case with RTF copper. RTF copper slightly increased the dielectric constant of Megtron 6, probably due to the capacitive roughness effect [10]. If mostly resin fills space around the strips and causes differences in the propagation velocity of modes, it must be accounted for in the model for better accuracy as it is demonstrated for FR408HR board. **Overall, the probe launches with back-drilled vias used on the test board are the major problem in the material identification and measurement to analysis correlation.** To make them predictable with simulation in isolation, they have to be re-designed with special attention to the localization and possibly with accurate and identical back-drilling.

Final Model Verification

Finally, the probe to probe link path is closely examined to study some of the discrepancies that are discussed in the previous sections. The launch structures at both ends of the traces that include via, via stubs and pads are examined carefully. The scattering parameters of the via and pad structures are generated using full wave electromagnetic solver. The full 3D structures with and without stub vias are shown in Figure 14. The frequency responses of the via and pad structures are analyzed as a function of the stub lengths. The side view of the via and pad structures with four different stub length are shown in Figure 16. The corresponding differential insertion loss and return loss are shown in Figure 17 (a) and Figure 17 (b), respectively. It is important to notice that in order to extend the bandwidth of the launch structure to *50 GHz* range, the lengths of the via stubs need to be small. Commonly accepted tolerance of minimum stub lengths of of *7±3* mil, after back drilling, can be limiting factror in accurately measuring the stripline characteristics at higher frequencies.

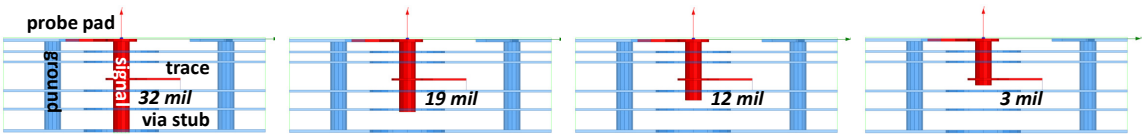


Figure 16: The side view of the launch structures used in 3D solver to study the impact of the lengths of via stubs.

After careful investgation, it is established that there are signifcant variations in the length of the via stubs. In order to accurately determine the length of the via stubs, digital microscope images of the back-drilled vias are taken. Figure 18 shows the top view and 3D images from a digital microscope of the back-drilled vias (holes).

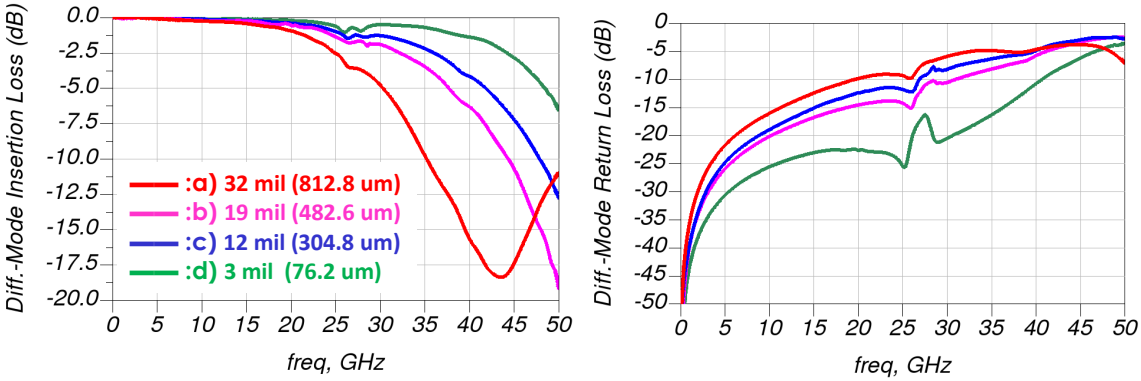


Figure 17: Differential insertion loss and (b) differential return loss of the lunch structures as a function of via stub length.

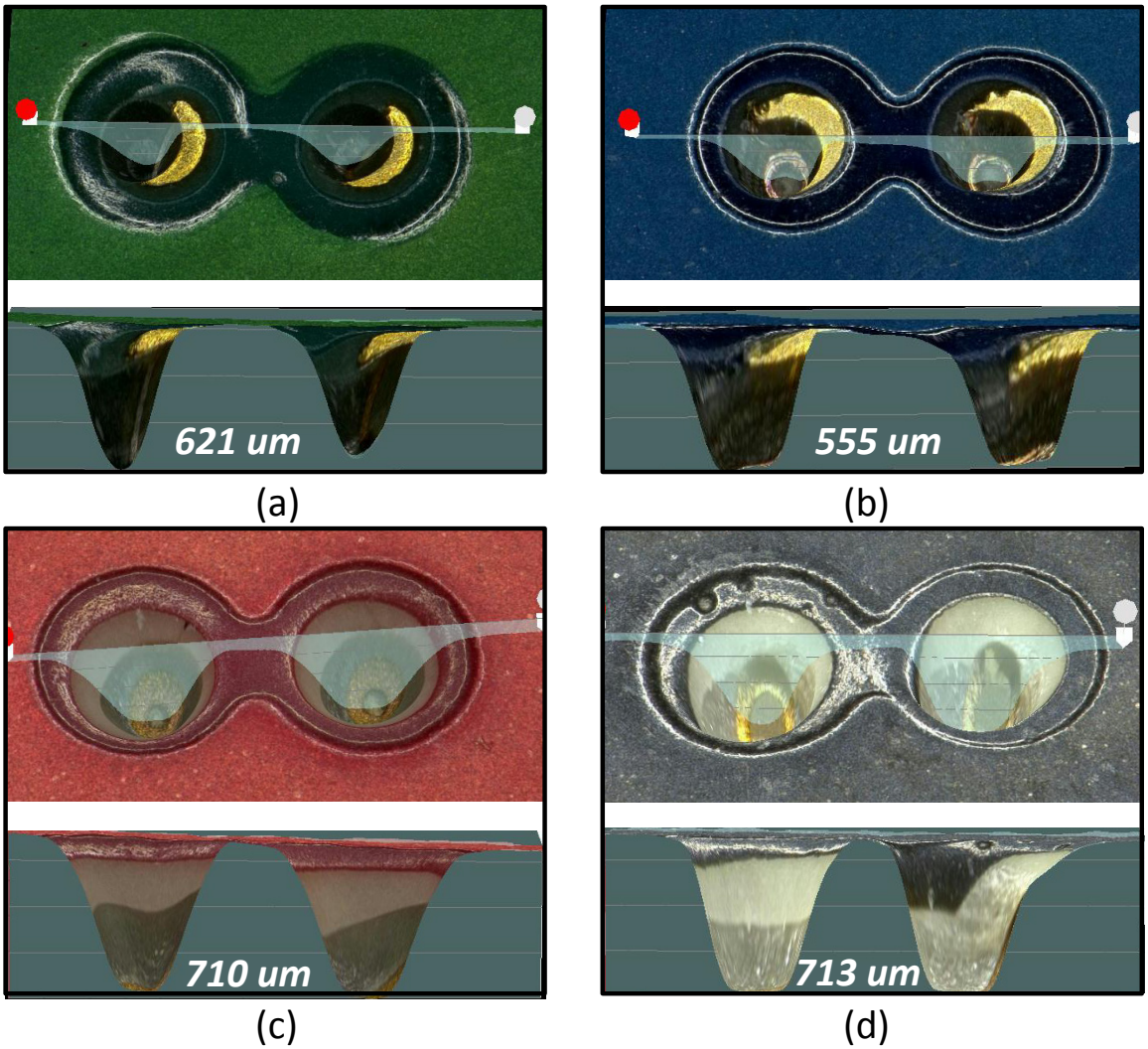


Figure 18: Top view and 3D images from a digital microscope of the back-drilled vias (holes) for (a) FR-408HR, (b) Nelco-N4000 13EPSI, (c) Megtron 6 RTF, and (d) Megtron 6 HVLP.

From the board cross-section of Figure 2 and the back-drilled via profile of Figure 18, the length of the via stub are estimated for the four boards as shown in Table V. Notice that the back-drilled holes are significantly various from board to board. We also noticed that the back-drilled holes show different depth even on the same board for vias very close to each other, as shown on Figure 18 (a). For the Megtron 6 RTF board, for example, the average back-drilled depth is *713 um*, the minimum and maximum depths are *681um* and *748 um*, respectively. In general, there are some via stubs that are succefully back drilled, some are partially backdrilled and some are not back-drilled, compeletly missed.

Table V : The board thickness, via and via stub length in *um*.

Board Types	Board Thickness	Pad to trace Via length	Back drill depth	Via stub length
FR408 HR	1470	600	620	250
Nelco N4000-13 EPSI	1360	540	555	265
Megatron 6 RTF	1400	560	710	130
Megtron 6 HVLP	1400	560	713	127

Based on the via stub length, the S-parameters of the via and pad structure are generated and cascaded to both ends of the trace model as shown in Figure 19. The trace model consists of transmission line models based on the parameters extracted for the four boards, given in Table III and IV. Then, frequency-domain linear simulations of the complete links are carried out to calculate the overall S-parameters of both *6 in*. and *12 in.* long traces. Then, the measured and simulated S-parameters are compared for multiple trace lengths and boards to verify the quality of the extracted trace models.

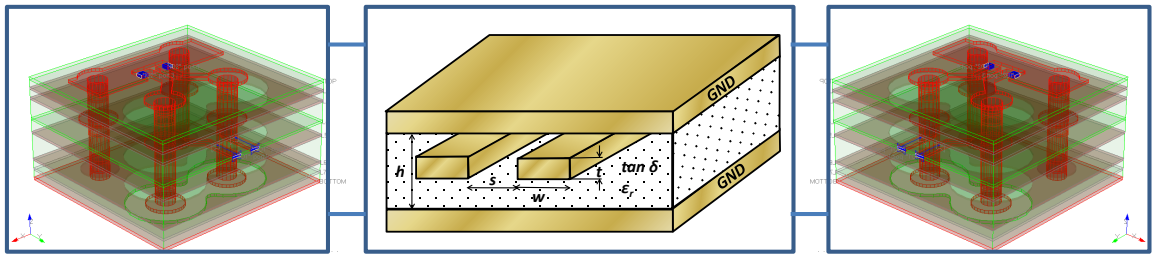


Figure 19: Cascade of the extracted transmission line model of the striplines and the S-parameters of the via and pad structures at both ends of the traces.

Figures 20 (a), (b), (c), and (b) show magnitude and phase (unwrap) of the differential insertion loss for *6-in.* and *12-in.* long traces for the FR408HR, Nelco N4000-13EPSI, Megtron 6 RTF, and Megtron 6 HLVP boards, respectively. The plots show good agreements between the measurements and the extract model parameters for all four boards over a wide frequency range. The minor divergence of the measurement and model results at very high frequency can be attributed to the uncertainty in the length of the remaining via stub.

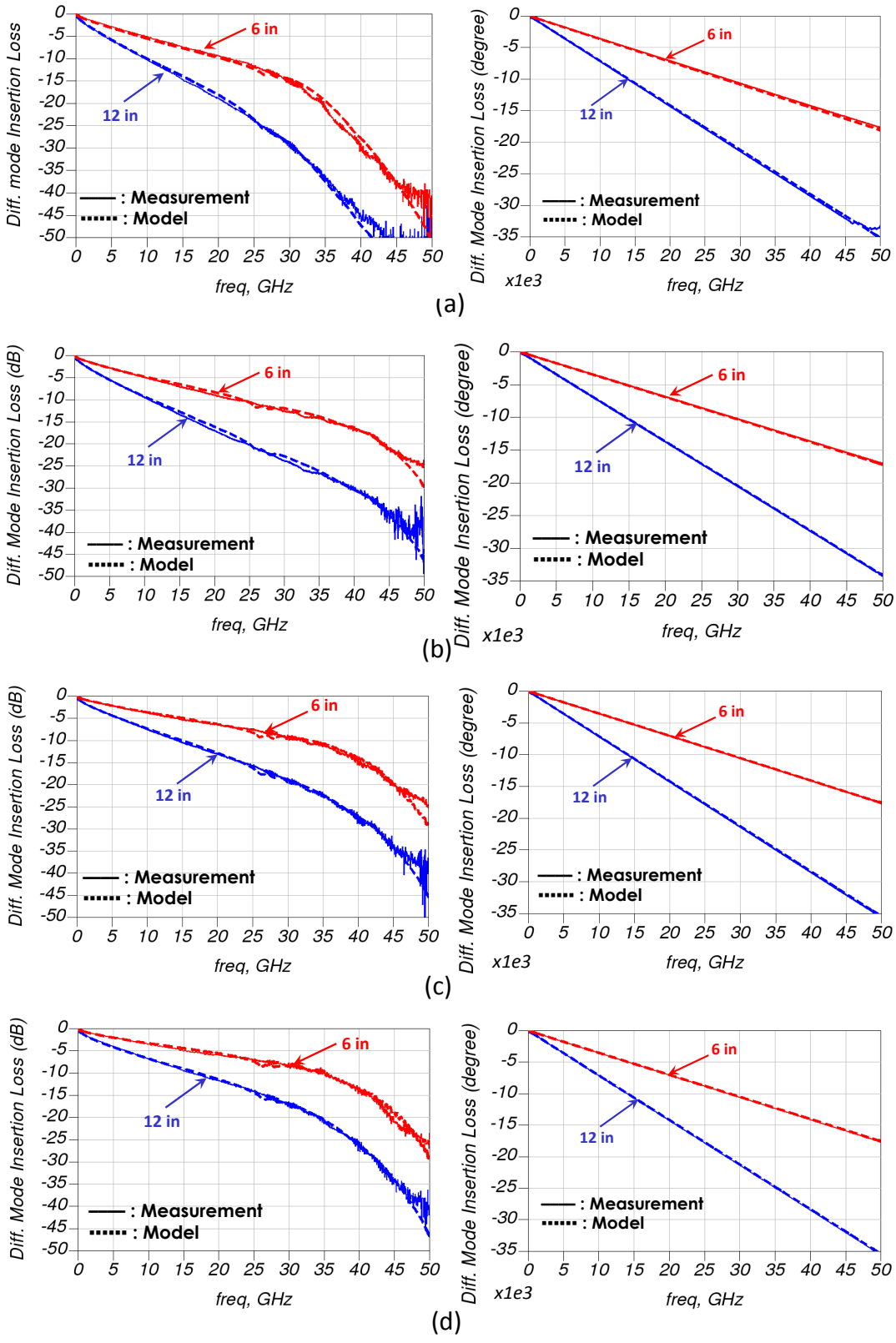


Figure 20: Magnitude and phase (unwrap) of the measured and simulated differential insertion loss for the four boards: (a) FR408HR, (b) Nelco N4000-13EPSI, (c) Megtron 6 with RTF finish, and (d) Megtron 6 with HVLP finish.

Conclusion

Several low-loss laminates are characterized over *50 GHz*. These low-loss boards can make it possible to extend the copper-based interconnect to *50 Gbps* backplane links. The outcome of the project is a systematic and practical methodology for identifying the dielectric and conductor roughness models, essential for accurate analysis of 50 Gbps interconnects. During the project we have learned the following lessons:

1. Formal S-parameters quality metrics are useful for pre-qualification of measured S-parameters;
2. Geometrically symmetric by design test fixtures was manufactured with substantial symmetry violations due to the manufacturing tolerances and fiber-weave effect;
3. Back-drilling of vias are the major symmetry violator and the roadblock in the material identification as well as in the model to measurement correlation;
4. Reduced bandwidth GMS-parameters can be still used to build frequency-continuous dielectric and conductor roughness models that provide model to measurement correlation up to *50 GHz* and beyond.

Acknowledgments

The authors would like to acknowledge the help and support of numerous people who helped with the project. Special thanks go to Matt Ortiz for performing the VNA measurements, Gnanadeep Kollipara for designing the boards, William Ng for taking the digital microscope images of the back-drilled vias, and Arun Vaidyanath for making the system engineer resource available to complete this study.

References

1. A. F. Benner, *et al.*, "A roadmap to 100G Ethernet at the enterprise data center," *IEEE. Communications Magazine,* vol. 45, no. 11, pp. 10-17, Nov. 2007.
2. R. Kollipara, *et al.*, "Practical design considerations for 10 to 25 Gbps copper backplane serial links," in *IEC DesignCon*, Santa Clara, CA, Feb. 6-9, 2006.
3. H. Braunisch, *et al.*, "High-speed flex-circuit chip-to-chip interconnects," *IEEE Transactions on Advanced Packaging Technologies*, vol. 31, no.1, pp. 82-90, Feb. 2008.
4. D. G. Kam, *et al.*, "Is 25 Gb/s on-board signaling viable?," *IEEE Transactions on Advanced Packaging Technologies*, vol. 32, no.2, pp. 328-344, May 2009.
5. IEEE P802.3bj™ 100 Gb/s Backplane and Copper Cable Task Force, http://www.ieee802.org/3/bj.
6. W. T. Beyene, *et al.*, "Advanced modeling and accurate characterization of a 16 Gb/s memory interface," *IEEE Transactions on Advanced Packaging Technologies*, vol. 32, no.2, pp. 306-327, May 2009.
7. Y. Shlepnev, Modeling frequency-dependent conductor losses and dispersion in serial data channel interconnects, Simberian App. Note #2007_02, http://www.simberian.com/AppNotes.php
8. Y. Shlepnev, Modeling frequency-dependent dielectric loss and dispersion for multi-gigabit data channels (with experimental validation), Simberian App. Note #2008_06, http://www.simberian.com/AppNotes.php
9. P. G. Huray, O. Oluwafemi, J. Loyer, E. Bogatin, X. Ye, Impact of Copper Surface Texture on Loss: A Model that Works, DesignCon 2010.
10. Y. Shlepnev, C. Nwachukwu, Roughness characterization for interconnect analysis. - Proc. of the 2011 IEEE International Symposium on Electromagnetic Compatibility, Long Beach, CA, USA, August, 2011, p. 518-523.
11. Y. Shlepnev, A. Neves, T. Dagostino, S. McMorrow, Practical identification of dispersive dielectric models with generalized modal S-parameters for analysis of interconnects in 6-100 Gb/s applications. DesignCon 2010.
12. Y. Shlepnev, System and method for identification of complex permittivity of transmission line dielectric, US Patent #8577632, Nov. 5, 2013, Provisional App. #61/296237 filed on Jan. 19, 2010.
13. Y. Shlepnev, System and method for identification of conductor surface roughness model for transmission lines, Patent Pending, App. #14/045,392 filed on Oct. 3, 2013.
14. Simbeor Electromagnetic Signal Integrity Software, www.simberian.com
15. Y. Shlepnev, Reflections on S-parameter Quality, DesignCon2011 IBIS Summit, Santa Clara, CA.
16. Y. Shlepnev, Sensitivity of PCB Material Identification with GMS-Parameters to Variations in Test Fixtures, Simberian app. note #2010_03, www.simberian.com